

2-line IPAD™, EMI filter with ESD protection

Features

- 2-line low-pass filter + ESD protection
- High efficiency in EMI filtering
- Lead-free package
- Very low PCB space occupation < 3.2 mm²
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

Complies with the following standards:

- IEC 61000-4-2
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883E - Method 3015-6 Class 3

Application

EMI filtering and ESD protection for USB port.

Description

The EMIF02-USB02F2 is a highly integrated array designed to suppress EMI / RFI noise for a USB port. The EMIF02-USB02F2 Flip Chip packaging means the package size is equal to the die size.

Additionally, this filter includes ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

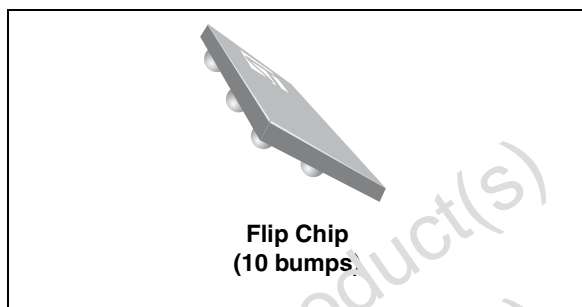


Figure 1. Pin layout (bump side)

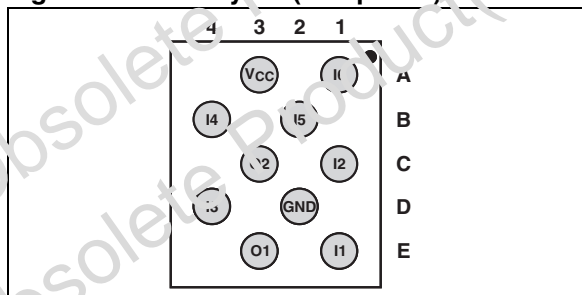
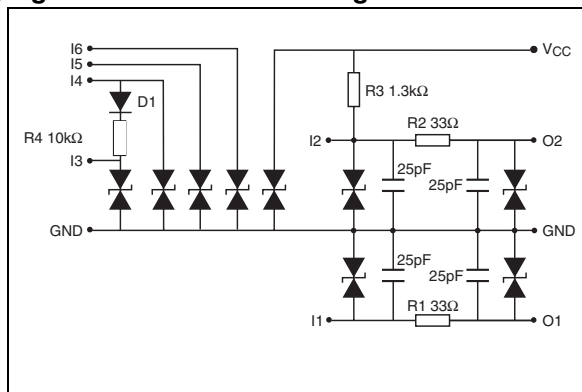


Figure 2. Basic cell configuration



1 Characteristics

Table 1. Absolute ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, air discharge	15	kV
	ESD discharge IEC 61000-4-2, contact discharge	8	
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	- 40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	- 55 to + 150	$^{\circ}\text{C}$

Table 2. Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter								
V_{BR}	Breakdown voltage								
I_{RM}	Leakage current @ V_{RM}								
V_{RM}	Stand-off voltage								
V_{CL}	Clamping voltage								
R_d	Dynamic impedance								
I_{PP}	Peak pulse current								
$R_{I/O}$	Series resistance between input and output								
C_{line}	Input capacitance per line								
Symbol	Test conditions					Min.	Typ.	Max.	Unit
V_{BR}	$I_P = 1\text{ }\mu\text{A}$					6			V
I_{RM}	$V_{RM} = 3\text{V}$		0.1	0.5	μA				
C_{line}	@ 0V			50	pF				
R_1, R_2	Tolerance $\pm 5\%$		33		Ω				
R_3	Tolerance $\pm 5\%$		1.3		k Ω				
R_4	Tolerance $\pm 5\%$		10		k Ω				
V_F	@ 1 mA (D1 diode)		1		V				

Figure 3. Attenuation measurement

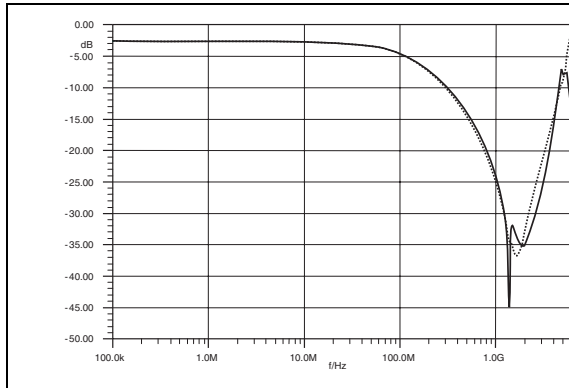


Figure 4. Analog crosstalk measurement (I1- O2)

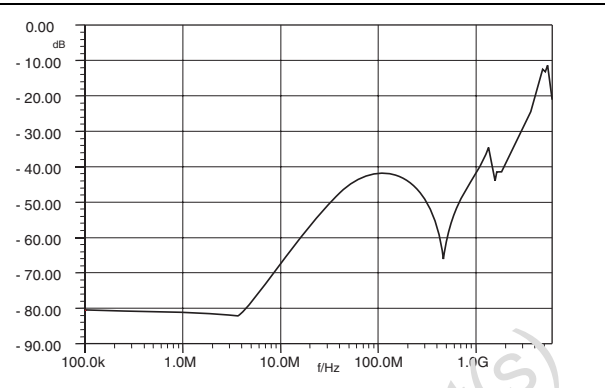


Figure 5. ESD response to IEC 61000-4-2 (+15kV contact discharge)

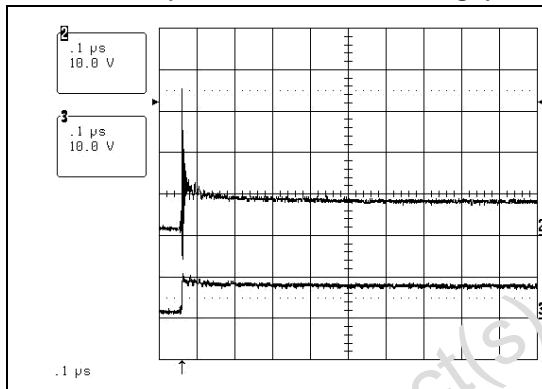
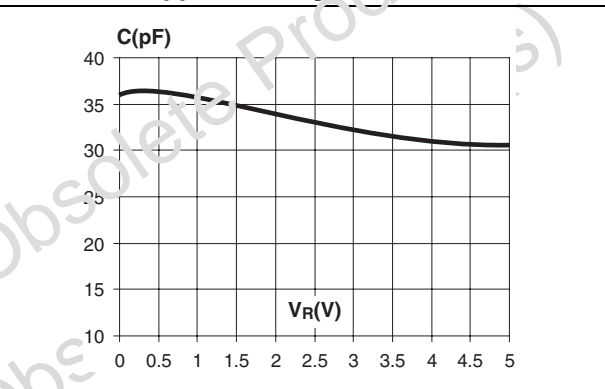


Figure 6. Line capacitance versus reverse applied voltage



Obsolete Product(s) - Obsolete Product(s)

2 Application information

Figure 7. Aplac model of D+ & D- cells

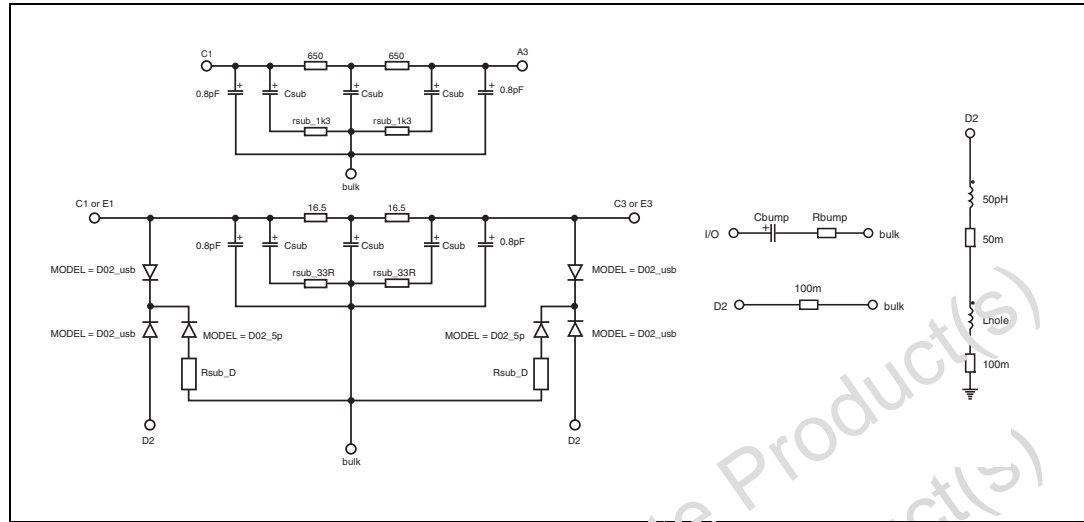
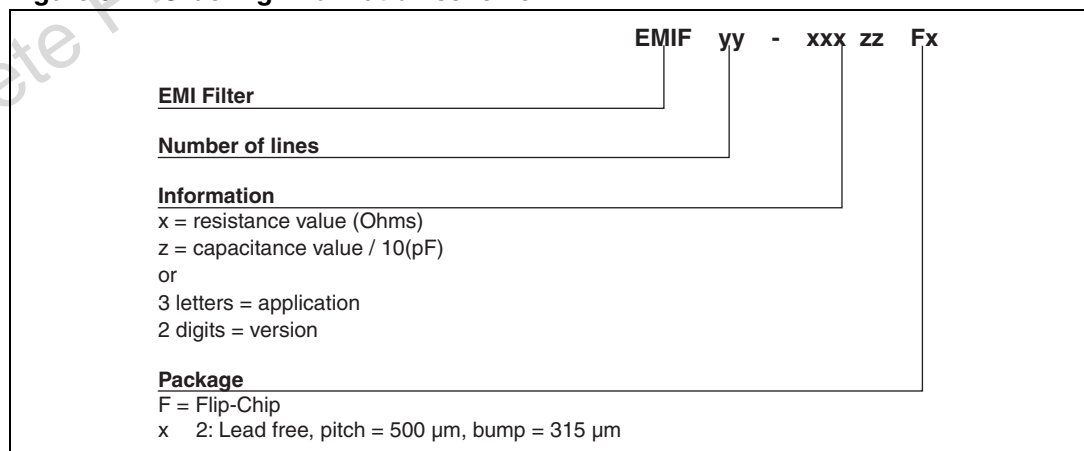


Figure 8. Aplac model parameters

Cz 17pF opt	D02_usb diodes model	D02_5p diodes model
Ls 0.4nH	+ BV = 7	+ BV = 100
Rs 0.1	+ BV = 1m	+ IBV = 1m
Rsub_D 10	+ CJC = Cz	+ CJO = 5p
Csub 0.3pF	+ M = 0.3333	+ M = 0.3333
Rsub_33R 16	+ RS = 2	+ RS = 2
Rsub_1k 1k	+ VJ = 0.6	+ VJ = 0.6
Ihole 1.0pH opt	+ TT = 100n	+ TT = 100n
Cbump 1.2pF opt		
Rbump 350		

3 Ordering information scheme

Figure 9. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 10. Flip Chip package dimensions

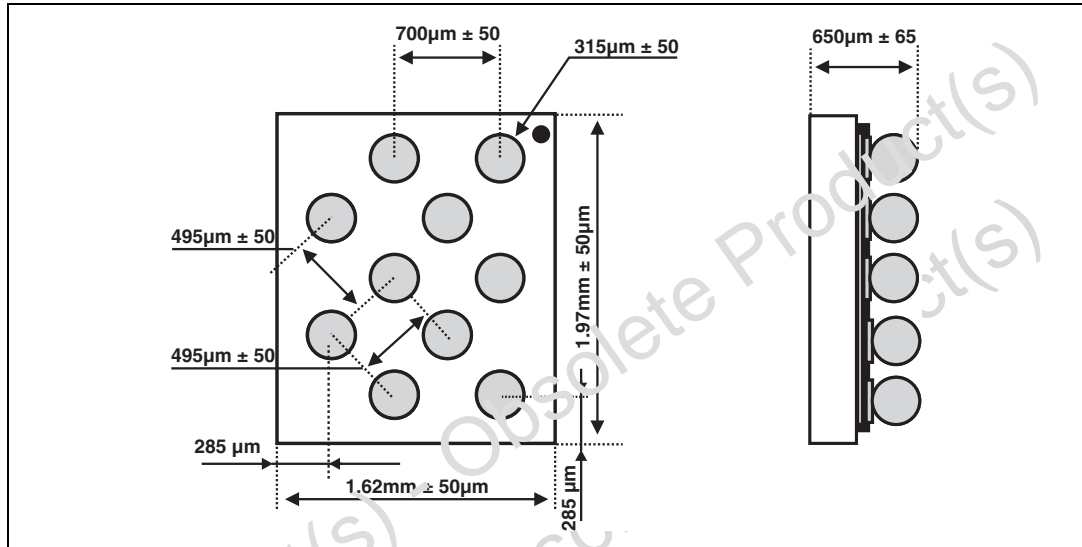
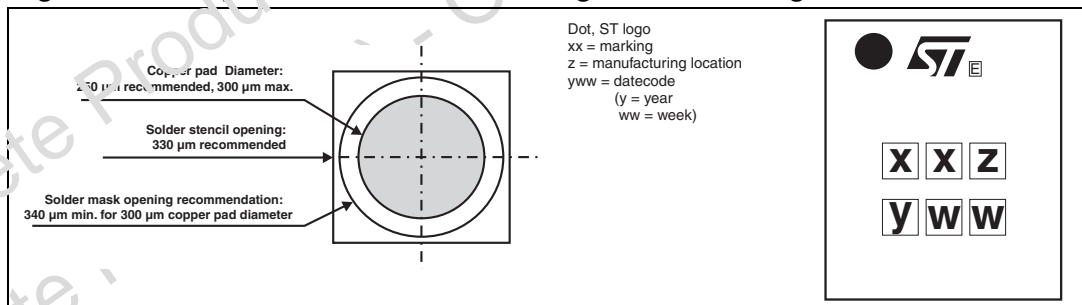


Figure 11. Footprint recommendations Figure 12. Marking



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