

PROTECTION PRODUCTS - RailClamp®
Description

RailClamp® TVS diode arrays are specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over-voltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients). The RClamp®7002M has been optimized for use on the next generation of ADSL interfaces. Their high surge capability makes them particularly useful in systems that utilize gas tubes as the primary protection component.

This device integrates surge rated, low capacitance steering diodes in a small MSOP-10L package. Each protection diode features a large area junction to minimize clamping voltage and increase reliability during high current surges. It has a maximum capacitance of only 10pF and may be used to protect two high-speed lines without sacrificing signal integrity. The RClamp7002M may be used on systems operating from 3.3 to 70 volts. This means that they may be used in applications that use the Central Office battery as the main supply.

The RClamp7002M is also designed for easy board layout by allowing the signal traces to run straight through the device. The high surge capability, ease of layout coupled with the low capacitance and clamping voltage of the RClamp7002M makes it the superior choice for protecting two high speed lines against high energy telecommunication surges.

Features

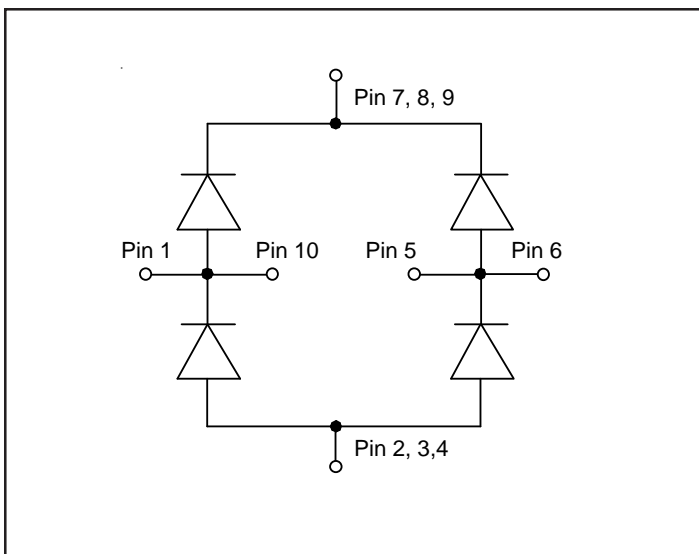
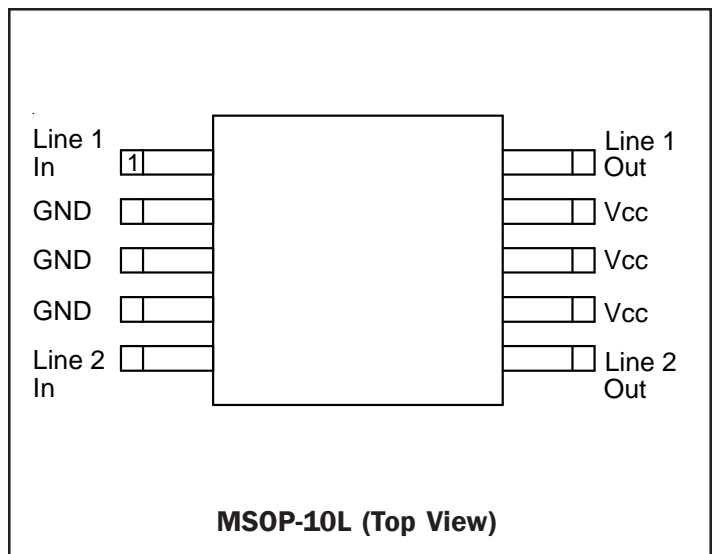
- ◆ 1000 Watts peak pulse power (**8/20µs**)
- ◆ Protection for high-speed data lines to
IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 1kV, 24A (1.2/50µs)
- ◆ Low clamping voltage: **10V at Ipp = 40A (8/20µs)**
- ◆ Array of surge rated suppression diodes
- ◆ Protects two high speed lines
- ◆ Low capacitance: **10pF** (I/O to Ground)
- ◆ Operating voltage range: 3.3 - 70V
- ◆ Small package saves board space
- ◆ Solid-state silicon-avalanche technology

Mechanical Characteristics

- ◆ JEDEC MSOP-10L package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking: Marking code and date code
- ◆ Packaging: Tape and Reel
- ◆ Lead Finish: Matte tin
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant

Applications

- ◆ ADSL Lines
- ◆ Central Office Equipment
- ◆ T1/E1 secondary IC Side Protection
- ◆ Small Office Home Office (SOHO) Applications
- ◆ WAN/LAN Equipment
- ◆ ISDN S/T Interface
- ◆ ATM Interfaces

Circuit Diagram

PIN Configuration


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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PP}	1000	W
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	70	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

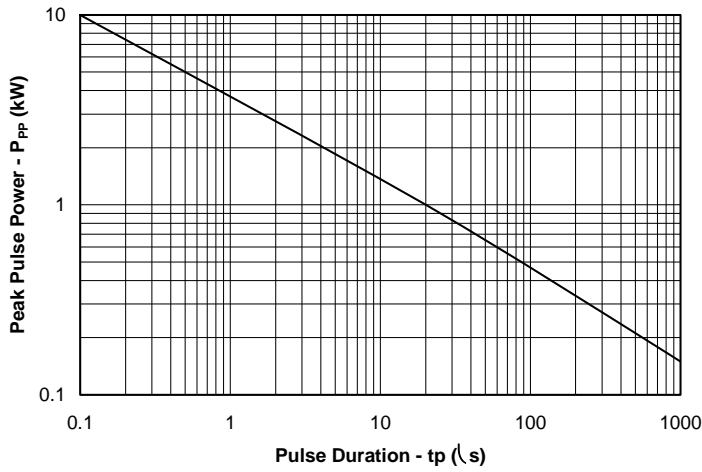
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				70	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 50\mu A$	85			V
Reverse Leakage Current	I_R	$V_{RWM} = 70V, T=25^\circ C$			5	μA
Forward Voltage	V_f	$I_f = 15mA$			1.2	V
Clamping Voltage	V_C	$I_{PP} = 1A, t_p = 8/20\mu s$ Any I/O pin to Ground			1.5	V
Clamping Voltage	V_C	$I_{PP} = 40A, t_p = 8/20\mu s$ Any I/O pin to Ground			10	V
Clamping Voltage	V_C	$I_{PP} = 70A, t_p = 8/20\mu s$ Any I/O pin to Ground			14.3	V
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz$ Any I/O pin to Ground			10	pF
		$V_R = 0V, f = 1MHz$ Between I/O pins		3		pF

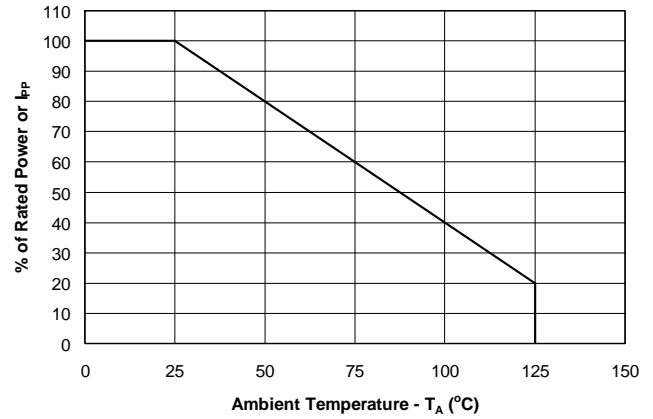
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Typical Characteristics

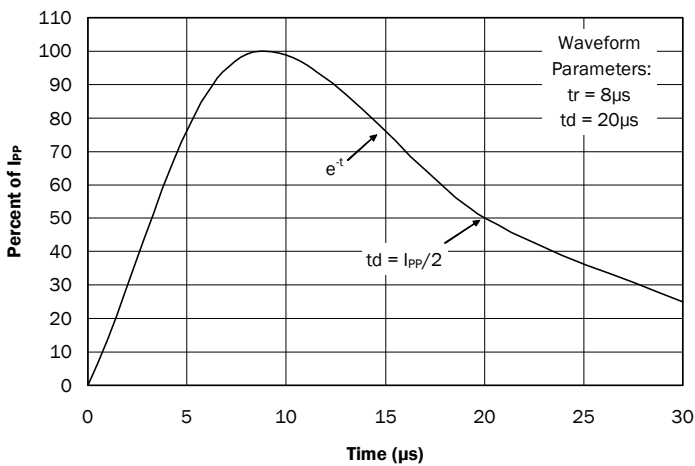
Non-Repetitive Peak Pulse Power vs. Pulse Time



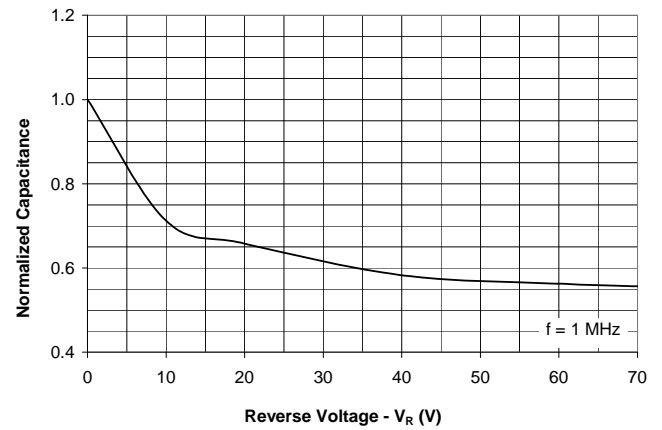
Power Derating Curve



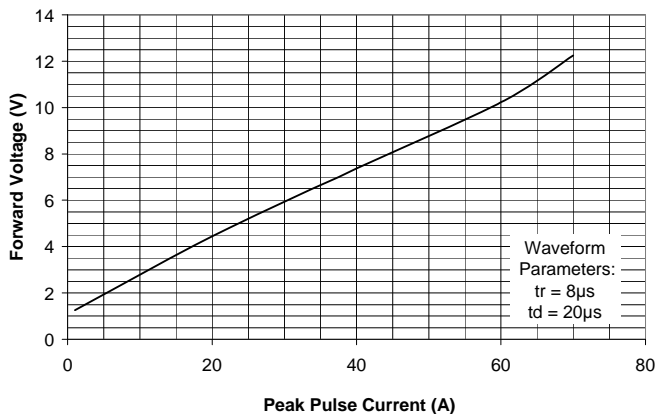
Pulse Waveform



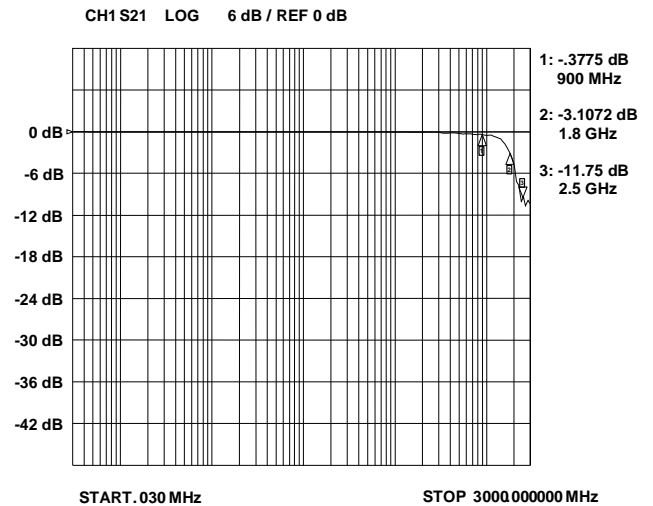
Capacitance vs. Reverse Voltage



Forward Voltage vs. Forward Current



Insertion Loss S21



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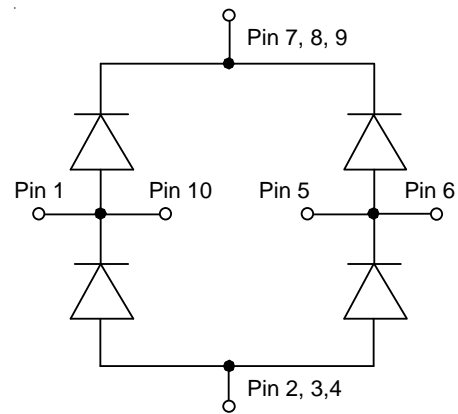
Applications Information

Device Connection Options for Protection of Two High-Speed Data Lines

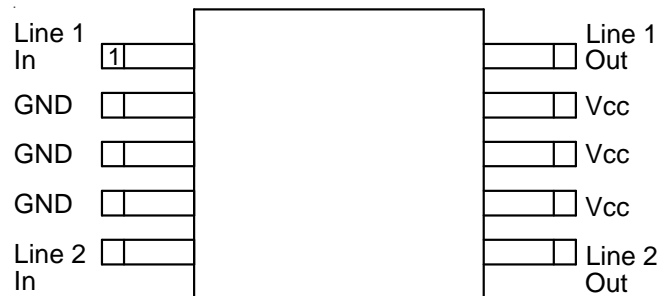
This device is designed to protect two data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_f) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data line inputs are connected at pins 1 and 5. The outputs are connected at pins 10 and 6 respectively. The negative reference is connected at pins 2, 3, and 4. These pins should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pins 7, 8, and 9. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pins 7, 8 and 9 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. An external TVS diode may be added between the supply rail and ground in order to prevent over-voltage on the supply rail.
2. In applications where no positive supply reference is available, or complete supply isolation is desired, an external TVS diode may be used as the reference. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

Schematic



Pin Configuration



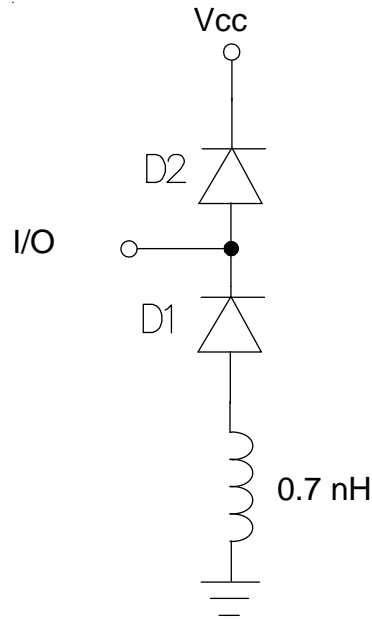
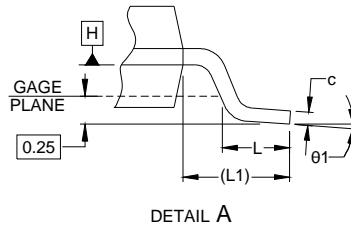
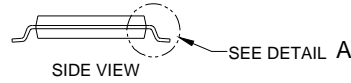
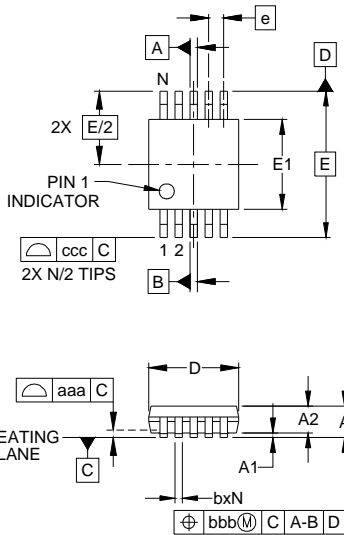
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Applications Information - Spice Model

RClamp7002M Spice Model

Table 1 - RClamp7002M Spice Parameters			
Parameter	Unit	D1 (LCRD)	D2 (LCRD)
IS	Amp	1.0E-20	1.0E-20
BV	Volt	200	200
VJ	Volt	0.53	0.53
RS	Ohm	0.037	0.14
IBV	Amp	1E-3	1E-3
CJO	Farad	3.5E-12	3.5E-12
TT	sec	2.541E-9	2.541E-9
M	--	0.142	0.142
N	--	1.1	1.1
EG	eV	1.11	1.11

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Outline Drawing - MSOP 10L

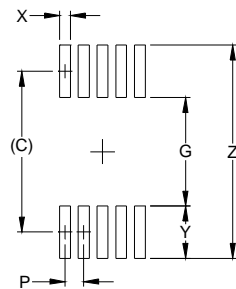


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
theta1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP 10L



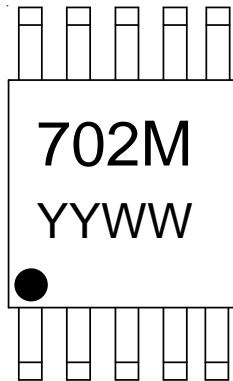
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

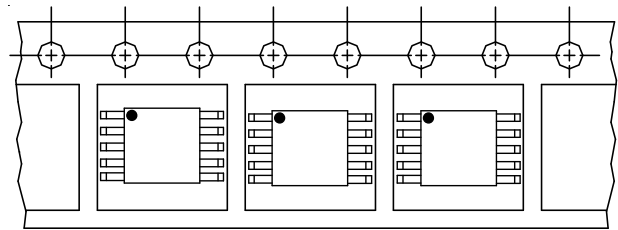
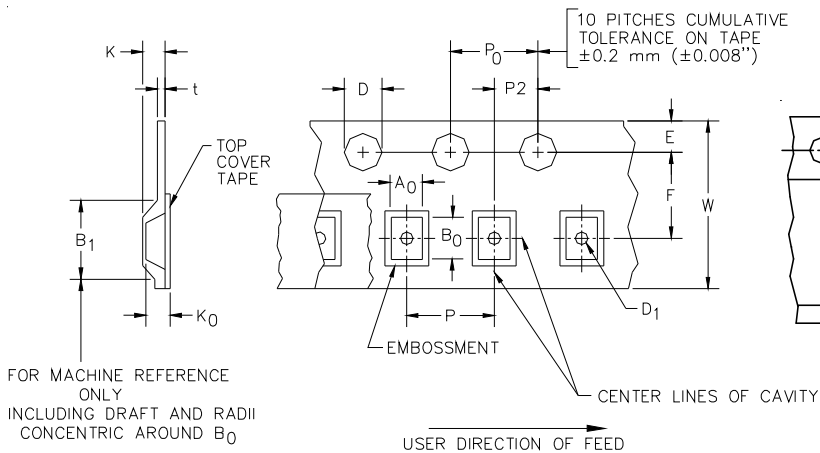
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Marking Codes



YYWW = Date Code

Tape and Reel Specification



Device Orientation in Tape

A0	B0	K0
5.30 +/-0.20 mm	3.40 +/-0.20 mm	1.40 +/-0.10 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
12 mm	8.2 mm	1.5 + 0.1 mm - 0.0 mm)	0.5 mm ±0.05	1.750±.10 mm	5.5±0.05 mm	4.5 mm	8.0±0.1 mm	4.0±0.1 mm	2.0±0.05 mm	0.4 mm	12.0 mm ± 0.3 mm

Contact Information

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