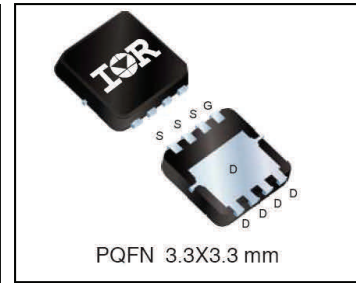
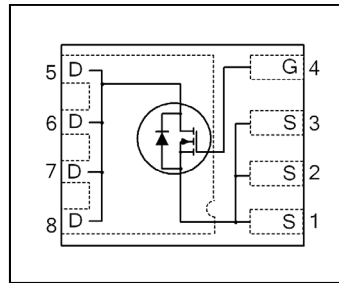


HEXFET® Power MOSFET

V_{DSS}	30	V
$R_{DS(on) \max}$ (@ $V_{GS} = 10V$)	12.4	mΩ
(@ $V_{GS} = 4.5V$)	17.9	
Qg (typical)	5.4	nC
I_D (@ $T_C = 25^\circ C$)	18 Ⓣ	A


Applications

- System/load switch,
- Charge or discharge switch for battery protection

Features

Low Thermal Resistance to PCB (< 5.0°C/W)
Low Profile (<1.05 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1, Consumer Qualification

 results in
⇒

Benefits

Enable better Thermal Dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHM8337PbF	PQFN 3.3mm x 3.3mm	Tape and Reel	4000	IRFHM8337TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	9.4	
I_{DM}	Pulsed Drain Current ①	94⑧	
$I_D @ T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	35⑥⑦	
$I_D @ T_{C(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	22⑥⑦	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Source Bonding Technology Limited)	18⑦	W
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑤	2.8	
$P_D @ T_{C(Bottom)} = 25^\circ C$	Power Dissipation ⑤	25	
	Linear Derating Factor ⑤	0.02	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑧ are on page 8

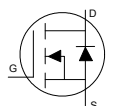
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	9.4	12.4	mΩ	V _{GS} = 10V, I _D = 12A ^③
		—	14.5	17.9		V _{GS} = 4.5V, I _D = 9.4A ^③
V _{GS(th)}	Gate Threshold Voltage	1.35	1.8	2.35	V	V _{DS} = V _{GS} , I _D = 25μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-6.2	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	μA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	17	—	—	S	V _{DS} = 15V, I _D = 9.4A
Q _g	Total Gate Charge	—	5.4	8.1	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 9.4A
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	1.1	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	0.7	—		
Q _{gd}	Gate-to-Drain Charge	—	2.2	—		
Q _{godr}	Gate Charge Overdrive	—	1.5	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	2.9	—		
Q _{oss}	Output Charge	—	3.8	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	2.0	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	9.0	—	ns	V _{DD} = 15V, V _{GS} = 4.5V ^③ I _D = 9.4A R _G = 1.3Ω
t _r	Rise Time	—	11	—		
t _{d(off)}	Turn-Off Delay Time	—	9.9	—		
t _f	Fall Time	—	5.6	—		
C _{iss}	Input Capacitance	—	755	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	171	—		
C _{rss}	Reverse Transfer Capacitance	—	83	—		

Avalanche Characteristics

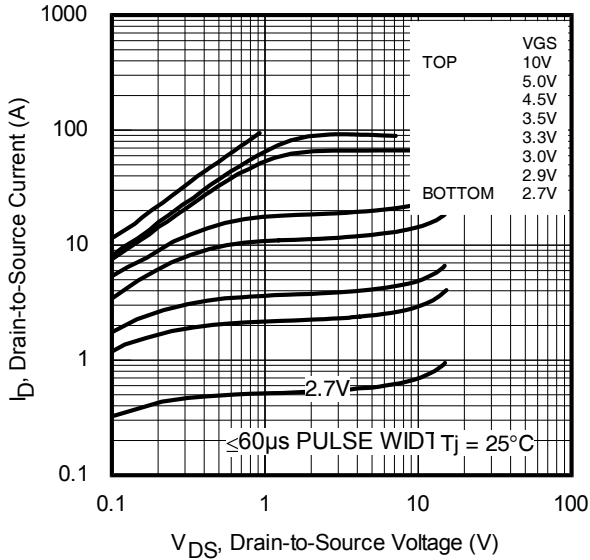
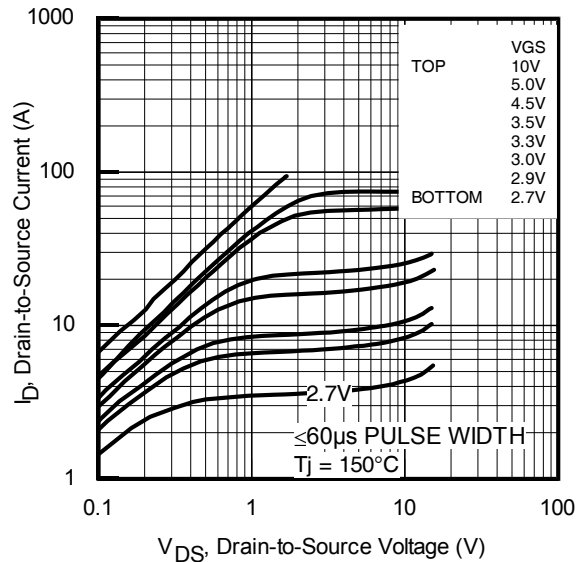
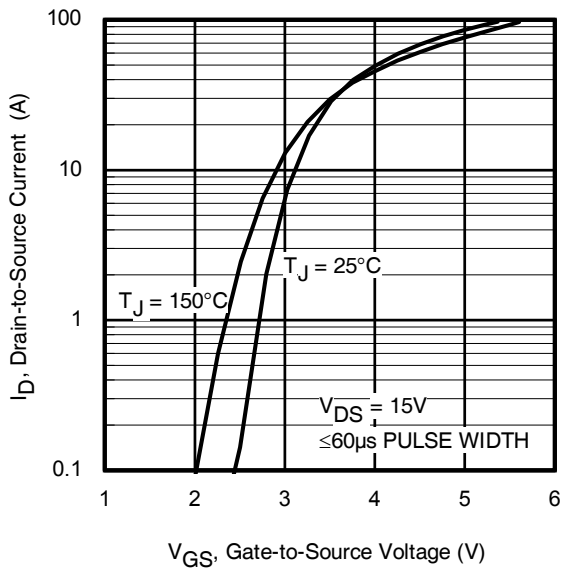
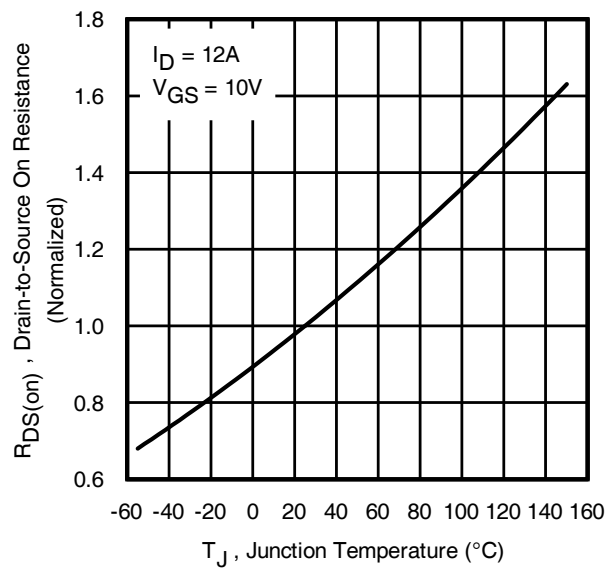
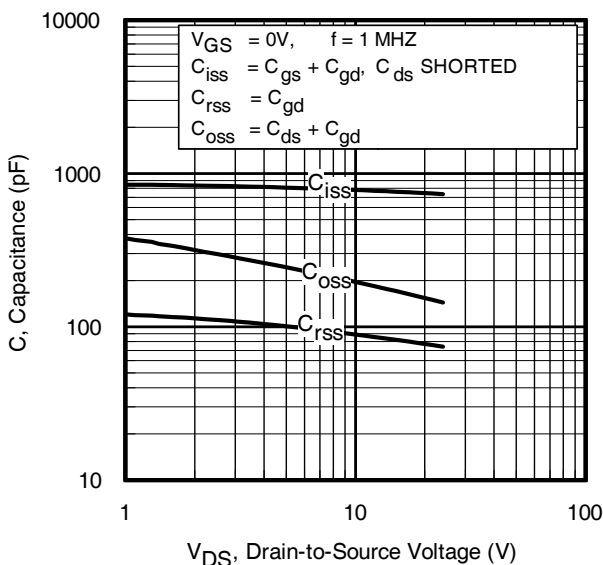
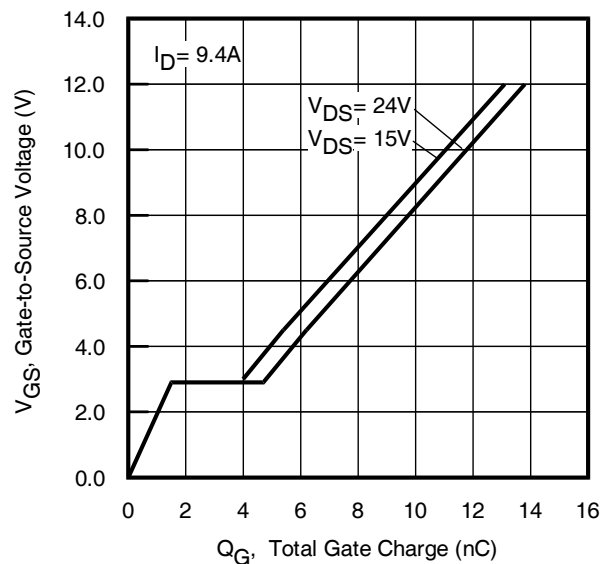
	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ^②	—	13	mJ

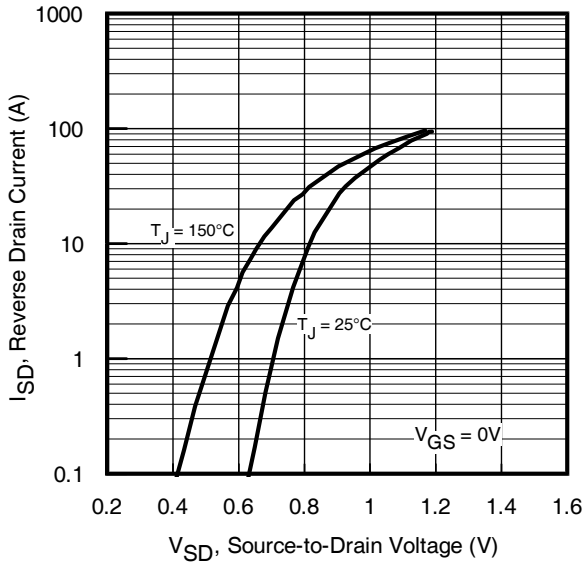
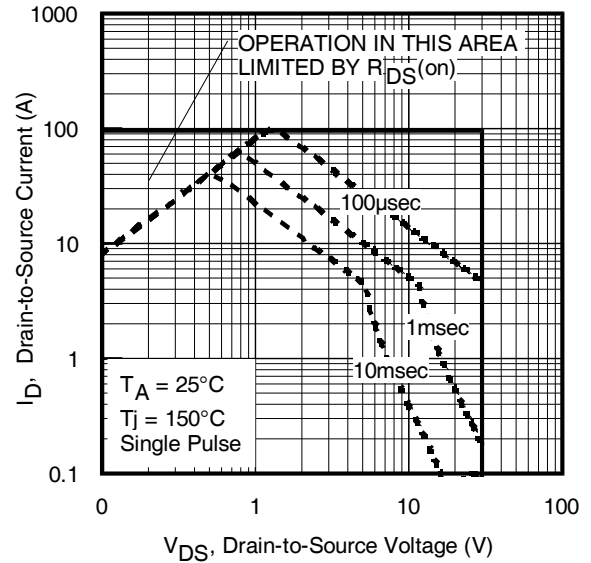
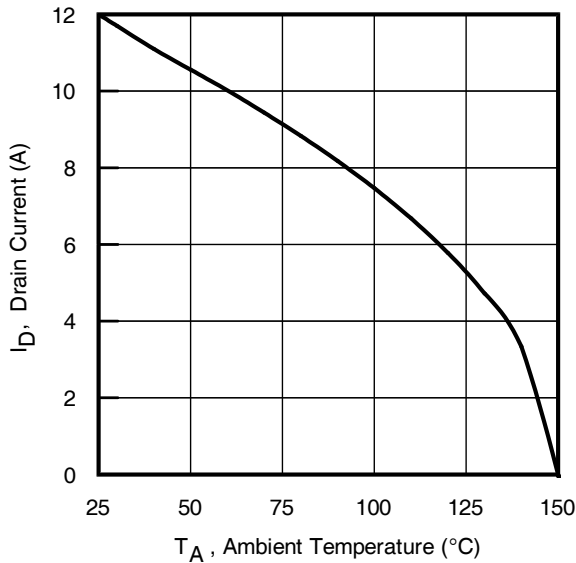
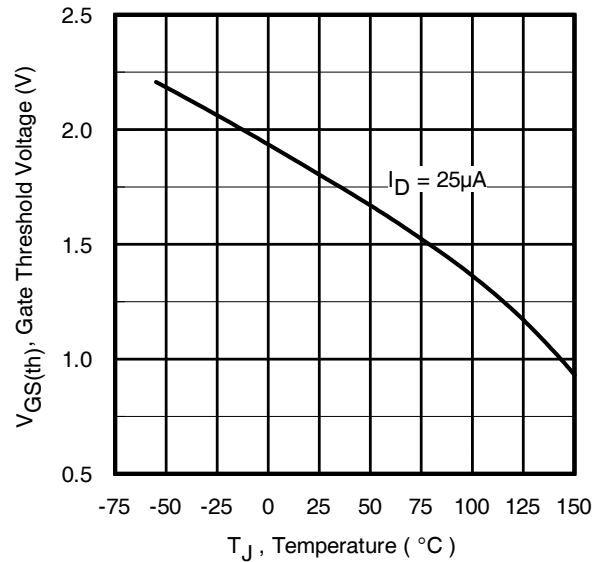
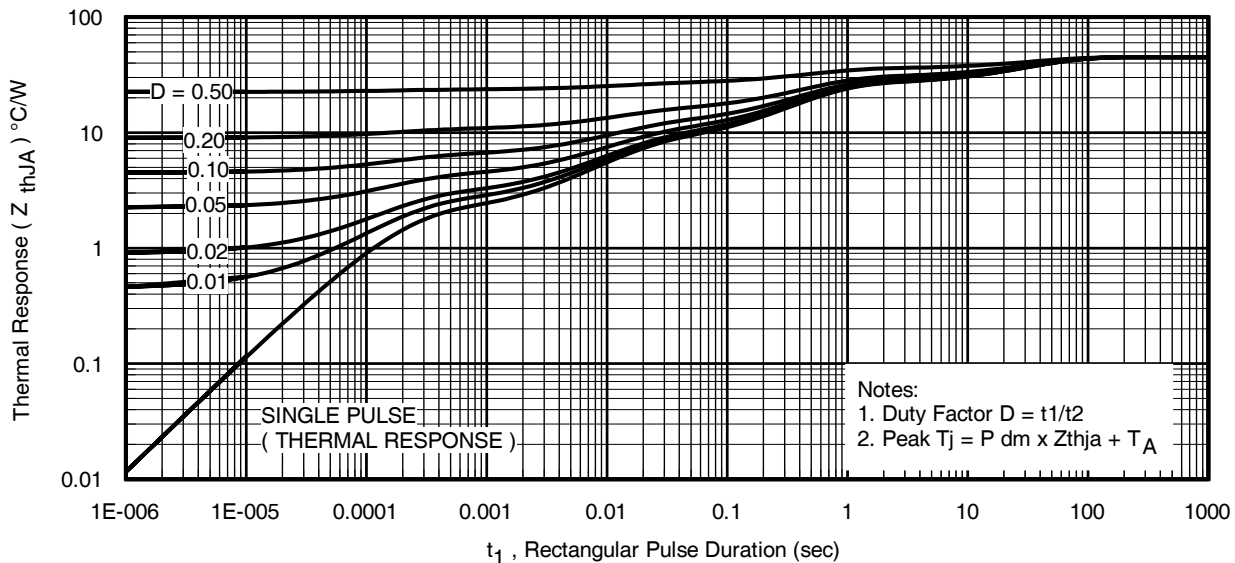
Diode Characteristics

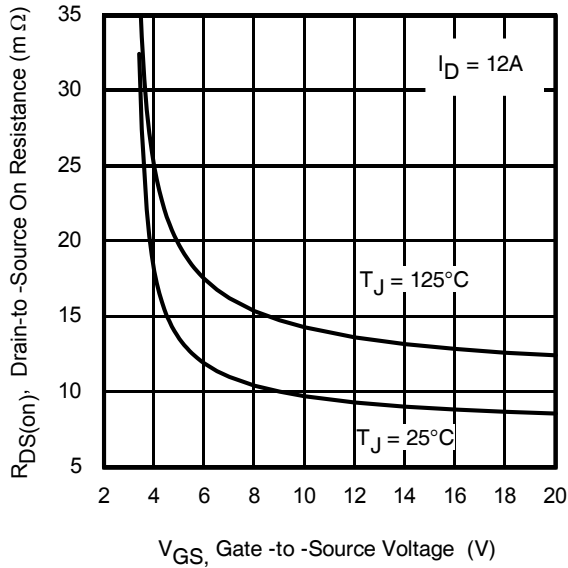
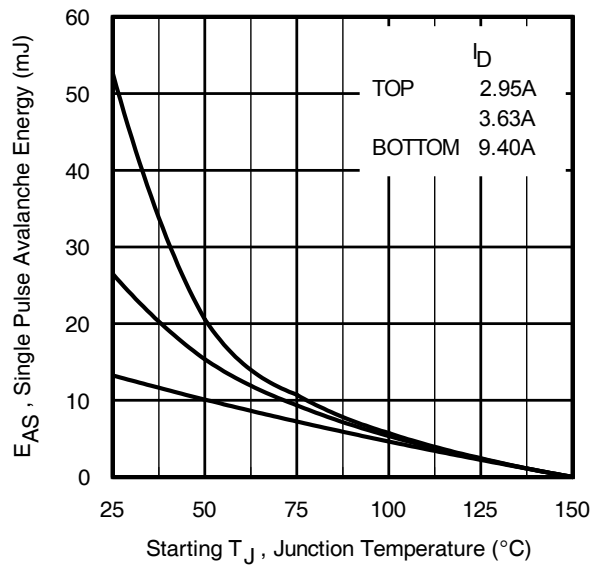
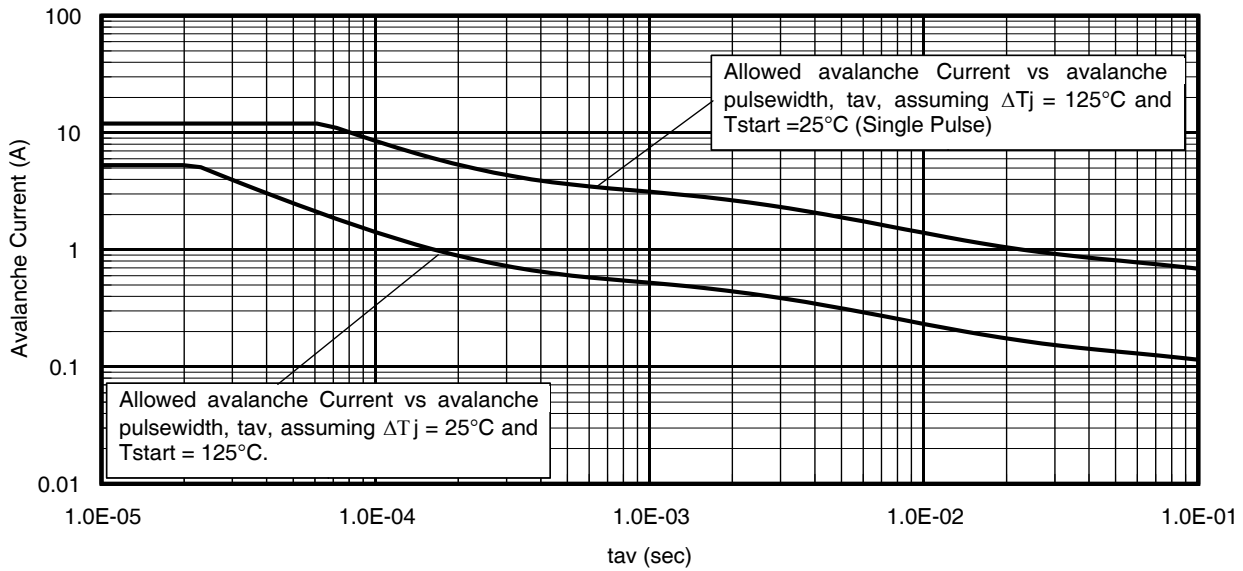
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	18 ^②	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	94 ^③		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 9.4A, V _{GS} = 0V ^③
t _{rr}	Reverse Recovery Time	—	20	30	ns	T _J = 25°C, I _F = 9.4A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	27	41	nC	di/dt = 200A/μs ^②

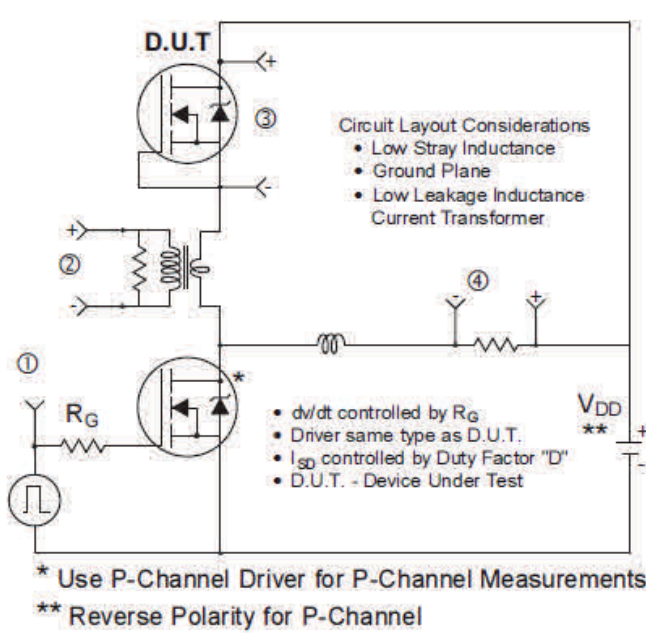
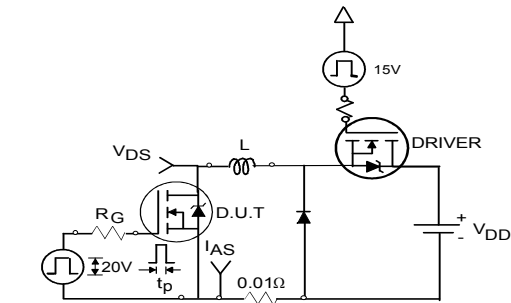
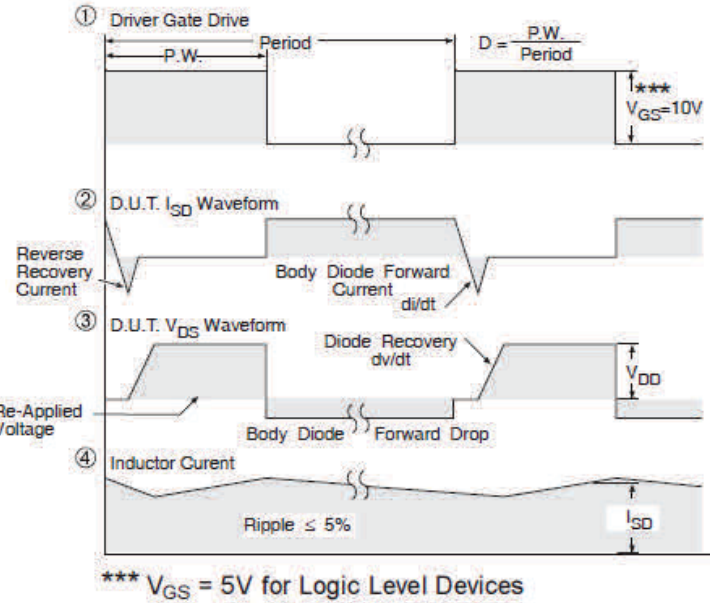
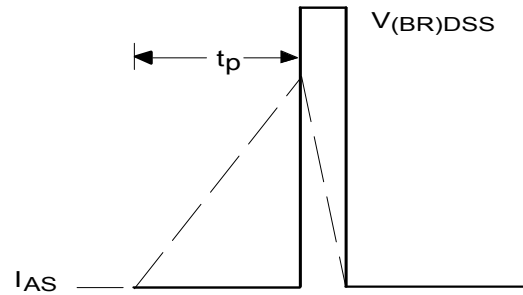
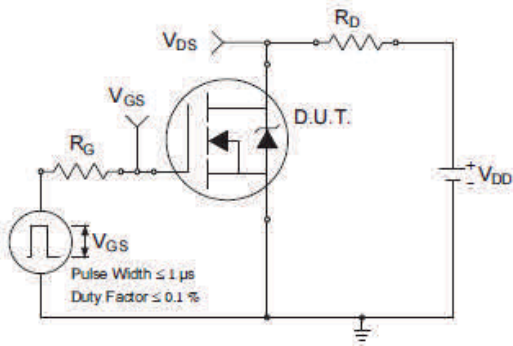
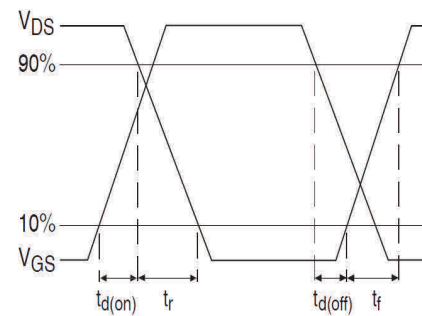
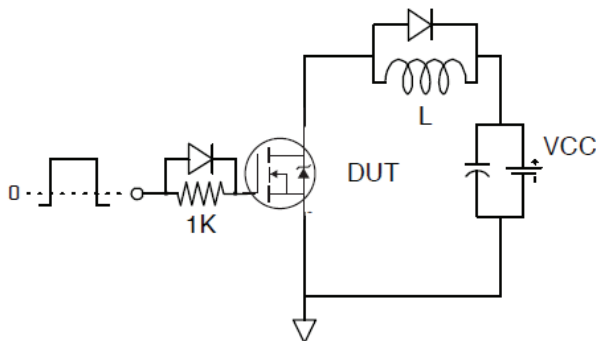
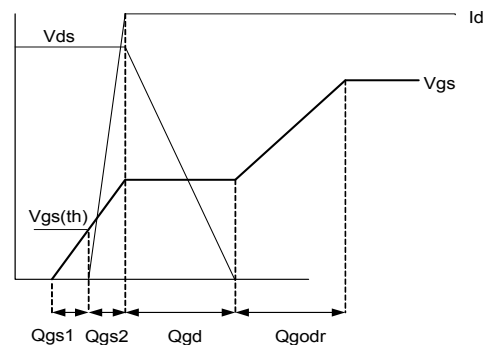
Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ^④	—	5.0	°C/W
R _{θJC} (Top)	Junction-to-Case ^④	—	50	
R _{θJA}	Junction-to-Ambient ^⑤	—	45	
R _{θJA} (<10s)	Junction-to-Ambient ^⑤	—	31	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Ambient Temperature

Fig 10. Threshold Voltage Vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14. Single avalanche event: pulse current vs. pulse width


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

Fig 16a. Unclamped Inductive Test Circuit

Fig 16b. Unclamped Inductive Waveforms

Fig 17a. Switching Time Test Circuit

Fig 17b. Switching Time Waveforms

Fig 18. Gate Charge Test Circuit

Fig 19. Gate Charge Waveform

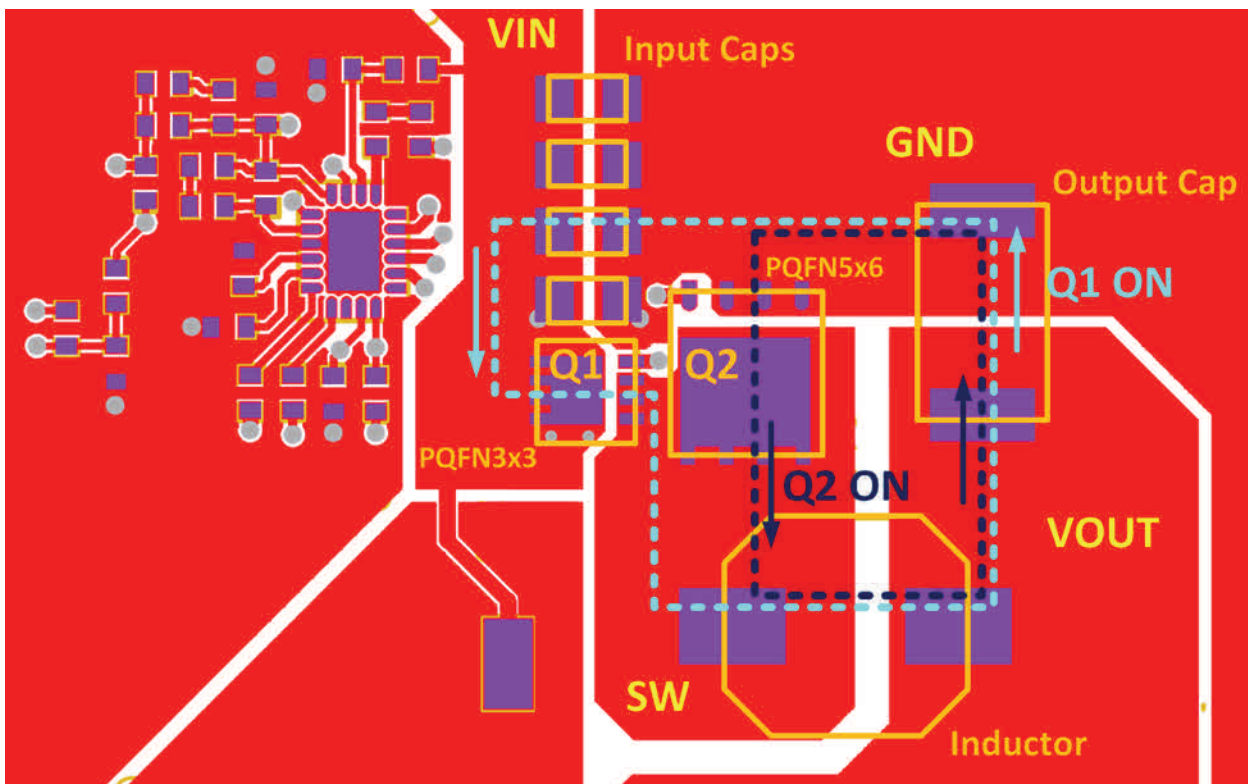
Placement and Layout Guidelines

The typical application topology for this product is the synchronous buck converter. These converters operate at high frequencies (typically around 400 kHz). During turn-on and turn-off switching cycles, the high di/dt currents circulating in the parasitic elements of the circuit induce high voltage ringing which may exceed the device rating and lead to undesirable effects. One of the major contributors to the increase in parasitics is the PCB power circuit inductance.

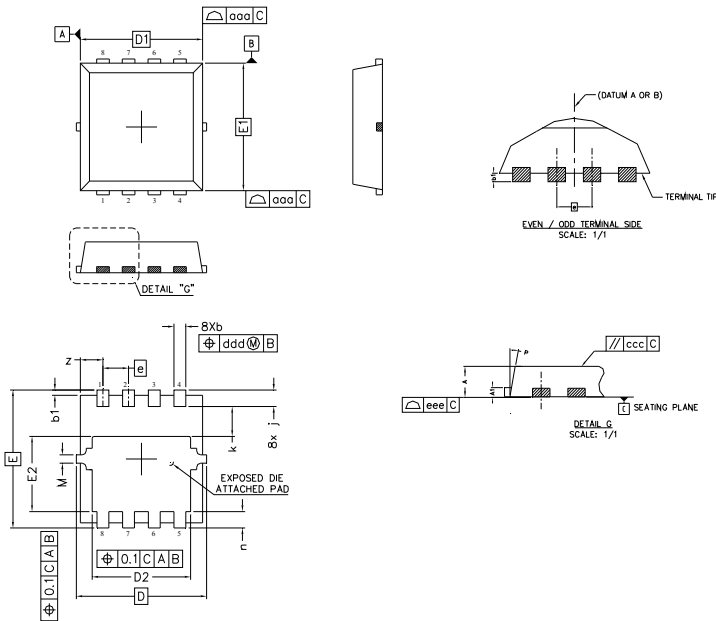
This section introduces a simple guideline that mitigates the effect of these parasitics on the performance of the circuit and provides reliable operation of the devices.

To reduce high frequency switching noise and the effects of Electromagnetic Interference (EMI) when the control MOSFET (Q1) is turned on, the layout shown in Figure 19 is recommended. The input bypass capacitors, control MOSFET and output capacitors are placed in a tight loop to minimize parasitic inductance which in turn lowers the amplitude of the switch node ringing, and minimizes exposure of the MOSFETs to repetitive avalanche conditions.

When the synchronous MOSFET (Q2) is turned on, high average DC current flows through the path indicated in Figure 19. Therefore, the Q2 turn-on path should be laid out with a tight loop and wide traces at both ends of the inductor to minimize loop resistance.

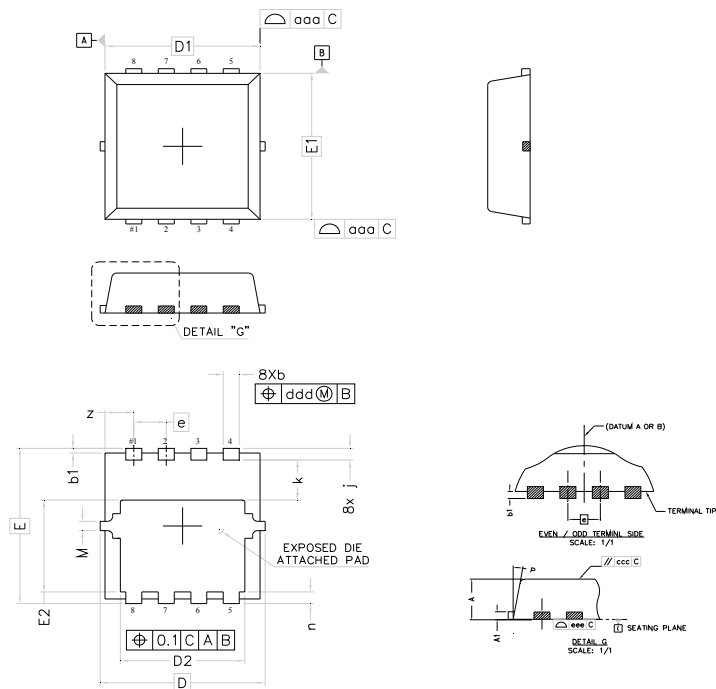


PQFN 3.3 x 3.3 Outline "C" Package Details



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	.0276	.0315
A1	0.10	0.25	.0039	.0098
b	0.25	0.35	.0098	.0138
b1	0.05	0.15	.0020	.0059
D	3.20	3.40	.1260	.1339
D1	3.00	3.20	.1181	.1260
D2	2.39	2.59	.0941	.1020
E	3.25	3.45	.1280	.1358
E1	3.00	3.20	.1181	.1260
E2	1.78	1.98	.0701	.0780
e	0.65 BSC		.0255 BSC	
j	0.30	0.50	.0118	.0197
k	0.59	0.79	.0232	.0311
n	0.30	0.50	.0118	.0197
M	0.03	0.23	.0012	.0091
P	10°	12°	10°	12°
z	0.50	0.70	.0197	.0276

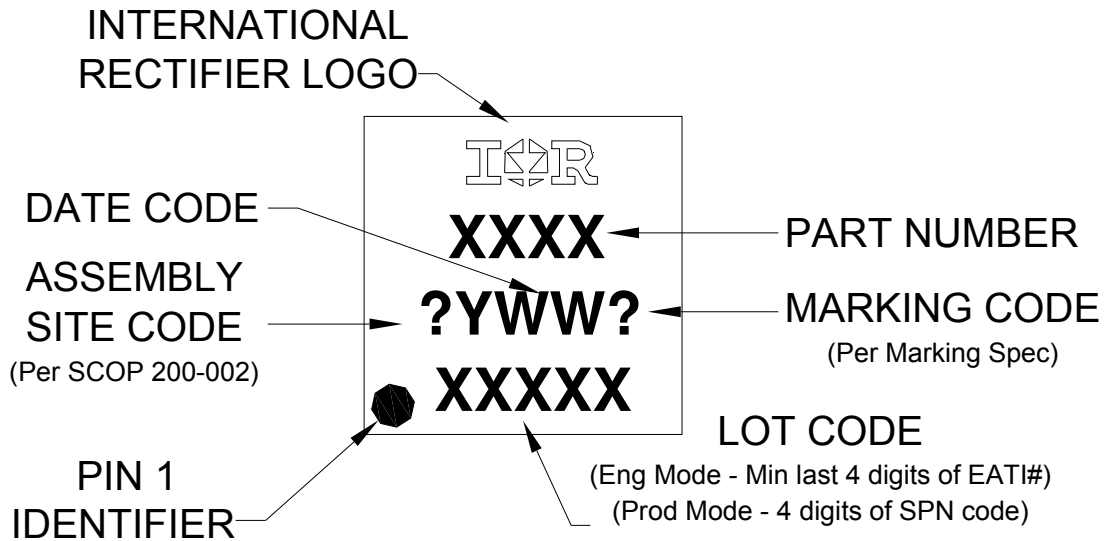
PQFN 3.3 x 3.3 Outline "G" Package Details



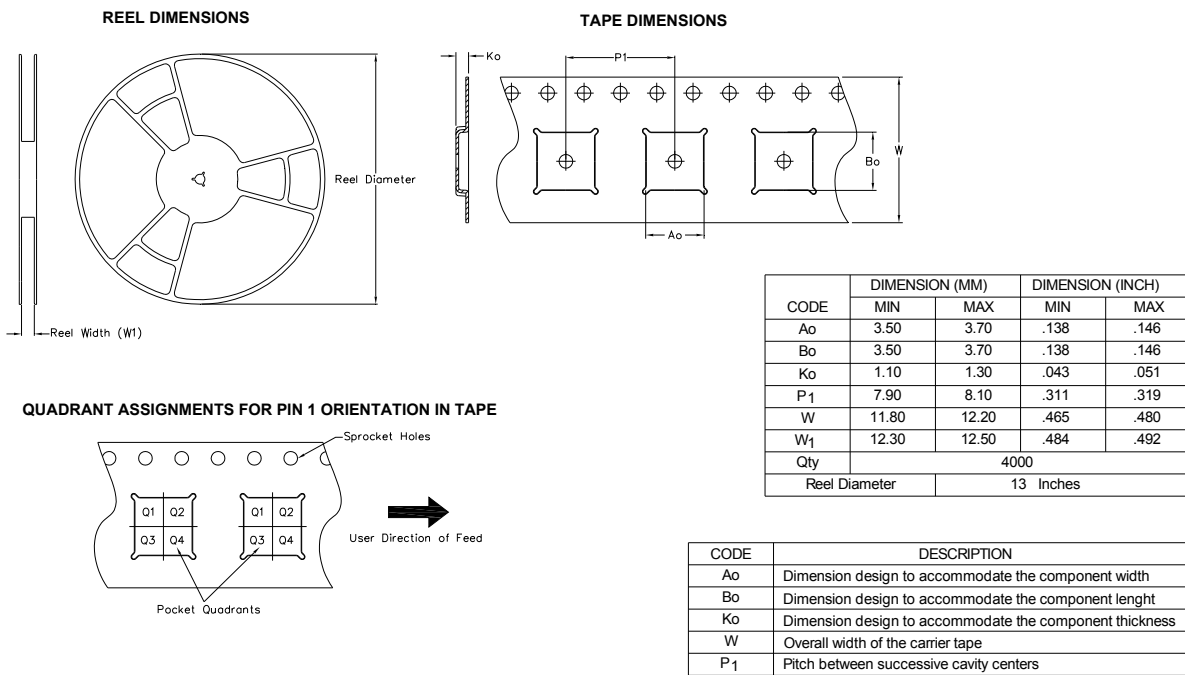
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	0.90	.0315	.0354
A1	0.12	0.22	.0047	.0086
b	0.22	0.42	.0087	.0165
b1	0.05	0.15	.0020	.0059
D	3.30 BSC		.1299 BSC	
D1	3.10 BSC		.1220 BSC	
D2	2.29	2.69	.0902	.1059
E	3.30 BSC		.1299 BSC	
E1	3.10 BSC		.1220 BSC	
E2	1.85	2.05	.0728	.0807
e	0.65 BSC		.0255 BSC	
j	0.15	0.35	.0059	.0137
k	0.75	0.95	.0295	.0374
n	0.15	0.35	.0059	.0137
M	NOM.	0.20	NOM.	.0078
P	9°	11°	9°	11°

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 3.3 x 3.3 Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN 3.3 x 3.3 Tape and Reel


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Consumer ^{††} (per JEDEC JESD47F guidelines)	
Moisture Sensitivity Level	PQFN 3.3mm x 3.3mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Higher qualification ratings may be available should the user have such requirements.
Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.297\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 9.4\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current limited to 18A by source bonding technology.
- ⑧ Pulse drain current is limited to 72A by source bonding technology.

Revision History

Date	Comments
6/5/2014	<ul style="list-style-type: none"> • Updated schematic on page 1 • Updated part marking on page 8 • Updated tape and reel on page 9
7/1/2014	<ul style="list-style-type: none"> • Remove "SAWN" package outline on page 8.
02/23/2016	<ul style="list-style-type: none"> • Updated datasheet with corporate template • Updated package outline to reflect the PCN # (241-PCN30-Public) for "Option C" and "Option G" on page 8.

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