SocketSLIC®

Analog Telephony Interface Module

Model MTIFM

Developer Guide

MultiTech® Systems

SocketSLIC® Developer Guide
Analog Telephony Interface Module
Model MTIFM
PN S000288D, Version D

Copyright

Revisions

Revision	*Date*	*Description*
A	03/17/03	First release.
B	06/15/07	Updated tech support listing and repair information.
C	03/26/09	Added the mechanical drawing, block diagram, developer board schematics, and Tip and Ring drawing. Changed the FCC compliance to Class A. Updated the requirement for a Poly-Switch. Updated recommended components. Updated Ring voltage levels and Telecom voltage levels. Added a Regulatory and Compliance appendix. Added a list of the Developer Kit contents. Removed references to EEPROM. Added a table of SPI Access Restrictions.
D	03/29/10	Add new Mechanical Drawing.

Trademarks

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Warranty

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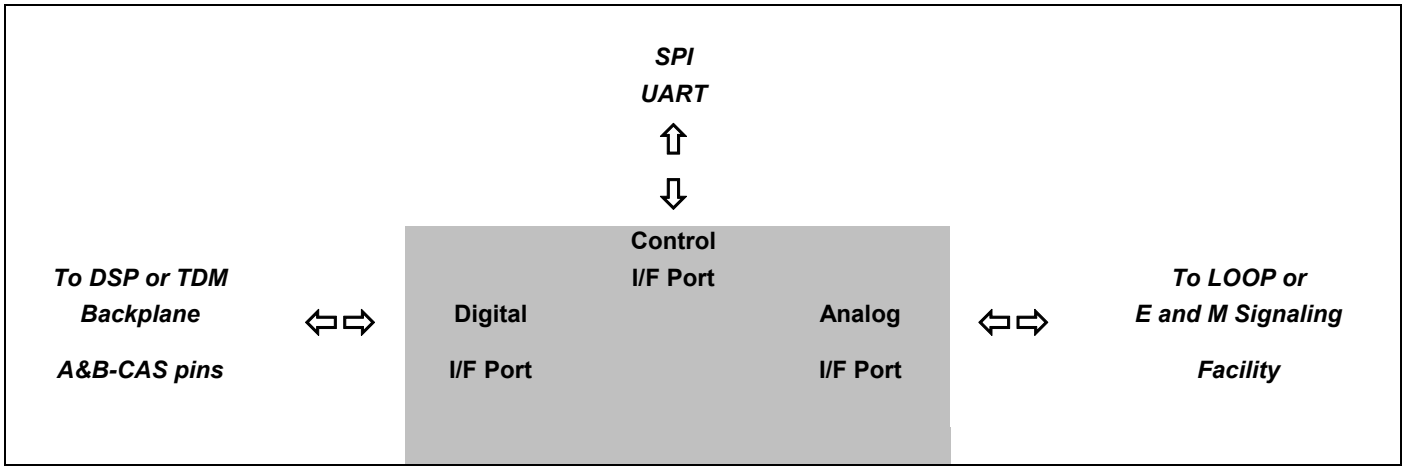
Chapter 1 – Introduction

Product Description

The SocketSLIC® (SLIC: Subscriber Line Interface Circuit) interface module is a complete, single circuit, full featured, flexible, isolated and programmable, ready to integrate analog-to-PCM interface. It allows the user to choose the appropriate telephony interface when the system is configured either in manufacturing or in the field. This flexibility adds convenience, low cost and quick time to market to designing modern communication systems or updating existing telephony systems. The SocketSLIC interface module takes care of the many standard analog interfaces allowing the designer to focus on the digital design.

The SocketSLIC consists of three module Interface (I/F) ports:

- **Analog**
- **Digital**
- **Control**



Field Programmable – Telephony interface Module

The analog interface port connects to analog telephony "Loop", "E and M", or "Dry" signaling facilities. The digital interface port connects to a TDM backplane with A/B-bit signaling access for digital telephony interfaces. The control interface port connects to a synchronous Serial Peripheral Interface (SPI) or serial Universal Asynchronous Receiver and Transmitter (UART) interface. These three module interface ports allow the designer and user to choose the appropriate telephony interface when the system is configured either in manufacturing or in the field. This flexibility adds convenience, low cost, and quick time to market to designing modern communication systems or updating existing telephony systems. **MTIFM** takes care of the many interfaces allowing the designer to focus on other design aspects of the project.

The Field Programmable Telephony interface Module **MTIFM** performs the functions of the following devices:

- **Data Access Arrangements** (DAA)
- **Subscriber Line Interface Circuits** (SLIC)
- **Analog Station Cards/Trunk Line Cards** (ASC/TLC)

The SocketSLIC converts analog payload like voice, data, and Fax to digital Pulse Code Modulation (PCM) and converts analog telephony signaling to digital Channel Associated Signaling (CAS). The module is transparent for the following signals, tones, and modes:

- **Addressing Signals** (Dial Pulse, DTMF, MF, MF-R1, MF-R2, MFC)
- **Call Progress Tones** (Dial Tone, Ring Back Tone, etc.)
- **Start-Modes** (Wink-Start, Immediate-Start, Delay-Dial)
- **Supervisory Signals** (Seizure, Flash, Wink, Disconnect)

Features

Programmable

- Answer Delay Timing
- CAS Bit Signaling Manipulations
- Hybrid Balances
- TDM Bit Clocks
- TDM Companding Modes
- TDM Framing Modes
- TDM Loopback Modes
- Receive Gains
- Ring Frequencies
- Ring Patterns
- Ring Voltages
- Special Functions
- Telecom Voltages
- Telephony Interfaces
- Time-slot Assignments
- Transmit Gains
- Wink Delay Timing

Status and Diagnostics Capability

- Telephony Lead Wiring Error Status
- TDM Loopback Function
- Internal Reset Counter

Supports

- Loop-Start, Ground-Start and Direct-Inward-Dialing (DID)
- Supports FXO, FXS, DPO, DPT, E&M, PLR, ETO, TO
- E&M Type I, II, III, IV, V Signaling
- Two-Wire and Four-Wire Transmissions
- Loop Disconnect Signals
- Caller ID and Other Class Services

Benefits

- Acts as a Universal Analog Trunk/Line Card
- AutoWink™ Signaling
- Caller ID Processing
- CMOS/TTL Compatible Inputs And Outputs
- Dielectric Barrier separating Digital (logic) and Analog (telephony) Ports
- Direct A and B Signaling Bit Access Pins
- Fast Digital Ring Detection Algorithm
- Flash Memory for Firmware Updates
- Fully Electrically Isolated Analog Telephony Interface
- Global Homologation
- Flash-to-Answer Supervision
- In-System Programmability Supported
- Internal 2-4 Wire Conversion
- Low Noise Design
- Low Power Consumption
- Low RFI Emissions
- No DIP Switches. No Jumpers (None on the SocketSLIC. The Developer Board has Dip Switches)
- On-Board Ring Generator
- On-Board Telecom Battery Power Supply
- Originate Loop-Disconnect Signal
- Pass Loop-Disconnect Signals
- PC Operating System Independent
- Telephone Trunk/Line Status Reporting
- Serial Peripheral Interface (SPI)
- Short Circuit Tolerant Analog Telephony Port Terminals
- Single Voltage Power Supply Input
- Small Dual-In-Line Package Footprint
- Transparent Interface Conversion Operation
- Universal Asynchronous Receiver and Transmitter (UART) Interface
- Works Without the need for Constant Host Processor Supervision

Safety

Handling Precautions

Proper care must be taken when handling and installing this product:

1. Observe the absolute maximum ratings
2. Avoid exposure to electrostatic discharge (ESD)
3. Prevent the application of reverse polarity to the power pins
4. Provide filtered power to the module
5. Never plug or unplug this product while powered

Electrostatic Discharge (ESD) Caution

Static electricity can destroy some sensitive components on this product. To prevent damage to the product due to an electrostatic discharge, always connect yourself to ground using a ground strap before touching the product. Handle product only by the edges and always store the product in anti static bags.

Safety Instructions

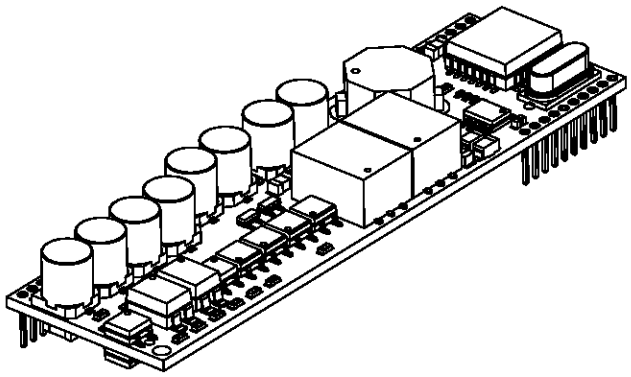
When using your telephone equipment, basic safety precautions should always be followed to reduce the risk of fire, electric shock, and injury to persons, including the following:

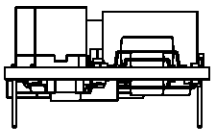
1. Read and understand all instructions
2. Follow all warnings and instructions
3. Unplug the equipment from the telecom connector before cleaning
4. Use a damp cloth for cleaning
5. Do not use liquid cleansers or aerosol cleaners
6. Do not use this product near water
7. When installing this product into your system, please make sure that the earth ground pin is securely connected to the systems chassis or telecom reference conductor terminal and that the system is plugged into a grounded three-prong outlet. Incorrect grounding can result in harmful or fatal electrical shock or component damage.

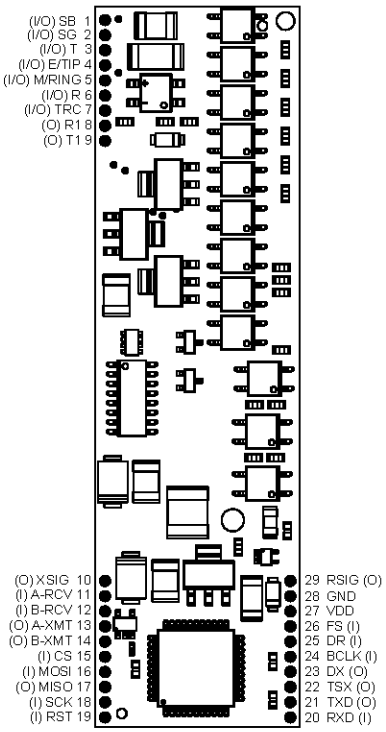
Telecom Safety Warning

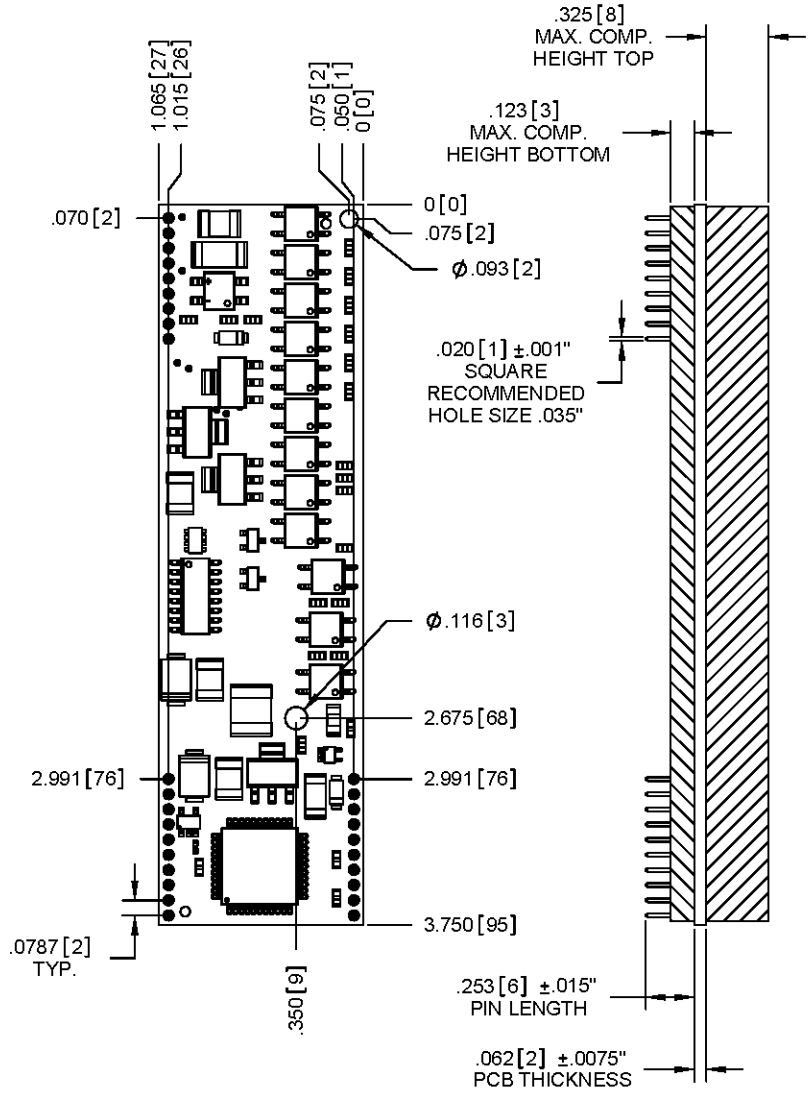
1. Never install telephone wiring during a lightning storm.
2. Never install a telephone jack in wet locations unless the jack is specifically designed for wet locations.
3. This product is to be used with UL and cUL listed computers.
4. Never touch uninsulated telephone wires or terminals unless the telephone line has been disconnected at the network interface.
5. Use caution when installing or modifying telephone lines.
6. Avoid using a telephone during an electrical storm. There may be a remote risk of electrical shock from lightning.
7. Do not use a telephone in the vicinity of a gas leak.
8. To reduce the risk of fire, use only 26 AWG or larger telecommunication line cord.
9. This product must be disconnected from its power source and telephone network interface when servicing.

SocketSLIC Mechanical Drawing









NOTE: DIMENSIONS IN In [mm]

Pin Description

Pin	Symbol	Type	Name/Description
1	SB	I/O	**SIGNAL BATTERY LEAD.** This pin is the signal-battery lead for type II, III, and IV interface arrangements for 2-wire and 4-wire E and M signaling facilities. This is not a power pin!
2	SG	I/O	**SIGNAL GROUND LEAD.** This pin is the signal-ground lead for type II, III, and IV interface arrangements for 2-wire and 4-wire E and M signaling facilities. This is not a power pin!
3	T	I/O	**T-LEAD.** This pin is the T-lead for 2-wire E&M transmit and receive talk-path and 4-wire E&M receive talk-path only.
4	E/TIP	I/O	**E-LEAD.** This pin is the E-lead in 2-wire and 4-wire E and M signaling facilities. This pin is also the Tip-lead for all 2-wire LOOP signaling facilities.
5	M/RING	I/O	**M-LEAD.** This pin is the M-lead in 2- wire and 4-wire E and M signaling facilities. This pin is also the Ring-Lead for all 2-wire LOOP signaling facilities.
6	R	I/O	**R-LEAD.** This pin is the R-lead for 2-wire E&M transmit and receive talk-path and 4-wire E&M receive talk-path only.
7	TRC	I/O	**TELECOM REFERENCE CONDUCTOR.** This pin is the telecom ground lead that connects the module's internal power supply to an external earth ground.
8	R1	O	**R1-LEAD.** This output pin is the R1-lead for the 4-wire E&M transmit talk-path only.
9	T1	O	**T1-LEAD.** This output pin is the T1-lead for the 4-wire E&M transmit talk-path only.
DIELECTRIC ISOLATION BARRIER			
10	XSIG	O	**TRANSMIT SIGNALING.** This output pin indicates the incoming analog signaling state (active high).
11	A-RCV	I	**A RECEIVE CAS BIT.** This input pin receives bit A for channel associated signaling.
12	B-RCV	I	**B RECEIVE CAS BIT.** This input pin receives bit B for channel associated signaling.
13	A-XMT	O	**A TRANSMIT CAS BIT.** This output pin transmits bit A for channel associated signaling.
14	B-XMT	O	**B TRANSMIT CAS BIT.** This output pin transmits bit B for channel associated signaling.
15	CS	I	**CHIP SELECT.** This input pin receives the chip select signal for the SPI and UART ports
16	MOSI	I	**SPI SLAVE INPUT.** This input pin receives the input data for the SPI port.
17	MISO	O	**SPI SLAVE OUTPUT.** This output pin transmits the output data for the SPI port.
18	SCK	I	**SPI CLOCK.** This input pin receives the shift clock for the SPI port.
19	RST	I	**RESET.** This input pin must be pulled low for normal operation. When pulled momentarily high for at least 1us, all programmable registers in the device are reset to the states specified under power-up initialization.
20	RXD	I	**RECEIVE DATA.** This input pin receives the input data for the UART.
21	TXD	O	**TRANSMIT DATA.** This output pin transmits the output data for the UART.
22	TSX	O	**TRANSMIT TIME-SLOT.** This open drain output pin is floating in a high-impedance state. When a time-slot is active on the DX output, the TSX output pulls low to indicate a valid time-slot and to enable a back-plane line driver.
23	DX	O	**TRANSMIT TDM.** This output pin remains in the high impedance state except during the assigned time-slot, when the transmit TDM data byte is shifted out on the rising edges of BCLK.
24	BCLK	I	**BIT CLOCK.** This input pin shifts TDM data into and out of the DR and DX pins. It must be 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz.
25	DR	I	**RECEIVE TDM.** This input pin is inactive except during the assigned time-slot when the receive TDM data byte is shifted in on the falling edges of BCLK.
26	FS	I	**FRAME-SYNC.** This input pin receives a pulse or square waveform with an 8kHz repetition rate is applied to it. This waveform defines the start of the time-slot assigned to this module (in non-delayed frame mode), or the start of the frame (in delayed frame mode using the internal time-slot assignment counter).
27	VDD	-	**LOGIC POWER.** This pin connects to the +5 Vdc power supply
28	GND	-	**LOGIC GROUND.** This pin connects to the +5 Vdc power supply return reference.
29	RSIG	O	**RECEIVE SIGNALING.** This output pin indicates the outgoing analog signaling state (active high).

Chapter 2 – Functions and Ports

Telephony Functions

The SocketSLIC provides the following standard **BORSCHT** telephony functions:

Battery Feed

- Battery Voltage Generation for powering the lines or trunks
- Loop Current Detection for recognizing line or trunk seizures

Over-voltage Protection

- External fuses (one-time fuse or polyfuse) for Current Limitation are required.
- External Transient Voltage Suppressors (TVS or MOV) for Overvoltage Protection are required.

Ringing

- Ring Detection
- Ring Generation

Supervision

- Normal Battery / Reverse Battery
- On-Hook / Off-Hook

Codec

- Analog-to-Digital (A/D) Conversion with mu-Law Or A-Law companding
- Digital-to-Analog (D/A) Conversion with mu-Law Or A-Law de-companding

Hybrid

- Programmable internal hybrid balance network
- 2-wire To 4-wire circuit conversion

Testing

- Internal loopback modes for the digital TDM stream
- An external relay may be required to provide test access.

Analog Interface Port

The **SocketSLIC** analog interface port can be configured to support the basic analog Public Switched Telephone Network (PSTN) interfaces. Each PSTN interface consists of two sides. One interface port represents one side of the interface. Start-mode and addressing information are passed transparently between the analog and digital ports.

The SocketSLIC supports the following analog interfaces:

- Interface with Loop-Start Supervision (LS)
- Interface with Reverse-Battery Supervision (RB)
- Interface with Ground-Start Supervision (GS)
- Interface with Loop-Reverse-Battery Supervision (LRBS)
- Interface with E and M Lead Supervision (E and M)
- Interface with no Supervision (NoS)

The SocketSLIC supports the following analog interface ports:

- Foreign Exchange Office (FXO)
- Foreign Exchange Subscriber (FXS)
- Dial Pulse Originating (DPO)
- Dial Pulse Terminating (DPT)
- E and M (E&M)
- Pulse Link Repeater (PLR)
- Transmission Only (TO)
- Equalized Transmission Only (ETO)

The SocketSLIC supports the following transmission types:

- Two-Wire (2-W)
- Four-Wire (4-W)

The SocketSLIC supports the following E and M signaling types:

- Type I (I)
- Type II (II)
- Type III (III)
- Type IV (IV)
- Type V (V)

The SocketSLIC supports the following telecom parameter adjustments:

- Transmit Gain (TG)
- Receive Gain (RG)
- Telecom Voltage (TV)
- Ring Voltage (RV)
- Ring Frequency (RF)
- Ring Pattern (RP)
- Answer Delay Timing (ADT)
- Wink Delay Timing (WDT)
- Lower Ring Frequency Detection Limit (LRFDL)
- Upper Ring Frequency Detection Limit (URFDL)

Digital Interface Port

The **SocketSLIC** contains a programmable interface for the transmission and reception of digital Time Division Multiplex (TDM). TDM data is shifted into the decoders TDM receive register via the DR pin during the selected time-slot on the falling edges of BCLK. The FS inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They can have any duration from a single cycle of BCLK high to one BCLK low. Two different relationships can be established between the frame-sync inputs and the actual time-slots on the TDM buses by setting bit 3 in the Codec Control Register (CCR). Non-delayed data mode is similar to long-frame timing of other TDM line cards for which time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use delayed-data mode (short-frame timing) in which the FS input must be high at least a half-cycle of BCLK earlier than the time-slot. The time-slot assignment circuit on the module can only be used with delayed-data timing.

The time-slot assignment capability of the module conforms to the Lucent Technologies Concentration Highway Interface (CHI). The beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal time-slot assignment counters.

During each assigned transmit time-slot, the selected DX output shifts the time division multiplex data out from the TDM transmit register on the rising edges of BCLK. TSX also pulls low for the first 7.5 bit times of the time-slot to control the high impedance state enable of a back-plane line driver. Serial TDM data is shifted into the selected DR input during each assignment of the receive time-slot on the falling edges of BCLK. The clock rates of 1.536 MHz, 2.048 MHz, and 4.096 MHz support 24, 32, or 64 time slots respectively.

The SocketSLIC supports the following TDM stream settings:

- Bit Clock (1.536 MHz, 2.048 MHz, 4.096 MHz)
- Companding Law (u-255 Law, A-Law)
- Frame Synchronization (delayed framing, non-delayed framing)
- Loopback Mode (analog and digital)

The SocketSLIC supports the following Channel Associated Signaling controls:

- CAS bit Status (hardware pin access or register read access)
- CAS bit Manipulation (invert & swap)
- CAS bit Declaration (force a specific logic level)

Control Interface Port

Control information is written into or read back from the module's registers either via the synchronous SPI or asynchronous UART communication.

The user can change the user accessible registers as required by port operation. The user-selected values are immediately executed after writing to the register. The module will revert to the default settings after subsequent resets or power ups. The desired modes for all programmable functions can be initialized via the SPI or UART interfaces.

The control interface port allows access to the following module functions:

- Configuration
- Communication
- Programming

Configuration and communication is accomplished through the following module pin connections:

<**TXD**>	UART transmit data output from module
<**RXD**>	UART receive date input to module
<**CSS**>	SPI Chip Select input to module
<**SCK**>	SPI Shift Clock input to module
<**MOSI**>	SPI Master Output/Slave Input to module
<**MISO**>	SPI Master Input/Slave Output from module

UART Operation

The Universal Asynchronous Receiver and Transmitter (UART) provide serial communication access to the module. Asynchronous communication is very common because of the wide spread use of modems. Asynchronous communication follows a defined method or protocol. ASCII characters are transmitted at TTL level into the module with a fixed baud rate of 19.2kbps (transmission speed). The UART consists of receive data input (RXD), transmit data output (TXD) and chip select input. The host may start sending ASCII data 1 ms after asserting the chip select input.

Baud Rate: 19.2 kbps
Data Bits: 8
Parity Bit: none
Stop Bit: 1
Maximum Character Read/Write: 4 (2 x 2 Byte Nibbles)
Minimum Character Read/Write: 2 (1 x 2 Byte Nibbles)
Transmit Data Pin: TXD
Receive Data Pin: RXD
Module Chip Select Pin: CS
Chip Select "warm-up": 1 ms

Example

The following is an example of how to set the Telecom Voltage to approximately 60Vdc using the UART interface. Typing/sending 2C, the register address for TVR, the serial port transmits the ASCII characters of 2C into the module. The module converts the ASCII character back to 2C hexadecimal. Typing/sending 0D, the data byte for 60Vdc, the serial port transmits the ASCII characters of 0D into the module. Note that the ASCII characters for the module must be capitalized.

2 – First register address byte nibble ASCII character
C – Second register address byte nibble ASCII character
0 – First register data byte nibble ASCII character
D – Second register data byte nibble ASCII character

Create a Commented Text File

Below is a method of creating a commented text file for configuring the module. The raw text file can be down loaded directly into the module. The module will only accept the following hexadecimal character set (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F). Note that the module only accepts capitalized letters from a through f.

This way the characters to the right of the semicolon are intended for the module configuration and the characters to the left of the semicolon are intended as a comment line.

```
60    ; read module version number
2002  ; set restore factory defaults
2806  ; set port to fxs-gs
2F0C  ; set enable autowink and enable flash-to-answer
3983  ; set rcv timeslot four
3A87  ; set xmt timeslot eight
```

SPI Operation

The SPI consists of the Serial Clock (SCK), the Master Output/Slave Input (MOSI) and Master Input/Slave Output (MISO), and the Chip Select input (CS). The module is configured as the SPI slave.

To shift control data into the module, SCK must be pulsed high eight times while CS is low. Data on the MOSI input is shifted into the serial input register on the falling edge of each SCK pulse. Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the MISO/TXD and MOSI/RXD pins. After all data is shifted in, the contents of the input shift register are decoded and can indicate that a second byte can either be defined by a second byte-wide CS pulse or can follow the first contiguously. It is not mandatory for CS to return high between the first and second control bytes.

At the end of the eighth SCK pulse in the second control byte, the data is loaded into the appropriate programmable register. CS can remain low continuously when programming successive registers, if desired. However, CS should be set high when no data transfers are in progress.

To read back data or status information from the module, the first byte of the appropriate instruction is strobed in during the first CS pulse. CS must then be taken low for a further eight SCK cycles, during which the data is shifted onto the MISO pin on the rising edges of SCK. When CS is high, the MISO pin is in the high-impedance state, enabling the MISO pins of many devices to be multiplexed together.

Serial Synchronous Communication Access

The SPI provides serial synchronous communication access to the module.

Maximum SPI Clock Speed:	256kHz
Minimum SPI Byte Spacing:	740µs
Transmit Data Pin:	MISO
Receive Data Pin:	MOSI
Serial Clock Pin:	SCK
Module Chip Select Pin:	CS

SPI Access Restrictions

Following a read command, give at least 740µs before the next access.

Following a write command, give at least 2.7ms before the next access.

Following a factory default command, give at least 100ms.

When doing a two byte read or write command, give 740µs between the register and the value read or written.

Example

The following is an example of how to set the Telecom Voltage to approximately 60Vdc using the SPI interface. This is accomplished by writing a 0x0D to the Telecom Voltage Register (TVR) which is located at register address 0x2C:

1st Byte	2C	register address byte
2nd Byte	0D	register data byte

More Serial Peripheral Interface Information

The control interface to the SocketSLIC is a 4-wire synchronous interface modeled after commonly available micro-controller and serial peripheral devices. The interface consists of a clock (SCK), chip select (SCS), serial data input (MOSI) and serial data output (MISO). Data is transferred a bite at time with each register access consisting of a pair of byte transfers.

The first byte of the pair is the command/address byte. The MSB of this byte indicates register read when 1 and a register write when 0. The remaining seven bits of the command/address byte indicate the address of the register to be accessed. The second byte of the pair is the data byte. During a read operation, the MISO becomes active and the 8-bit contents of the register are driven out MSB first. The MISO will be high impedance on either the falling edge of SCLK following the LSB, or the rising of CS whichever comes first. MOSI is a "do not care" during the data portion of read operations. During write operations, data is driven into the SocketSLIC via the MOSI pin MSB first. The MISO pin will remain in the “High Impedance State” during write operations. Data always transitions on the rising edge. The clock should return to a logic high when no transfer is in progress. There are a number of variations of usage on this four-wire interface:

Special Functions

All special functions are based on SocketSLIC proprietary processing methods and can be selected through the Special Function Register (SFR).

Caller ID Processing

Caller ID processing (CID) applies to FXO-LS and FXS-LS ports only. The user must select the CID function when the attached telephone equipment is capable of originating or terminating caller ID signals. When selected, the FXS-LS or FXO-LS audio talk-path is enabled during non-ring burst periods for transmission of the caller ID information. The caller ID signal passes through the FXS-LS configuration from the digital module side to the analog module side. The caller ID signal passes through the FXO-LS configuration from the analog module side to the digital module side.

Pass Loop Disconnect

Pass Loop Disconnect operation (PLD) applies to the FXO-LS and FXS-LS port configurations. The user must select the PLD function when the attached telephone equipment is capable of originating or terminating loop-disconnect signals. When selected, the XMT CAS bit that indicates ringing also indicates the remote back to on-hook condition while the local connected equipment is still in the off-hook condition. The loop disconnect signal eliminates possible locked up trunk conditions between FXO-LS and FXS-LS interfaces. Some CO/PBX based FXS-LS interfaces originate a loop disconnect signal in from of a temporary drop in loop current towards the FXO-LS interface.

Autowink Operation

AutoWINK operation (AW) may be selected for FXS port configurations. The user must select the AWO function when conversion from FXS loop/ground-start to DID/E&M wink-start mode is required. When selected, a wink signal of 200ms duration is issued on the XMT CAS bit after off-hook detection of the connected local equipment and after the wink delay timer (WDR) expires. The wink is the go-ahead or handshake signal for the calling end to release the addressing information or routing digits.

Flash-To-Answer Supervision

Flash-to-Answer supervision (FtA) may be selected for FXS port configurations. The user must select the FTA function to provide proper answer-supervision when converting from FXS to DID or E&M interfaces. When selected, an answer supervision condition is issued for the duration of the call on the XMT CAS bit after the detection of the first hook-flash from the connected local equipment. If the answer delay timer is enabled, the answer signal is automatically set after the answer delay timer (ADR) expires. The first flash after answer is the go-ahead or call acceptance signal for the local switch to start the billing process. All subsequent hook-flashes are converted and passed normally. Please read the DID information on the FCC Part 68 page in this manual.

Originate Loop Disconnect

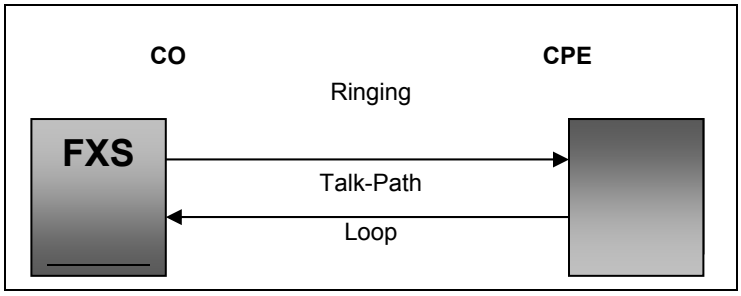
Originate Loop Disconnect (OLD) operation applies to the FXS-LS port only. The user must select the OLD function when the attached telephone equipment is capable of terminating (understanding) loop-disconnect signals. When selected, the FXS-LS port issues an automatic loop disconnect signal (loop current drop) of about 1.7 s duration if the local equipment connected to the FXS port remains in the off-hook state. The loop disconnect signal does not guarantee that the local connected equipment goes back to the on-hook condition. If the local connected equipment does not go back on-hook during the loop disconnect signal, the same off-hook condition will appear like a new request for service from the local connected equipment.

Chapter 3 – Interfaces

Interface With Loop-Start Supervision

The interface with loop-start supervision is part of the loop signaling facility interface group. This interface is often referred to as Plain-Old-Telephone-Service (POTS). "Plain-Old-Telephone-Service" is a service provided by the Central Office (CO) for common in-bound and out-bound call traffic. Loop-start is a form of signaling in which the end office supplies battery between tip and ring conductors. A terminal indicates an off-hook state by allowing current to flow. Loop refers to the closing of switch contacts across the tip and ring conductors to allow current to flow in the telephone loop. The interface with loop-start supervision is not polarity sensitive. However, it is good practice to always connect the tip-lead from one side to the tip-lead of the other side and connect the ring-lead from one side to the ring-lead from the other side. The two sides of the loop-start interface are the Foreign eXchange Office (FXO) and the Foreign eXchange Subscriber (FXS) ports.

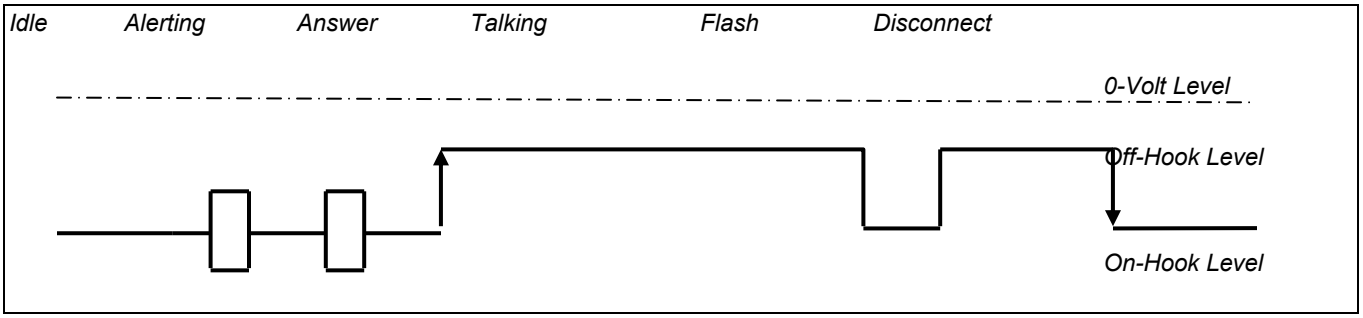
Connection



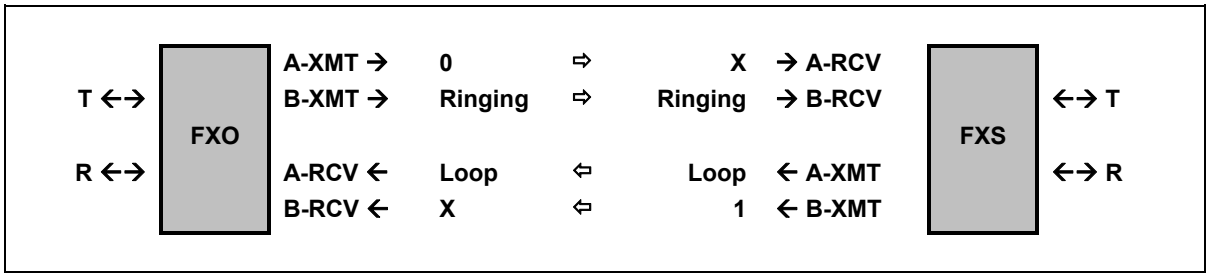
States

Conditions	No Ringing	Ringing
Open Loop	**Idle**	**Alerting**
Closed Loop	**Seized**	**Talking**

Voltage Diagram



CAS Bit Mapping



Sequence of Events

- **H** High DC resistance loop (greater than 30,000 Ohms)
- **L** Low DC resistance loop (100 Ohms to 2,400 Ohms)
- **N** Normal battery with the tip at ground potential (+Vdc) and ring at battery potential (–Vdc)
- **O** Open circuit condition (Battery and/or ground leads are removed from the circuit)

FXS-LS INITIATES, FXS-LS TERMINATES

Line States	Interface Conditions		Comments
	FXS-LS	FXO-LS	
FXS and FXO Idle	**N**	**H**	Switch and Phone are waiting for a call
FXS Alerting	**Ringing →**	**((Ringing))**	Switch send ringing towards phone
FXO Answer	**N or Ringing**	**H → L**	Phone goes off-hook to answer the call
FXS and FXS Connect	**N**	**L**	Phone and switch have a talk-path connection
FXS Disconnects First	**N → O → N**	**L**	Switch issues disconnect signal (optional)
FXO Disconnects Next	**O**	**L → H**	Phone goes on-hook

FXS-LS INITIATES, FXO-LS TERMINATES

Line States	Interface Conditions		Comments
	FXS-LS	FXS-LS	
FXS and FXO Idle	**N**	**H**	Switch and phone are waiting for a call
FXS Alerting	**Ringing →**	**((Ringing))**	Switch send ringing towards phone
FXO Answers	**N or Ringing**	**H → L**	Phone goes off-hook to answer the call
FXS and FXS Connect	**N**	**L**	Phone and Switch have a talk-path connection
FXO Disconnects First	**N**	**L → H**	Phone goes on-hook
FXS Disconnects Next	**N**	**H**	Switch assumes idle condition

FXO-LS INITIATES, FXS-LS TERMINATES

Line States	Interface Conditions		Comments
	FXS-LS	FXO-LS	
FXO and FXS Idle	**N**	**H**	Switch and phone are waiting for a call
FXO Seizes	**N**	**H → L**	Phone goes off-hook
FXO and FXS Connect	**N**	**L**	Phone and switch have a talk-path connection
FXS Disconnects First	**N → O → N**	**L**	Switch issues disconnect signal (optional)
FXO Disconnects Next	**N**	**L → H**	Phone goes on-hook

FXO-LS INITIATES, FXO-LS TERMINATES

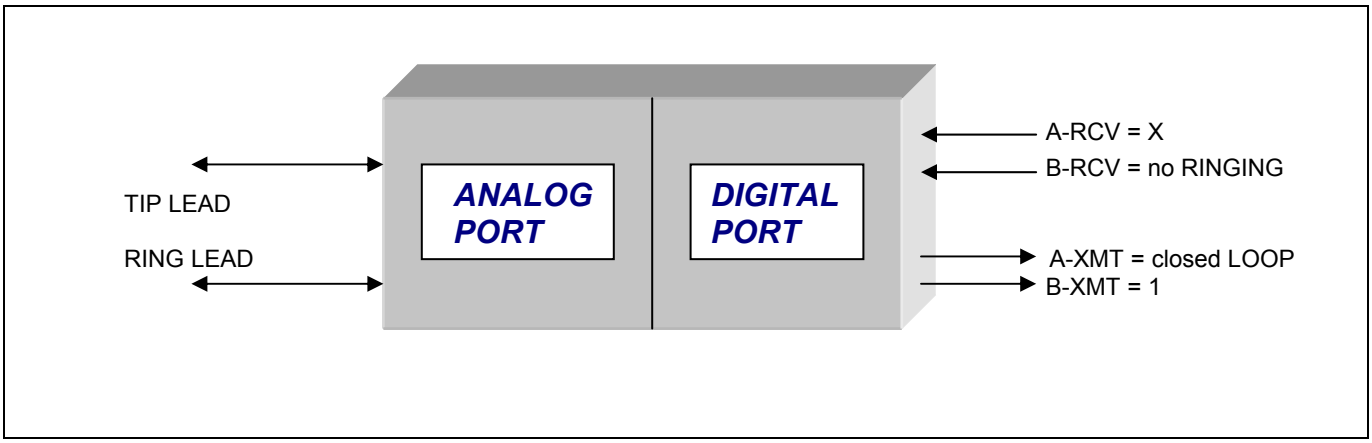
Line States	Interface Conditions		Comments
	FXS-LS	FXO-LS	
FXO and FXS Idle	**N**	**H**	Switch and phone are waiting for a call
FXO Seizes	**N**	**H → L**	Phone goes off-hook
FXO and FXS Connect	**N**	**L**	Phone and Switch have a talk-path connection
FXO Disconnects First	**N**	**L → H**	Phone goes on-hook
FXS Disconnects Next	**N**	**H**	Switch assumes idle condition

Foreign Exchange Subscriber Loop-Start Port

The Foreign Exchange Subscriber Loop-Start (FXS-LS) port looks like a telephone wall outlet jack. This port is also referred to as the CO side of the loop-start interface. Its counterpart is the FXO port configured for loop-start supervision.

Abbreviation: **FXS-LS**
Alerting: **RINGING**
CAS Bits: **A and B**
Signaling Type: **NONE**
Start mode: **LOOP-START**
Transmission: **2-WIRE**
Wire terminals: **TIP and RING**

INTERFACING



FXS-LS PORT CONDITIONS

The Analog Port	Does	What	in which state
Receives	Open	LOOP	Idle or Alerting
Receives	Closed	LOOP	Seized or Answered
Transmits	No	RINGING	Idle or Answered
Transmits	AC	RINGING	Alerting

FXS-LS PORT CAS BIT FUNCTIONS

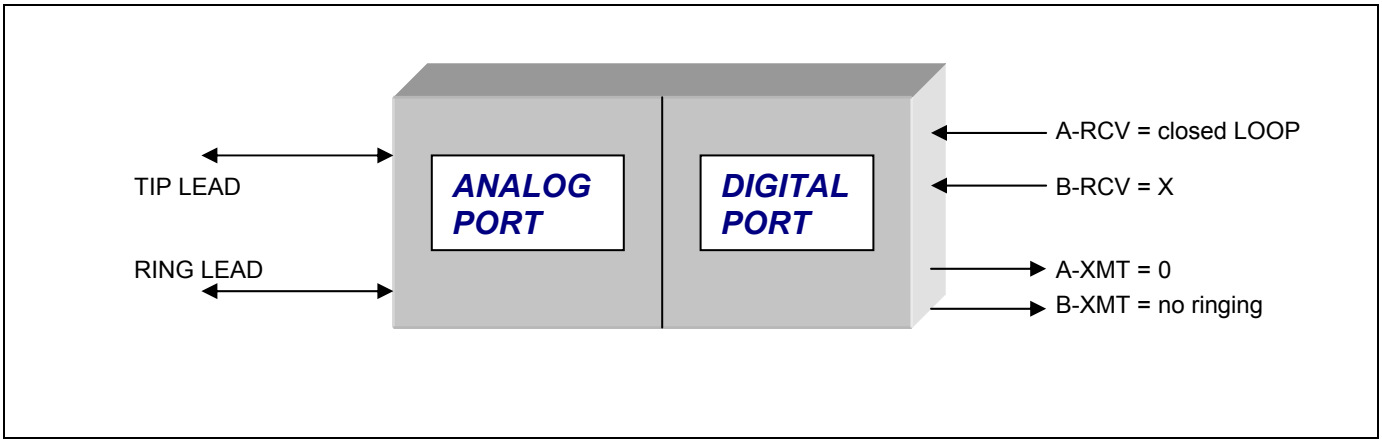
Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
Open LOOP	**0**	**1**	**-**	**-**	-
Closed LOOP	**1**	**1**	**-**	**-**	-
-	**-**	**1**	**X**	**1**	**No** RINGING
Open LOOP	**0**	**1**	**X**	**0**	**AC** RINGING
Closed LOOP	**1**	**1**	**X**	**0**	**No** RINGING

Foreign Exchange Office Loop-Start Port

The Foreign Exchange Office Loop-Start (FXO-LS) port looks like a regular telephone. This port is also referred to as the CPE side of the loop-start interface. Its counterpart is the FXS port configured for loop-start supervision.

Abbreviation: **FXO-LS**
Alerting: **RINGING**
CAS Bits: **A and B**
Signaling Type: **NONE**
Start-Mode: **LOOP-START**
Transmission: **2-WIRE**
Wire terminals: **TIP and RING**

INTERFACING



CONDITIONS

The Analog Port	does	What	in which state
Receives	No	RINGING	Idle or Seized
Receives	AC	RINGING	Alerting
Transmits	Open	LOOP	Idle or Alerting
Transmits	Closed	LOOP	Seized or Answered

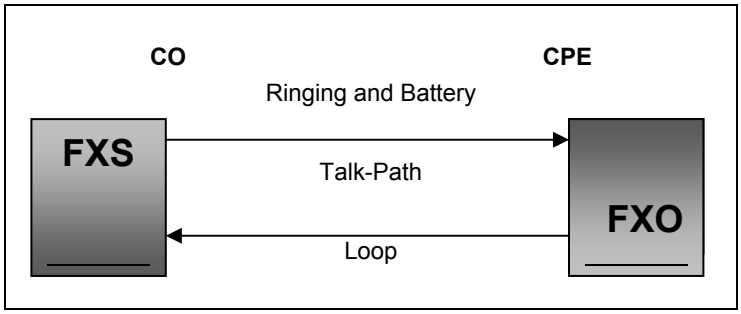
CAS BIT FUNCTIONS

Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
No RINGING	**0**	**1**	**-**	**-**	-
AC RINGING	**0**	**0**	**-**	**-**	-
-	**-**	**-**	**0**	**X**	**Open** LOOP
-	**-**	**-**	**1**	**X**	**Closed** LOOP

Interface With Reverse-Battery Supervision

The interface with reverse-battery supervision is part of the loop signaling facility interface group. This interface is capable of ringing and providing battery polarity reversal at the same time. The reverse battery signaling states vary greatly from application to application. Most typically the call waiting indication in a customer loop is performed by reversing the polarity going to the phone receiving the call waiting indication along with a 300 ms burst of the 440 Hz call waiting call-progress tone. The reverse-battery-signaling interface is polarity sensitive. It makes a difference which way the tip and ring wires are hooked up to the public switched telephone network. The two sides of the reverse-battery interface are the Foreign eXchange Office (FXO) and the Foreign eXchange Subscriber (FXS) ports.

Connection



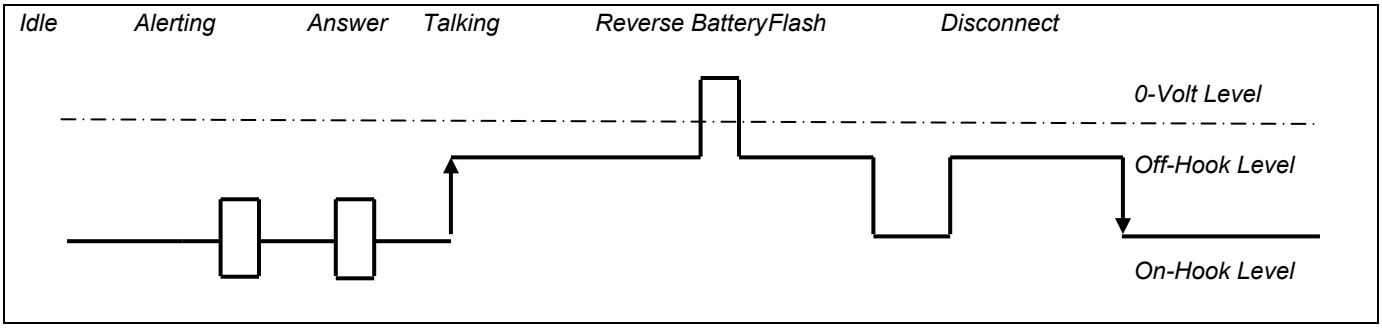
States

The reverse battery signaling states are not specified

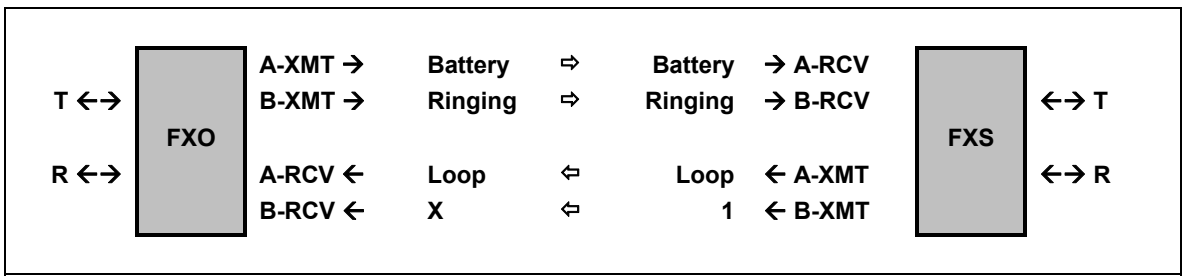
Conditions	No Ringing	Ringing
Open Loop	**Idle**	**Alerting**
Closed Loop	**Seized**	**Talking**

Voltage Diagram

The reverse battery signaling states are not specified



CAS Bit Mapping



Sequence of Events

- **H** High DC resistance loop (greater than 30,000Ohms)
- **L** Low DC resistance loop (100Ohms to 2,400Ohms)
- **N** Normal battery with the tip at ground potential (+Vdc) and ring at battery potential (–Vdc)
- **R** Reverse battery with the tip at battery (–Vdc) and the ring at ground (+Vdc)
- **O** Open circuit condition (Battery and/or ground leads are removed from the circuit)

FXS-RB INITIATES, FXS-LS TERMINATES

Line States	Interface Conditions		Comments
	FXS-LS	FXO-LS	
FXS and FXO Idle	**N**	**H**	Switch and Phone are waiting for a call
FXS Alerting	**Ringing →**	**(((Ringing)))**	Switch sends ringing towards phone
FXO Answer	**N or Ringing**	**H → L**	Phone goes off-hook to answer the call
FXS and FXS Connect	**N**	**L**	Phone and switch have a talk-path connection
FXS Reverses Polarity	**R**	**L**	Switch issues Call Waiting (**CW**) signal.
FXS Disconnects First	**N → O → N**	**L**	Switch issues disconnect signal (optional)
FXO Disconnects Next	**O**	**L → H**	Phone goes on-hook

FXS-LS INITIATES, FXO-LS TERMINATES

Line States	Interface Conditions		Comments
	FXS-LS	FXS-LS	
FXS and FXO Idle	**N**	**H**	Switch and phone are waiting for a call
FXS Alerting	**Ringing →**	**(((Ringing)))**	Switch sends ringing towards phone
FXO Answers	**N or Ringing**	**H → L**	Phone goes off-hook to answer the call
FXS and FXS Connect	**N**	**L**	Phone and Switch have a talk-path connection
FXS Reverses Polarity	**R**	**L**	Switch issues Call Waiting (**CW**) signal.
FXO Disconnects First	**N**	**L → H**	Phone goes on-hook
FXS Disconnects Next	**N**	**H**	Switch assumes idle condition

FXO-LS INITIATES, FXS-LS TERMINATES

Line States	Interface Conditions		Comments
	FXS-LS	FXO-LS	
FXO and FXS Idle	**N**	**H**	Switch and phone are waiting for a call
FXO Seizes	**N**	**H → L**	Phone goes off-hook
FXO and FXS Connect	**N**	**L**	Phone and switch have a talk-path connection
FXS Reverses Polarity	**R**	**L**	Switch issues Call Waiting (**CW**) signal.
FXS Disconnects First	**N → O → N**	**L**	Switch issues disconnect signal (optional)
FXO Disconnects Next	**N**	**L → H**	Phone goes on-hook

FXO-LS INITIATES, FXO-LS TERMINATES

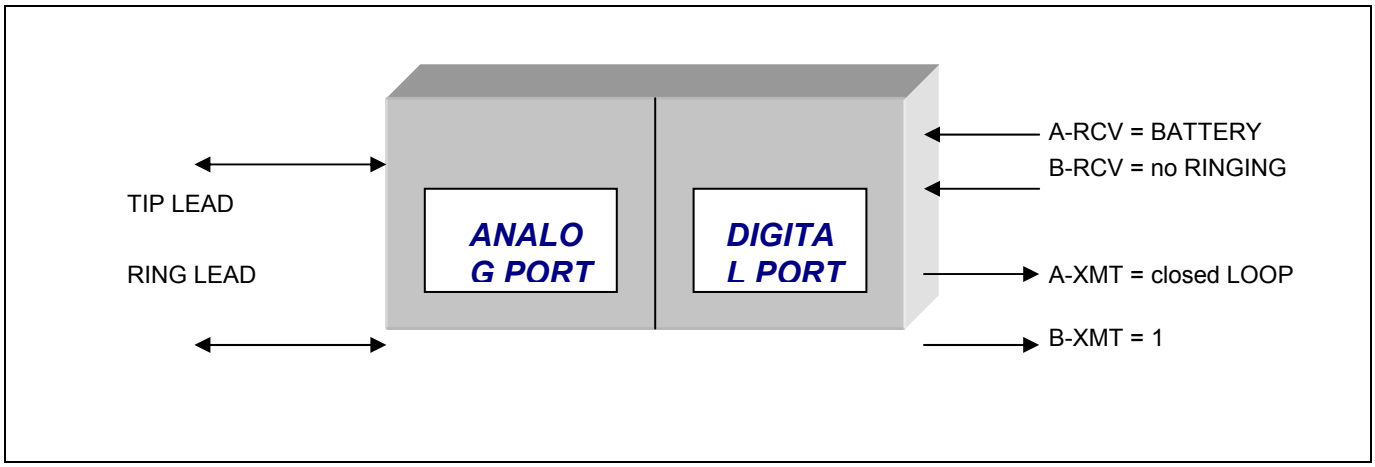
Line States	Interface Conditions		Comments
	FXS-LS	FXO-LS	
FXO and FXS Idle	**N**	**H**	Switch and phone are waiting for a call
FXO Seizes	**N**	**H → L**	Phone goes off-hook
FXO and FXS Connect	**N**	**L**	Phone and Switch have a talk-path connection
FXS Reverses Polarity	**R**	**L**	Switch issues Call Waiting (**CW**) signal.
FXO Disconnects First	**N**	**L → H**	Phone goes on-hook
FXS Disconnects Next	**N**	**H**	Switch assumes idle condition

Foreign Exchange Subscriber Reverse-Battery Port

The Foreign Exchange Subscriber Reverse Battery (FXS-RB) port looks like a Direct-Inward-Dialing CO port with ringing capabilities. Its counterpart is the FXO port configured for reverse-battery supervision.

Abbreviation	**FXS-RB**
Alerting	**RINGING**
CAS Bits	**A and B**
Signaling Type	**NONE**
Start mode	**LOOP-START**
Transmission	**2-WIRE**
Wire terminals	**TIP and RING**

FXS-RB PORT INTERFACING



FXS-RB PORT CONDITIONS

The Analog Port	Does	What	in which state
Receives	Open	LOOP	Idle or Alerting
Receives	Closed	LOOP	Seized or Answered
Transmits	No	RINGING	Idle or Answered
Transmits	AC	RINGING	Alerting
Transmits	Normal	BATTERY	Not specified
Transmits	Reverse	BATTERY	Not specified

FXS-RB PORT CAS BIT FUNCTIONS

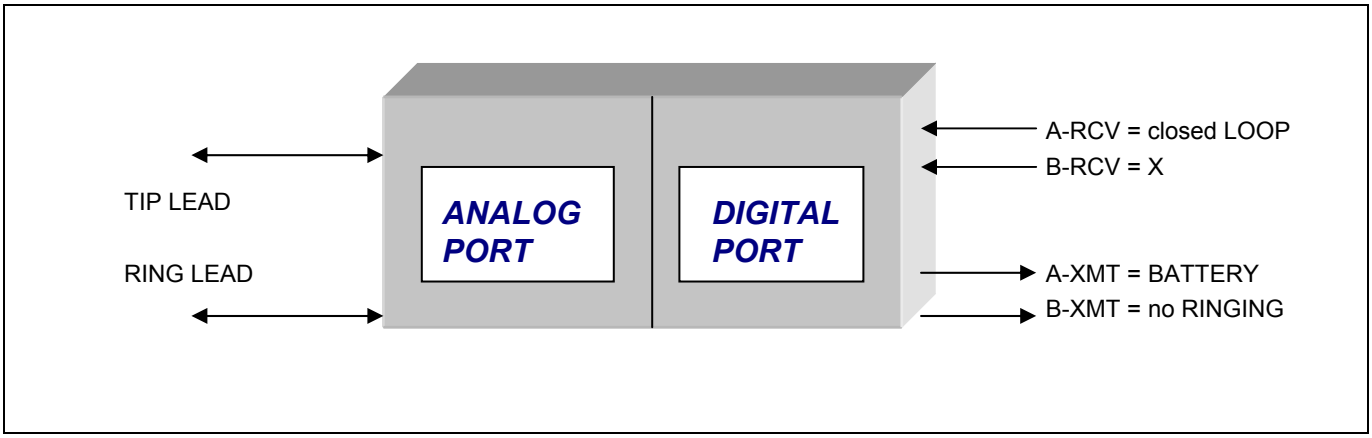
Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
Open LOOP	**0**	**1**	**-**	**-**	-
Closed LOOP	**1**	**1**	**-**	**-**	-
-	**-**	**1**	**X**	**1**	**No** RINGING
Open LOOP	**0**	**1**	**X**	**0**	**AC** RINGING
Closed LOOP	**1**	**1**	**X**	**0**	**No** RINGING
-	**X**	**1**	**0**	**X**	**Normal** BATTERY
-	**X**	**1**	**1**	**X**	**Reverse** BATTERY

Foreign Exchange Office Reverse-Battery Port

The Foreign Exchange Office Reverse-Battery (FXO-RB) port looks like a Direct-Inward-Dialing PBX port with ring detection capabilities. Its counterpart is the FXS port configured for reverse-battery supervision.

Abbreviation: **FXO-RB**
Alerting: **RINGING**
CAS Bits: **A and B**
Signaling Type: **NONE**
Start-Mode: **LOOP-START**
Transmission: **2-WIRE**
Wire terminals: **TIP and RING**

FXO-RB PORT INTERFACING



FXO-RB PORT CONDITIONS

The Analog Port	does	What	in which state
Receives	No	RINGING	Idle or Seized
Receives	AC	RINGING	Alerting
Receives	Normal	BATTERY	Not Specified
Receives	Reverse	BATTERY	Not Specified
Transmits	Open	LOOP	Idle or Alerting
Transmits	Closed	LOOP	Seized or Answered

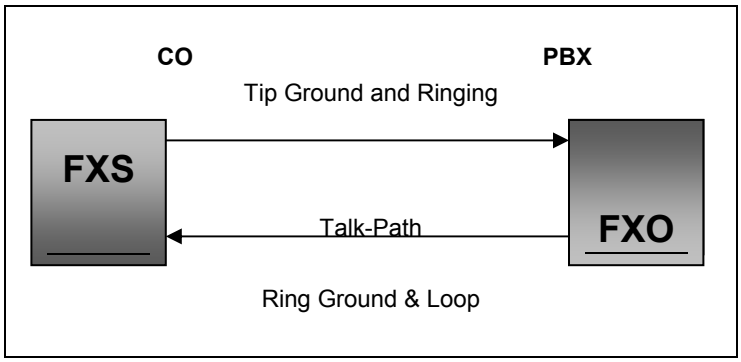
FXO-RB PORT CAS BIT FUNCTIONS

Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
No RINGING	**X**	**1**	**-**	**-**	-
AC RINGING	**X**	**0**	**-**	**-**	-
Normal BATTERY	**0**	**X**			
Reverse BATTERY	**1**	**X**			
-	**-**	**-**	**0**	**X**	**Open** LOOP
-	**-**	**-**	**1**	**X**	**Closed** LOOP

Interface With Ground-Start Supervision

The interface with ground-start supervision is part of the loop signaling facility interface group. This interface most commonly connects the trunk side of a PBX to the servicing Central Office. Ground-start is a form of signaling in which grounding a wire indicates a request for service by either interface side. The interface with ground-start supervision is polarity sensitive. Always connect the T-lead from one side to the T-lead of the other side and connect the R-lead from one side to the R-lead from the other side. If the T-lead and the R-lead are reversed, the PBX will not be able to initiate out-bound calls. The two sides of the ground-start interface are the foreign exchange office and the foreign exchange subscriber ports.

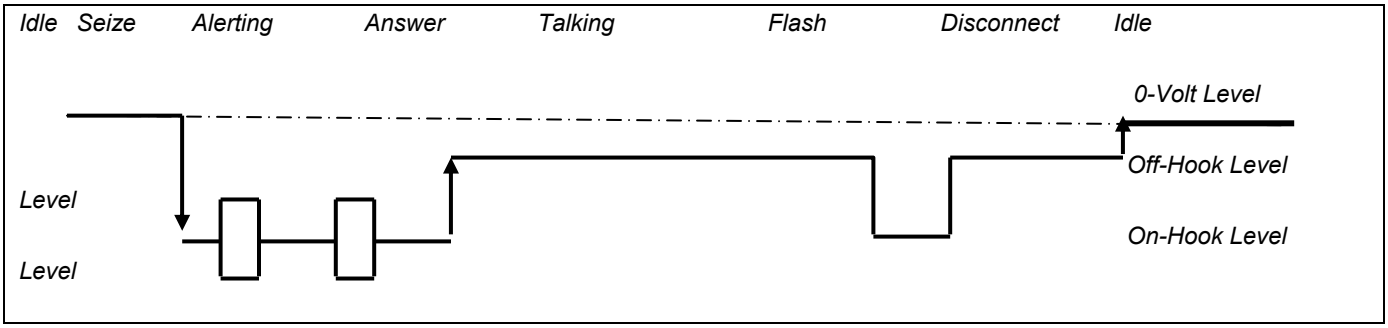
Connection



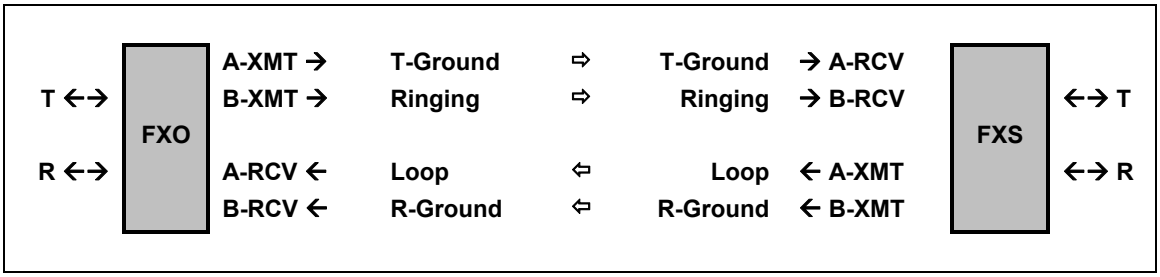
States

Conditions	No Ringing	Ringing	No Tip Ground	Tip Ground
Open Loop	**PBX Idle**	**CO Alerting**	**CO Idle**	**CO Seized**
Closed Loop	**PBX Connected**	**PBX Answered**	**PBX Error**	**PBX Answer**
No Ring Ground	**PBX Idle**	**CO Alerting**	**CO Idle**	**CO Seized**
Ring Ground	**PBX Seized**	**PBX Error**	**PBX Seized**	**PBX Connected**

Voltage Diagram



CAS Bit Mapping



Sequence of Events

- **H** High DC resistance loop (greater than 30,000 Ohms)
- **L** Low DC resistance loop (100 Ohms to 2,400 Ohms)
- **N** Normal battery with the tip lead at ground (+Vdc) and the ring lead at battery (–Vdc)
- **O** Open circuit condition (Battery and/or ground leads are removed from the circuit)

FXS-GS INITIATES, FXS-GS TERMINATES

Line States	Interface Conditions		Comments
	FXS-GS	FXO-GS	
FXS and FXO Idle	**O**	**H**	CO and PBX are waiting for a call
FXS Seizure	**N (Tip Grounded)**	**H**	CO lands a call by applying ground to tip lead
FXS Alerting	**Ringing →**	**((Ringing))**	CO send ringing towards PBX
PBX Answer	**N or Ringing**	**H → L**	PBX goes off-hook to answer the call
FXS and FXS Connect	**N**	**L**	PBX and CO now have a talk-path connection
FXS Disconnects First	**N → O**	**L**	CO removes ground from tip lead first
PBX Disconnects Next	**O**	**L → H**	PBX goes on-hook next

FXS-GS INITIATES, PBX-GS TERMINATES

Line States	Interface Conditions		Comments
	FXS-GS	PBX-GS	
FXS and PBX Idle	**O**	**H**	CO and PBX are waiting for a call
FXS Seizure	**N (Tip Grounded)**	**H**	CO lands a call by applying ground to tip lead
FXS Alerting	**Ringing →**	**((Ringing))**	CO send ringing towards PBX
FXO Answers	**N or Ringing**	**H → L**	PBX goes off-hook to answer the call
FXS and FXS Connect	**N**	**L**	PBX and CO now have a talk-path connection
FXO Disconnects First	**N**	**L → H**	PBX goes on-hook first
FXS Disconnects Next	**N → O**	**H**	CO removes ground from tip lead next

FXO-GS INITIATES, FXS-GS TERMINATES

Line States	Interface Conditions		Comments
	FXS-GS	FXO-GS	
FXO and FXS Idle	**O**	**H**	PBX and CO are waiting for a call
FXO Seizes	**O**	**H (Ring Grounded)**	PBX issues the request for service
FXS Answers	**N**	**H**	CO responds with grounding the tip
FXO Off-Hook	**N**	**H → L**	PBX goes off-hook after seeing ground on tip
FXO and FXS Connect	**N**	**L**	PBX and CO now have a talk-path connection
FXS Disconnects First	**N → O**	**L**	CO removes ground from tip lead first
FXO Disconnects Next	**O**	**L → H**	PBX goes on-hook next

FXO-GS INITIATES, FXO-GS TERMINATES

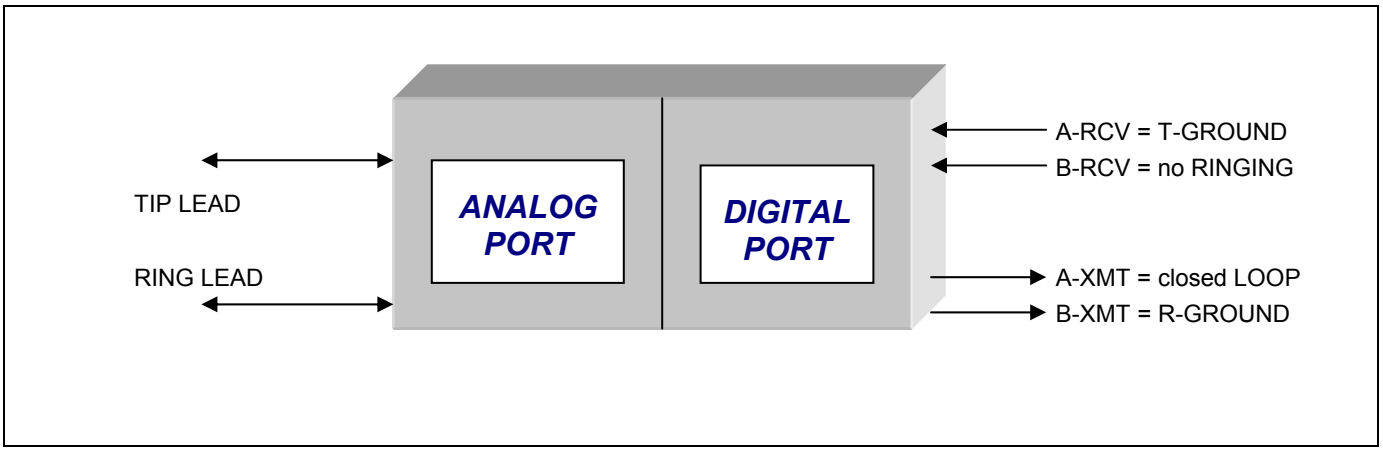
Line States	Interface Conditions		Comments
	FXS-GS	FXO-GS	
FXO and FXS Idle	**O**	**H**	CO and PBX are waiting for a call
FXO Seizes	**O**	**H (Ring Grounded)**	PBX issues the request for service
FXS Answers	**N**	**H**	CO responds with grounding the tip
FXO Off-Hook	**N**	**H → L**	PBX goes off-hook after seeing ground on tip
FXO and FXS Connect	**N**	**L**	PBX and CO now have a talk-path connection
FXO Disconnects First	**N**	**L → H**	PBX goes on-hook first
FXS Disconnects Next	**N → O**	**H**	CO removes ground from tip lead next

Foreign Exchange Subscriber Ground-Start Port

The Foreign Exchange Subscriber Ground-Start (FXS-GS) port looks like a CO trunk circuit. This port is also referred to as the CO side of the ground-start interface. Its counterpart is the FXO port configured for ground-start supervision.

Abbreviation: **FXS-GS**
Alerting: **RINGING**
CAS Bits: **A and B**
Signaling Type: **NONE**
Start Mode: **GROUND-START**
Transmission: **2-WIRE**
Wire terminals: **TIP and RING**

FXS-GS PORT INTERFACING



FXS-GS PORT CONDITIONS

The Analog port	does	what	and/or	what	in which state
Receives	OPEN	LOOP	NO RING	GROUND	PBX idle
Receives			RING	GROUND	PBX seized
Receives	CLOSED	LOOP	RING	GROUND	PBX connected
Transmits	NO	RINGING	NO TIP	GROUND	CO idle
Transmits	NO	RINGING	TIP	GROUND	CO seized
Transmits	AC	RINGING	TIP	GROUND	CO alerting
Transmits	NO	RINGING	TIP	GROUND	CO connected

FXS-GS PORT CAS BIT FUNCTIONS

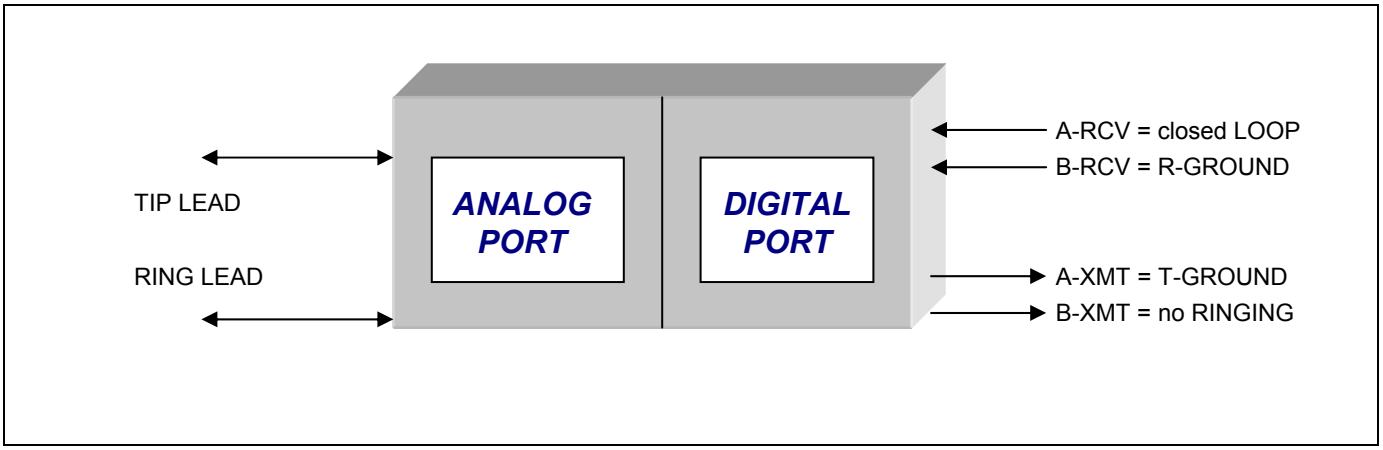
Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
Open LOOP, **No Ring** GROUND	0	1	X	-	
Open LOOP, **Ring** GROUND	0	0	1	-	**No Tip** GROUND
Closed LOOP or **Ring** GROUND	1	1	0	-	**Tip** GROUND
-	-	-	1	X	**No** RINGING, **No Tip** GROUND
-	-	-	0	1	**No** RINGING, **Tip** GROUND
Open LOOP	0	1	0	0	**AC** RINGING, **Tip** GROUND
Closed LOOP	1	1	0	0	**No** RINGING, **Tip** GROUND

Foreign Exchange Office Ground-Start Port

The Foreign Exchange Office Ground-Start (FXO-GS) port looks like a PBX trunk circuit. This port is also referred to as the PBX trunk side of the ground-start interface. Its counterpart is the FXS port configured with ground-start supervision.

Abbreviation: **FXO-GS**
Alerting: **RINGING**
CAS Bits: **A and B**
Signaling Type: **NONE**
Start mode: **GROUND-START**
Transmission: **2-WIRE**
Wire terminals: **TIP and RING**

FXO-GS PORT INTERFACING



FXO-GS PORT CONDITIONS

The Analog Port	does	what	in which state
Receives	No Tip	GROUND	CO idle
Receives	Tip	GROUND	CO seized
Receives	AC	RINGING	CO alerting
Receives	No	RINGING	CO connected
Transmits	Open	LOOP	PBX on-hook
Transmits	Closed	LOOP	PBX off-hook
Transmits	No Ring	GROUND	PBX idle
Transmits	Ring	GROUND	PBX seized

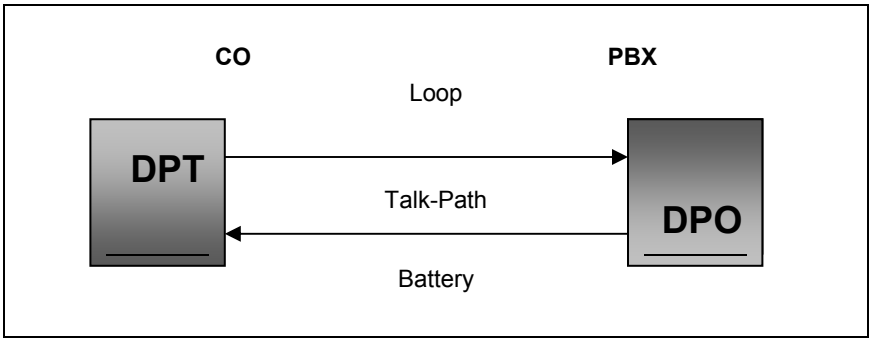
FXO-GS PORT CAS BIT FUNCTIONS

Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
No Tip GROUND	**1**	-	-	-	-
Tip GROUND	**0**	-	-	-	-
No RINGING	-	**1**	-	-	-
AC RINGING	-	**0**	-	-	-
-	-	-	**0**	-	**Open** LOOP
-	-	-	**1**	-	**Closed** LOOP
-	-	-	-	**1**	**No Ring** GROUND
-	-	-	-	**0**	**Ring** GROUND

Interface With Loop-Reverse-Battery Supervision

The interface with loop-reverse-battery supervision is part of the loop signaling facility interface group. This interface is also known as Direct-Inward-Dialing Service or DID service. DID is a function provided by the Central Office for in-bound call traffic only. The customer premise equipment (CPE), Private Branch Exchanges (PBX) or Voice Messaging Systems (VMS) typically receive the last 3 to 7 digits of the telephone number dialed by the caller through the Central Office which is connected at the other side of the DID trunk. The PBX/VMS uses the DID digits to route and place the call to a specific person (station) or during a ring-no-answer/busy-no-answer condition to an individual mailbox. The loop-reverse-battery-signaling interface is polarity sensitive. It makes a difference which way the tip and ring wires are hooked up to the public switched telephone network. If the wires are reversed, the trunk busies out and the caller may hear the all-trunks-busy or fast busy signal. The two sides of the loop-reverse-battery interface are the dial pulse originating and the dial pulse terminating (DPT) port.

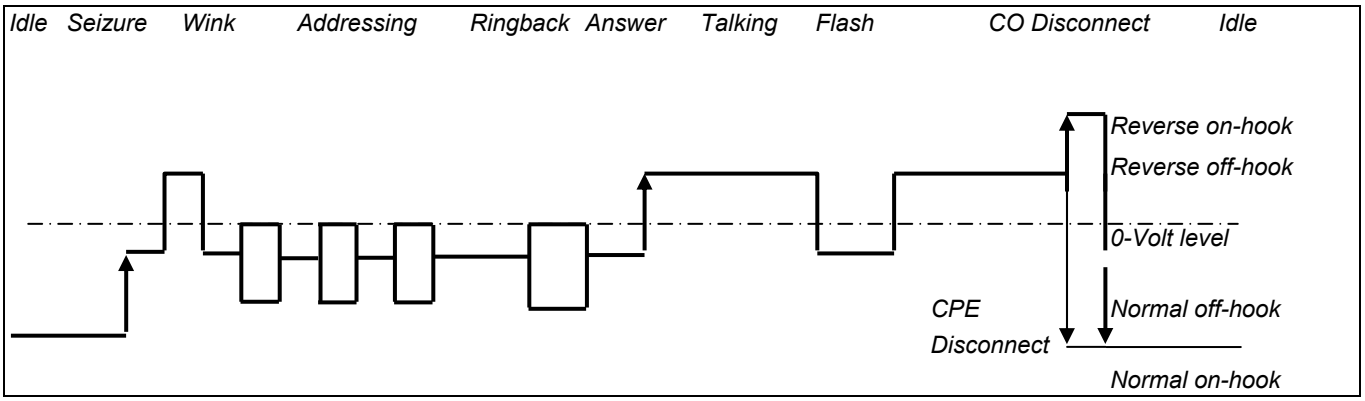
Connection



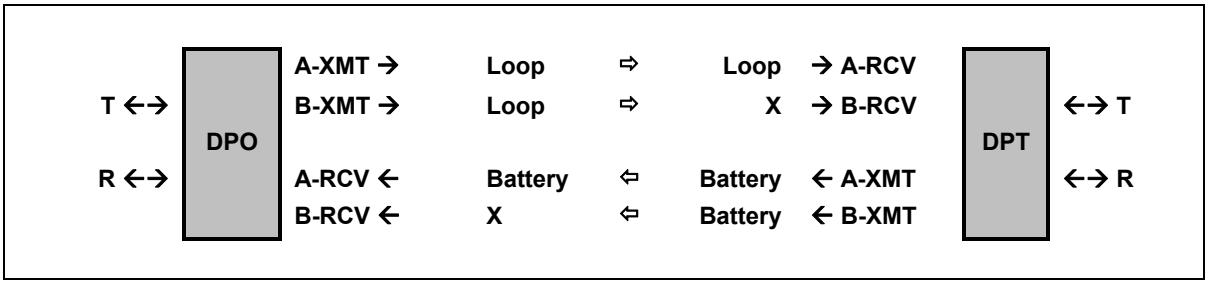
States

Conditions	Normal Battery	Reverse Battery
Loop Open	**Idle**	**Busy**
Loop Closed	**Seized**	**Answered**

Voltage Diagram



CAS Bit Mapping



Sequence of Events

- **H** High DC resistance loop (greater than 30,000 Ohms)
- **L** Low DC resistance loop (100 Ohms to 2,400 Ohms)
- **N** Normal battery with the tip at ground (+Vdc) and the ring at battery (–Vdc)
- **R** Reverse battery with the tip at battery (–Vdc) and the ring at ground (+Vdc)

DPT INITIATES, DPT TERMINATES

Line States	Interface Conditions		Comments
	DPT	DPO	
DPT and DPO Idle	**H**	**N**	CO and PBX are waiting for a call
DPT seizes	**H → L**	**N**	CO goes off-hook
DPO answers	**L**	**N → R**	PBX provides reverse battery
DPO and DPT Connect	**L**	**R**	PBX and CO have a talk-path connection
DPT Disconnects First	**L → H**	**R**	CO goes back on-hook
DPO Disconnects Next	**H**	**R → N**	PBX goes back to normal battery

DPT INITIATES, DPO TERMINATES

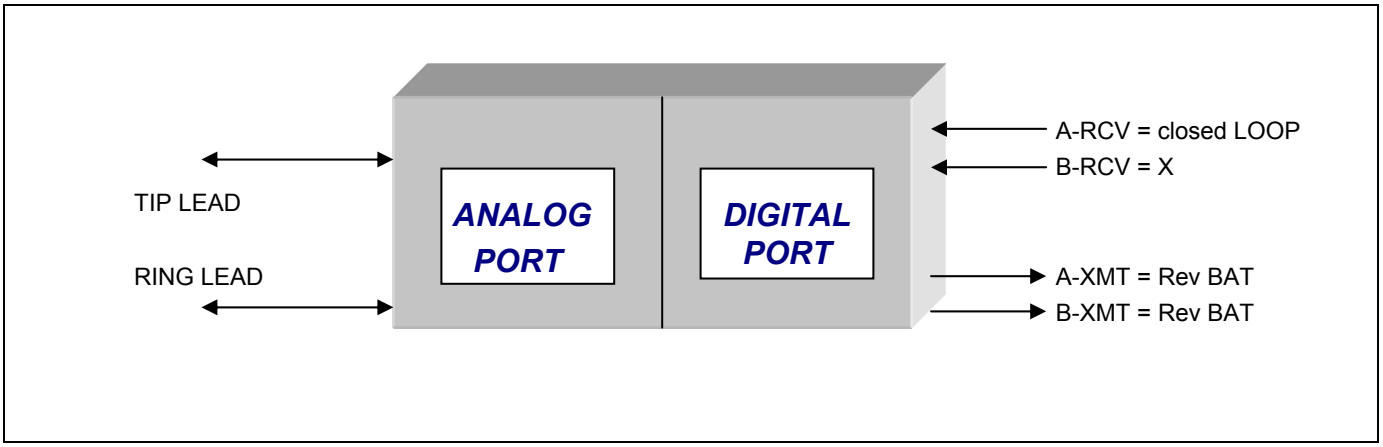
Line States	Interface Conditions		Comments
	DPT	DPO	
DPT and DPO Idle	**H**	**N**	CO and PBX are waiting for a call
DPT seizes	**H → L**	**N**	CO goes off-hook
DPO answers	**L**	**N → R**	PBX provides reverse battery
DPO and DPT Connect	**L**	**R**	PBX and CO have a talk-path connection
DPO Disconnects First	**L**	**R → N**	PBX goes back to normal battery
DPT Disconnects Next	**L → H**	**N**	CO goes back on-hook

Dial Pulse Terminating Port

The Dial Pulse Terminating (DPT) port looks like a CO network interface circuit configured for loop-reverse-battery supervision. This port is also referred to as the CO side of the DID trunk. Its counterpart is the DPO port.

Abbreviation: **DPT**
Alerting: **NONE**
CAS Bits: **A = B**
Signaling Type: **NONE**
Start Mode: **IMMEDIATE, WINK, and DELAY-DIAL**
Transmission: **2-WIRE**
Wire terminals: **TIP and RING**

DPT PORT INTERFACING



DPT PORT CONDITIONS

The Analog Port	does	What	in which state
Receives	normal	BATTERY	Idle or Seized
Receives	reverse	BATTERY	Busy or Answered
Transmits	Open	LOOP	Idle or Busy
Transmits	closed	LOOP	Seized or Answered

DPT PORT CAS BIT FUNCTIONS

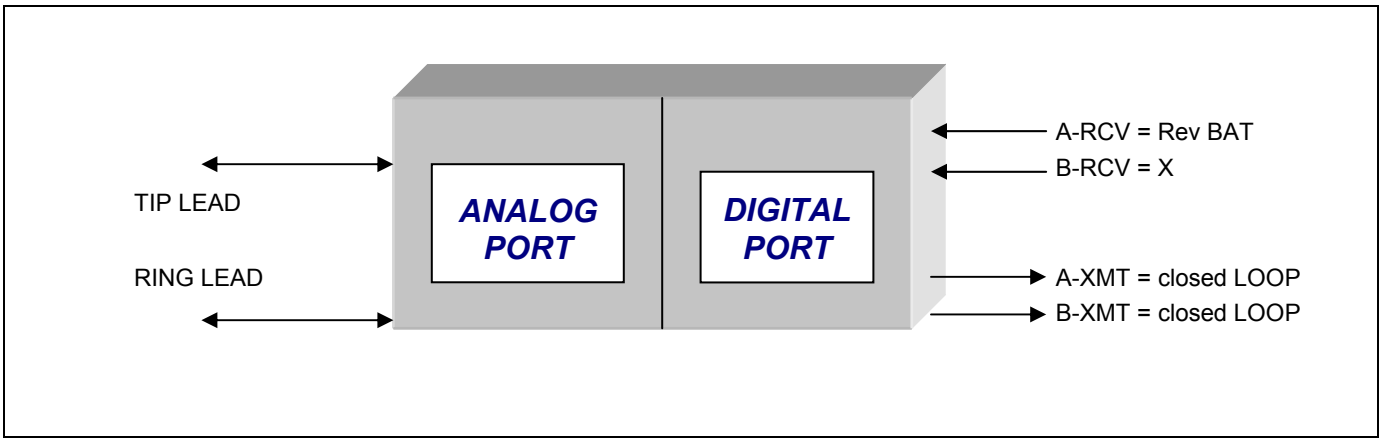
Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
Normal BATTERY	0	0	X	X	-
Reverse BATTERY	1	1	X	X	-
-	X	X	0	X	**Open** LOOP
-	X	X	1	X	**Closed** LOOP

Dial Pulse Originating Port

The Dial Pulse Originating (DPO) port looks like a CPE trunk circuit configured for loop-reverse-battery supervision. This port is also referred to as the CPE side of DID trunk. Its counterpart is the DPT port.

Abbreviation: **DPO**
Alerting: **NONE**
CAS Bits: **A = B**
Signaling Type: **NONE**
Start Modes: **IMMEDIATE, WINK, and DELAY-DIAL**
Transmission: **2-WIRE**
Wire terminals: **TIP and RING**

DPO PORT INTERFACING



DPO PORT CONDITIONS

The Analog Port	Does	what	in which state
Receives	Open	LOOP	Idle or Busy
Receives	Closed	LOOP	Seized or Answered
Transmits	Normal	BATTERY	Idle or Seized
Transmits	Reverse	BATTERY	Busy or Answered

DPO PORT CAS BIT FUNCTIONS

Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
Open LOOP	**0**	**0**	**X**	**X**	-
Closed LOOP	**1**	**1**	**X**	**X**	-
-	**X**	**X**	**0**	**X**	**Normal** BATTERY
-	**X**	**X**	**1**	**X**	**Reverse** BATTERY

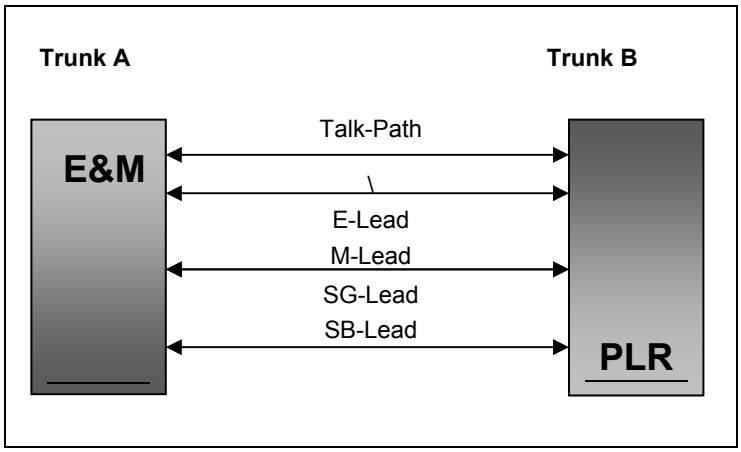
Interface With E and M Lead Supervision

The interface with E and M lead supervision is part of the E and M signaling facility interface group. The term E and M describes interfaces used by switches within the confines of a building. E and M signaling is not used in outside wiring.

On an E and M trunk, the carrier facilities or PBX Tie Lines may dial many or no digits in DTMF or MF via in-band signaling or Dial Pulse via E-lead or M-lead out-of-band signaling.

The switch uses the digits to route and place the call to a specific person (station) or during a ring-no-answer/busy-no-answer condition to an individual mailbox. The term E and M originates from the old Ear and Mouthpieces associated with early telephones. The E and M lead-signaling interface is wiring sensitive. Always connect the E-lead from one side to the E-lead of the other side. If the E and M-lead are hooked up reversed, the interface will not operate as properly. The two sides of the E and M interface are the E&M and the pulse link repeater ports (PLR).

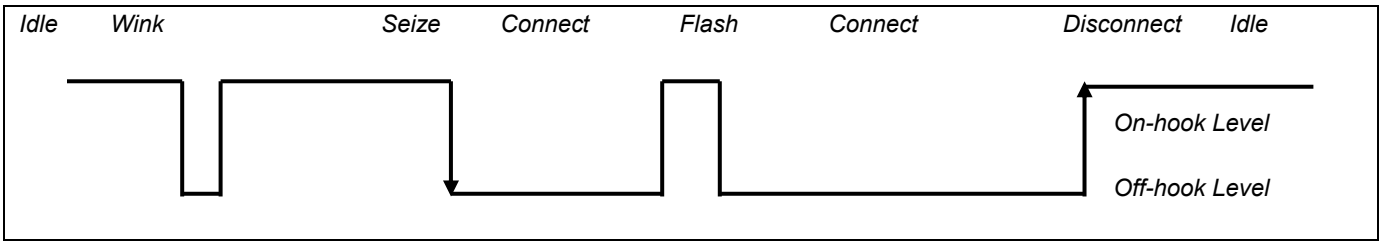
Connection



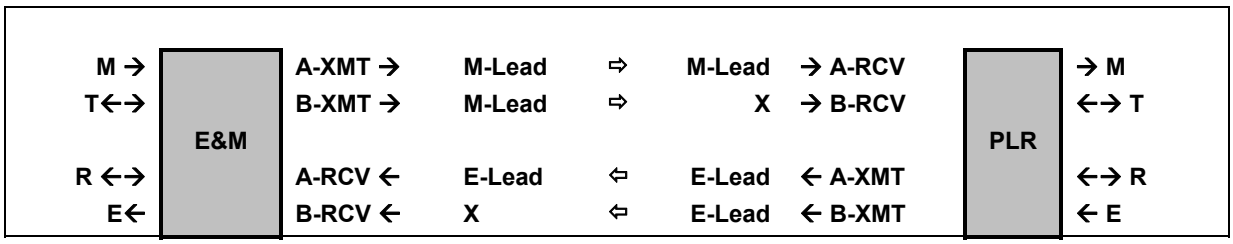
Conditions

Conditions	Open E-Lead	Ground E-lead
Ground Or Open M-Lead	**Idle**	**E-Lead Seized**
Battery Or Ground M-Lead	**M-Lead Seized**	**Connected**

Voltage Diagram



CAS Bit Mapping



Sequence of Events

- **Open** **High DC resistance loop (greater than 20,000 Ohms)**
- **Looped** **Low DC resistance loop (0 Ohms to 2,400 Ohms)**
- **Battery** **Battery potential (–Vdc)**
- **Ground** **Ground potential (+Vdc)**

TYPE I

Line States	Interface Conditions		Comments
	M	E	
Idle	Ground	Open	Trunk is waiting for a call
PLR Seizure	Battery	Open	PLR lands a call on the E and M trunk
E&M Seizure	Ground	Ground	E&M lands a call on the E and M trunk
Connect	Battery	Ground	Called party and calling party are communicating

TYPE II

Line States	Interface Conditions		Comments
	M	E	
Idle	Open	Open	Trunk is waiting for a call
PLR Seizure	Battery	Open	PLR lands a call on the E and M trunk
E&M Seizure	Open	Ground	E&M lands a call on the E and M trunk
Connect	Battery	Ground	Called party and calling party are communicating

TYPE III

Line States	Interface Conditions		Comments
	M	E	
Idle	Ground	Open	Trunk is waiting for a call
PLR Seizure	Battery	Open	PLR lands a call on the E and M trunk
E&M Seizure	Ground	Ground	E&M lands a call on the E and M trunk
Connect	Battery	Ground	Called party and calling party are communicating

TYPE IV

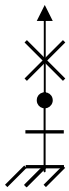
Line States	Interface Conditions		Comments
	M	E	
Idle	Open	Open	Trunk is waiting for a call
PLR Seizure	Ground	Open	PLR lands a call on the E and M trunk
E&M Seizure	Open	Ground	E&M lands a call on the E and M trunk
Connect	Ground	Ground	Called party and calling party are communicating

TYPE V

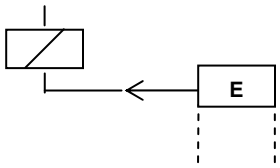
Line States	Interface Conditions		Comments
	M	E	
Idle	Open	Open	Trunk is waiting for a call
PLR Seizure	Ground	Open	PLR lands a call on the E and M trunk
E&M Seizure	Open	Ground	E&M lands a call on the E and M trunk
Connect	Ground	Ground	Called party and calling party are communicating

Interface Diagrams

Here is a listing between the different E&M/PLR port interface diagrams. For simplicity reasons the diagrams do not contain any form of circuitry or contact protection.

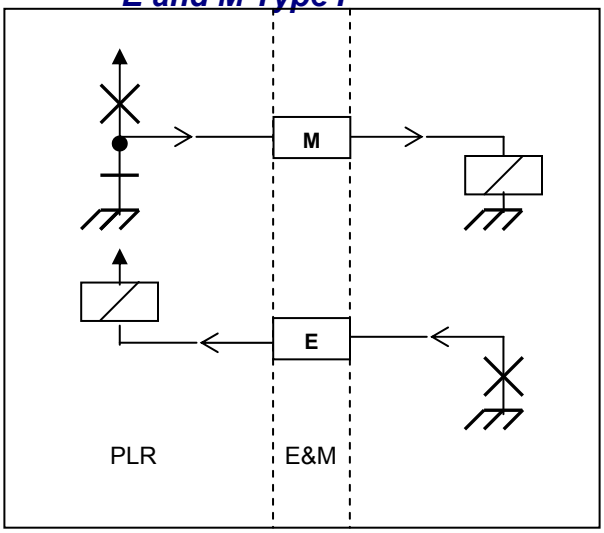


-48 Vdc Battery
Normally open Contact
Wire Junction
Normally closed Contact
Earth or Chassis Ground

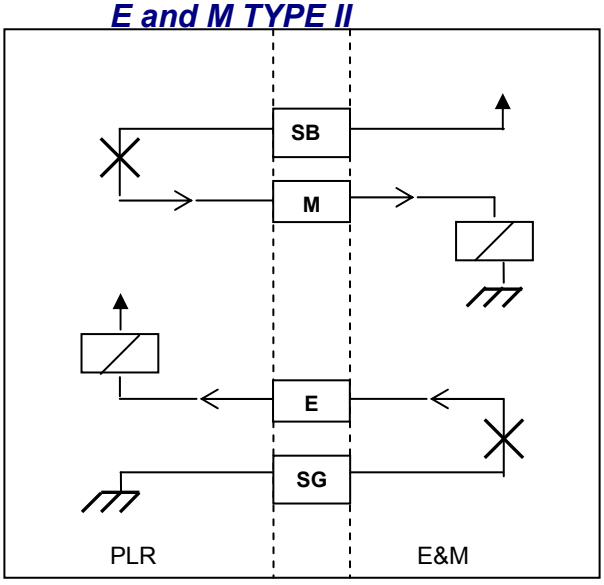


Relay
Wire Connection
Lead Terminal
Interface Demarcation

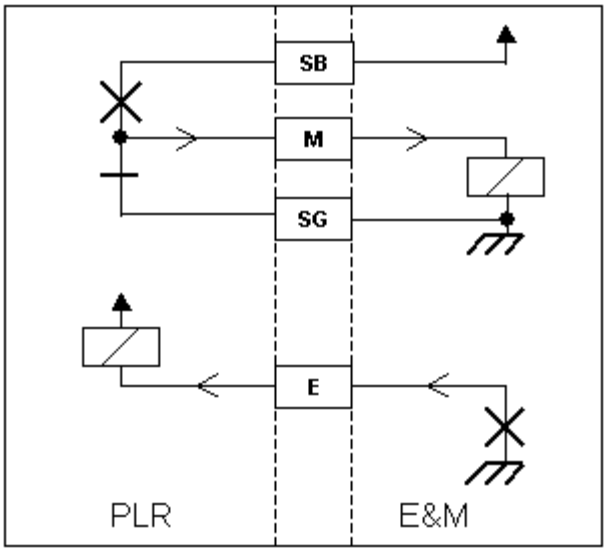
E and M Type I



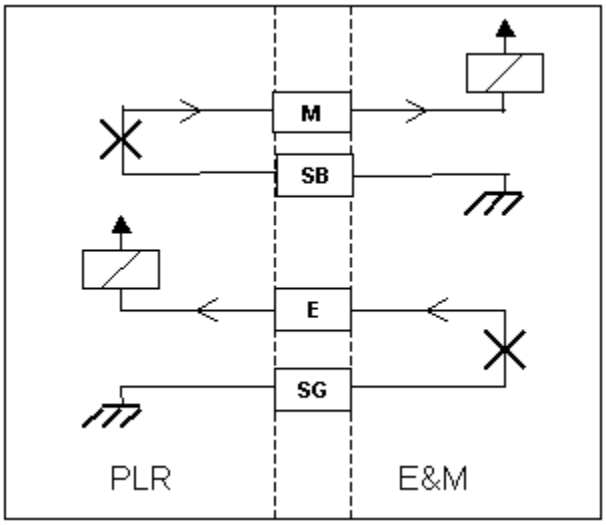
E and M TYPE II



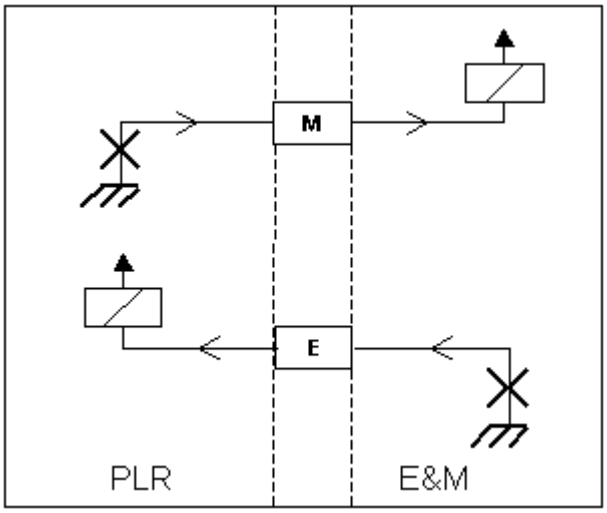
E and M TYPE III



E and M TYPE IV



E and M TYPE V

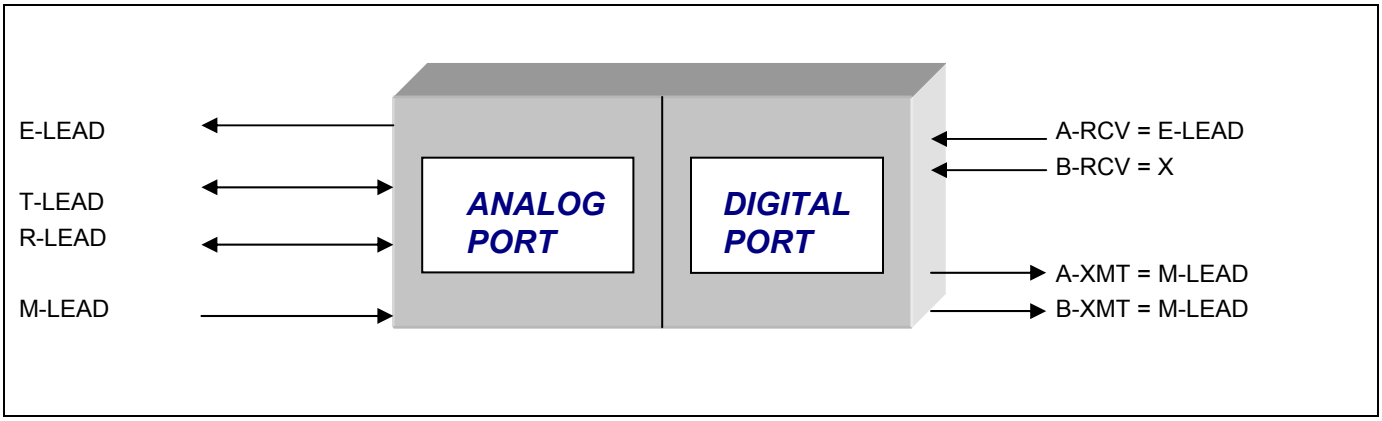


E and M Port

The E and M (E&M) port looks like a signaling circuit configured for E and M supervision. This port is also referred to as the normal E&M side of the E and M signaling interface. Its counterpart is the PLR port.

Abbreviation: **E&M**
Alerting: **NONE**
CAS Bits: **A = B**
Signaling Type: **I, II, III, IV, V**
Start Mode: **IMMEDIATE, WINK, and DELAY-DIAL**
Transmission: **2-WIRE and 4-WIRE**
Wire terminals: **T, R, T1, R1, E, M, SG, SB, and TRC**

E&M PORT INTERFACING



E&M PORT CONDITIONS

The Analog Port	Does	What	In which state
Receives	Ground or Open	M-LEAD	Idle or E-Lead Seized
Receives	Battery or Ground	M-LEAD	Seized or Connected
Transmits	Open	E-LEAD	Idle or M-Lead Seized
Transmits	Ground	E-LEAD	Seized or Connected

E&M PORT CAS BIT FUNCTIONS

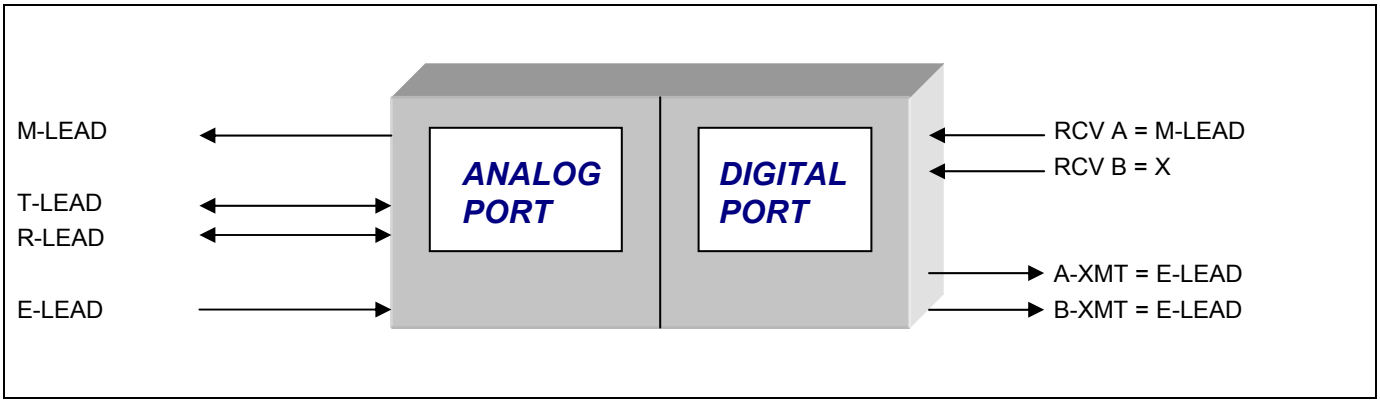
Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
Ground or **Open** M-LEAD	**0**	**0**	**X**	**X**	-
Battery or **Ground** M-LEAD	**1**	**1**	**X**	**X**	-
-	**X**	**X**	**0**	**X**	**Open** E-LEAD
-	**X**	**X**	**1**	**X**	**Ground** E-LEAD

Pulse Link Repeater Port

The Pulse Link Repeater (PLR) port looks like a trunk circuit configured for E and M supervision. This port is also referred to as the reverse E and M side of the E and M signaling interface. Its counterpart is the E&M port.

Abbreviation: **PLR**
Alerting: **NONE**
CAS Bits: **A = B**
Signaling Type: **I, II, III, IV, V**
Start Mode: **IMMEDIATE, WINK, and DELAY-DIAL**
Transmission: **2-WIRE and 4-WIRE**
Wire terminals: **T, R, T1, R1, E, M, SG, SB, and TRC**

INTERFACING



CONDITIONS

The Analog Port	Does	What	In which state
Receives	Open	E-LEAD	Idle or M-Lead Seized
Receives	Ground	E-LEAD	Seized or Connected
Transmits	Ground or Open	M-LEAD	Idle or E-Lead Seized
Transmits	Battery or Ground	M-LEAD	Seized or Connected

CAS BIT FUNCTIONS

Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
Open E-LEAD	**0**	**0**	**X**	**X**	-
Ground E-LEAD	**1**	**1**	**X**	**X**	-
-	**X**	**X**	**0**	**X**	**Ground** or **Open** M-LEAD
-	**X**	**X**	**1**	**X**	**Battery** or **Ground** M-LEAD

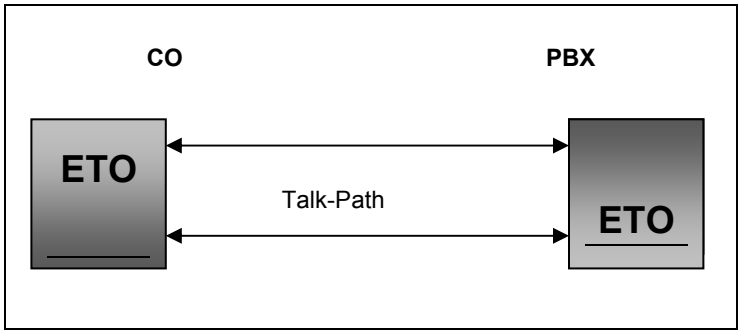
Interface With No Supervision

No supervision indicates that the trunk is a “dry” circuit. “Dry” means that there is no battery power or flow of any current involved. There is also no signaling associated with this kind of interface. The talk-path consists of a balanced wire pair and is suitable for long haul signal transmissions. The signaling interface without any supervision is not wiring sensitive. However, it is good practice to always connect the T-lead from one side to the T-lead of the other side and connect the R-lead from one side to the R-lead from the other side. The Interface with no supervision maintains a constant and direct talk-path connection to the other side.

The following ports are part of this interface:

- **Transmission Only (TO)**
- **Equalized Transmission Only (ETO)**

Connection



Conditions

Conditions	NO Signaling
NO Signaling	**Connected**

Sequence of Events

X = Any condition

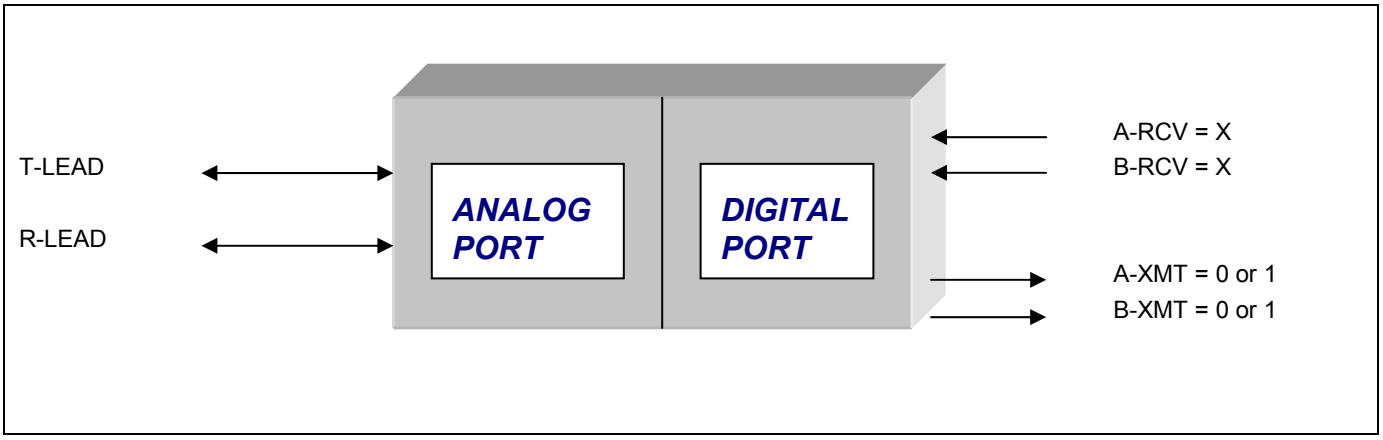
Line States	**Interface Conditions**		**Comments**
	TO	*TO*	
Idle = Connect	**X**	**X**	Line is passing payload

Transmission-Only Port

The Transmission-Only (TO) port looks like a two-wire terminal circuit configured for no supervision. This port is also referred to as the 2-wire dry voice circuit. This port may carry talk-path information in either direction on the same wire pair. The advantage of the TO is that transmit and receive signals are carried on one wire pair only. Its counterpart is the TO port.

Abbreviation: **"TO"**
Alerting: **NONE**
CAS Bits: **does not care**
Signaling Type: **NONE**
Start Mode: **NONE**
Transmission: **2-WIRE**
Wire terminals: **T, R**

INTERFACING



CONDITIONS

The Analog Port	Does	What	In which state
Receives	No	SIGNALING	Any
Transmits	No	SIGNALING	Any

CAS BIT FUNCTIONS

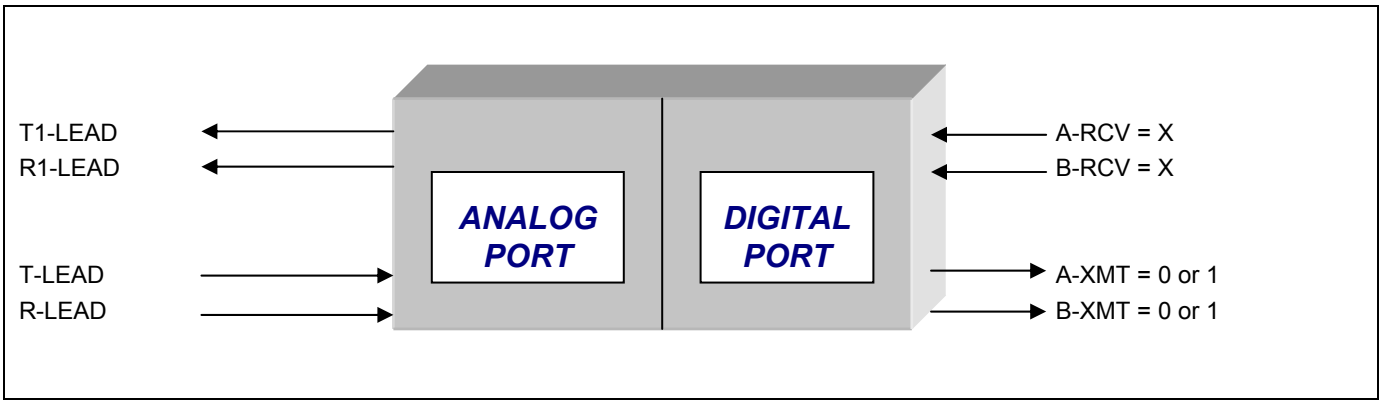
Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
No SIGNALING	**0 or 1**	**0 or 1**	**X**	**X**	**No** SIGNALING

Equalized Transmission-Only Port

The Equalized Transmission Only (ETO) port looks like a four-wire terminal circuit configured for no supervision. This port is also referred to as the 4-wire dry voice circuit. The port carries transmit and receive talk-path information on separate wire pairs. The advantage of the ETO is that signals can easily be amplified, attenuated, or equalized as required. Each wire pair of this four-wire circuit has to be defined as transmit only and receive only port. Its counterpart is the ETO port.

Abbreviation	**ETO**
Alerting	**NONE**
CAS Bits	**does not care**
Signaling Type	**NONE**
Start Mode	**NONE**
Transmission	**4-WIRE**
Wire terminals	**T, R, T1, and R1**

INTERFACING



CONDITIONS

The Analog Port	Does	What	In which state
Receives	No	SIGNALING	Any
Transmits	No	SIGNALING	Any

CAS BIT FUNCTIONS

Input To Port	A-XMT	B-XMT	A-RCV	B-RCV	Output From Port
No SIGNALING	**0 or 1**	**0 or 1**	**X**	**X**	**No** SIGNALING

Chapter 4 – Module Registers

Address and data are written into or read back from the 32 module registers through the control interface port using either UART or SPI communication. All module register write instructions require 2 bytes.

- Some of the registers are read only
- Some of the registers should not be written to
- Some of the registers are not user accessible
- Some of the registers are reserved for future use
- Some of the registers are for factory use only

#	FUNCTION	ABBR.	Read	Write
1	Module Mode Register	MMR	0x60	0x20
2	Solid State Register 1	SSR1	For factory use only	
3	Telephony Error Status Register	TER	0x62	Read only
4	Solid State Register 2	SSR2	For factory use only	
5	CAS Bit Status Register	CBR	0x64	Read only
6	CAS Bit Manipulation Register	CMR	0x65	0x25
7	CAS Bit Receive Declaration Register	RDR	0x66	0x26
8	CAS Bit Transmit Declaration Register	TDR	0x67	0x27
9	Interface Selection Register	ISR	0x68	0x28
10	Ring Pattern Register	RPR	0x69	0x29
11	Ring Frequency Register	RFR	0x6A	0x2A
12	Ring Voltage Register	RVR	0x6B	0x2B
13	Telecom Voltage Register	TVR	0x6C	0x2C
14	Upper Ring Frequency Detection Limit Register	URFDLR	0x6D	0x2D
15	Lower Ring Frequency Detection Limit Register	LRFDLR	0x6E	0x2E
16	Special Function Register	SFR	0x6F	0x2F
17	Codec Control Register	CCR	0x70	0x30
18	Interface Latch Register	ILR	For factory use only	
19	Latch Direction Register	LDR	For factory use only	
20	Reserved for Future Use	-	0x73	0x33
21	Receive Gain Register	RGR	0x74	0x34
22	Transmit Gain Register	TGR	0x75	0x35
23	Hybrid Balance Register 1	HBR1	0x76	Write not recommended
24	Hybrid Balance Register 2	HBR2	0x77	Write not recommended
25	Hybrid Balance Register 3	HBR3	0x78	Write not recommended
26	Receive Time-slot Register	RTR	0x79	0x39
27	Transmit Time-slot Register	TTR	0x7A	0x3A
28	Reserved for Future Use	-	0x7B	0x3B
29	SPI Control Register	SPCR	0x7C	0x3C
30	Wink Delay Register	WDR	0x7D	0x3D
31	Answer Delay Register	ADR	0x7E	0x3E
32	Reset Count Register	RCR	0x7F	0x3F

Factory Defaults

All user accessible read/write registers have factory pre-loaded register default values. The values have been selected for standard North American telephone operation. Writing 0x02 to the Module Mode Register (MMR) restores the factory default values. After the factory default values have been restored the user settings may have to be re-loaded.

Default Settings

Register	Read	Value	Function	Parameter
MMR	0x60	0xXX	Module Mode Register	Returns firmware version
SSR1	0x61	0xXX	Solid State One Register	No default value applicable
TER	0x62	0xXX	Telephony Error Register	No default value applicable
SSR2	0x63	0xXX	Solid State Two Register	No default value applicable
CBR	0x64	0xXX	CAS Bit Status Register	No default value applicable
CMR	0x65	0x00	CAS Bit Manipulation	Nothing manipulated
RDR	0x66	0x00	CAS Bit Receive Declaration	Nothing declared
TDR	0x67	0x00	CAS Bit Transmit Declaration	Nothing declared
ISR	0x68	0x01	Interface Selection	FXO-LS (looks like a telephone)
RPR	0x69	0x00	Ring Pattern Selection	DA1C1 (typical pattern)
RFR	0x6A	0x32	Ring Frequency Selection	20.00 Hz (typical frequency)
RVR	0x6B	0x1F	Ring Voltage Selection	71.30 Vac (highest voltage)
TVR	0x6C	0x00	Telecom Voltage Selection	50.00 Vdc (typical voltage)
URFDLR	0x6D	0x0E	Upper Ring Frequency Detection Limit	71.42 Hz (highest limit)
LRFDLR	0x6E	0x3F	Lower Ring Frequency Detection Limit	15.87 Hz (lowest limit)
SFR	0x6F	0x00	Special Function Register	No special function selected
CCR	0x70	0x80	Codec Control Selection	-2.048 MHz TDM clock -u-Law companding -Delayed data timing
ILR	0x70	0xCC	Interface Latch	Fixed and not user accessible
LDR	0x72	0x30	Latch Direction	Fixed and not user accessible
-	0x73	0x00	Reserved for Future Use	No default value applicable
RGR	0x74	0xC2	Receive Gain Selection	+2.0 dB
TGR	0x75	0x83	Transmit Gain Selection	+6.0 dB
HBR1	0x76	0xE0	Hybrid Balance Register 1	Should not be changed by user
HBR2	0x77	0x24	Hybrid Balance Register 2	Should not be changed by user
HBR3	0x78	0x26	Hybrid Balance Register 3	Should not be changed by user
RTR	0x79	0x80	Receive Time-slot Selection	TDM Time-slot is set to 0
TTR	0x7A	0x80	Transmit Time-slot Selection	TDM Time-slot is set to 0
-	0x7B	0xXX	Reserved for Future Use	No default value applicable
SPCR	0x7C	0xC7	SPI Control Register	-MSB first -Low when Idle -Clock on leading edge
WDR	0x7D	0xFF	Wink Delay Register	Wink delay timing is disabled
ADR	0x7E	0xFF	Answer Delay Register	Answer delay timing is disabled
RCR	0x7F	0xXX	Reset Count Register	No default value applicable

Value Ranges

From the following registers the user may select a specific value from a range of values. Factory default settings are loaded for ease of use and installation.

Register Range Settings

#	Parameter	Register	Minimum	Default	Maximum
11	Ring Frequency	RFR	16.13 Hz	20.00 Hz	66.67 Hz
12	Ring Voltage	RVR	19.30 Vrms	71.30 Vrms	71.30 Vrms
13	Telecom Voltage	TVR	24.70 Vdc	50.00 Vdc	74.70 Vdc
14	Upper Ring Frequency Detection Limit	URFDLR	15.87 Hz	71.42 Hz	71.42 Hz
15	Lower Ring Frequency Detection Limit	LRFDLR	15.87 Hz	15.87 Hz	71.42 Hz
21	Receive Gain	RGR	-17.3 dB	+2.0 dB	+2.1 dB
22	Transmit Gain	TGR	-0.4 dB	+6.0 dB	+19.0 dB
30	Wink Delay	WDR	0 s	Off	25.4 s
31	Answer Delay	ADR	0 s	Off	25.4 s

Individual Register Details

Module Mode Register

The module mode register allows the user to set a number or special module modes. The module can be shut down in order to reduce its current draw to about 4mA. Shutting down the module powers down all active components of the module, including the on board processor. In this mode the module will not respond to any external input or communication command. A temporary transition to the high state on the module's reset pin is required to bring the module back to normal operation. The module is pre-loaded with register default settings. In the default mode the module look like a regular telephone or modem input. See the register default settings for further information.

- Reading this register returns the firmware version number
- Writing 0x00 to this register has no effect
- Writing 0x01 to this register shuts down the module
- Writing 0x02 to this register restores the original factory default register settings

MMR Settings

Read @ 0x60

Write @ 0x20

Function	Bit Number							
	7	6	5	4	3	2	1	0
Reserved	**X**	-	-	-	-	-	-	-
Reserved	-	**X**	-	-	-	-	-	-
Reserved	-	-	**X**	-	-	-	-	-
Reserved	-	-	-	**X**	-	-	-	-
Reserved	-	-	-	-	**X**	-	-	-
Reserved	-	-	-	-	-	**X**	-	-
Normal Operation	-	-	-	-	-	-	**0**	-
Restore Factory Defaults	-	-	-	-	-	-	**1**	-
Normal Operation	-	-	-	-	-	-	-	**0**
Shut Down	-	-	-	-	-	-	-	**1**

Telephony Error Register

The telephony error register indicates various analog port error conditions. The interface is capable of recognizing the absence of current when current should be flowing. In, short, when going off-hook, current should flow. If current does not flow in an off-hook condition, then the port is either not powered correctly either due to wiring error or a power fail condition on the other side of the interface. Errors are normally due to wiring mistakes or incompatible interface port operation.

The following analog port errors may be encountered during operation:

FXO-LS	**Closed loop condition but loop current is not flowing**
FXO-RB	**Closed loop condition but loop current is not flowing**
FXO-GS	**Ring ground condition but ground current is not flowing**
FXO-GS	**Closed loop condition but loop current is not flowing**
DPT	**Closed loop condition but loop current is not flowing**
E&M	**E-lead active but E-lead current is not flowing**
PLR	**M-lead active but M-lead current is not flowing**

No error condition is detectable for FXS, DPO, TO and ETO port interfaces.

The TER is a read only register. The new value is latched until the next register read resets the value back to “0”.

TER Settings

Read @ 0x62

Function	Bit Number							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
M Normal Current Load Ok	0	-	-	-	-	-	-	-
M Normal Current Load Error	1	-	-	-	-	-	-	-
M Reverse Current Load Ok	-	0	-	-	-	-	-	-
M Reverse Current Load Error	-	1	-	-	-	-	-	-
E Normal Current Load Ok	-	-	0	-	-	-	-	-
E Normal Current Load Error	-	-	1	-	-	-	-	-
E Reverse Current Load Ok	-	-	-	0	-	-	-	-
E Reverse Current Load Error	-	-	-	1	-	-	-	-
Reserved	-	-	-	-	0	-	-	-
Reserved	-	-	-	-	-	0	-	-
Reserved	-	-	-	-	-	-	0	-
Reserved	-	-	-	-	-	-	-	0

CAS Bit Status Register

The CAS Bit Status Register allows the user to read the CAS bit status for the current condition of the selected interface port. The CBR is a read only register.

CBR Settings

Read @ 0x64

Function	Bit Number							
	7	6	5	4	3	2	1	0
A-RCV	X	-	-	-	-	-	-	-
B-RCV	-	X	-	-	-	-	-	-
C-RCV	-	-	X	-	-	-	-	-
D-RCV	-	-	-	X	-	-	-	-
A-XMT	-	-	-	-	X	-	-	-
B-XMT	-	-	-	-	-	X	-	-
C-XMT	-	-	-	-	-	-	X	-
D-XMT	-	-	-	-	-	-	-	X

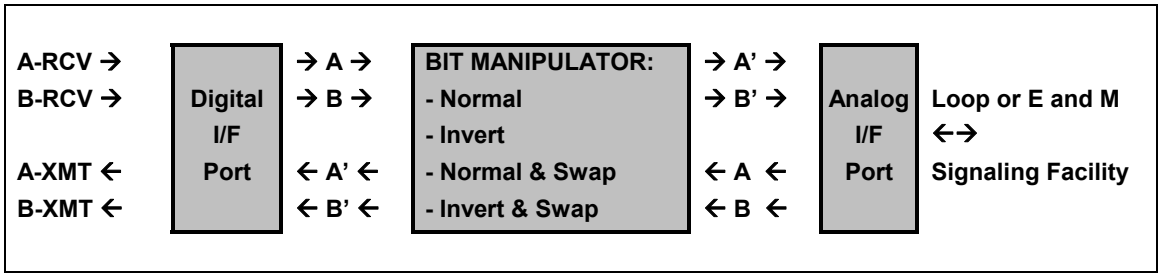
CAS Bit Manipulation Register

The CAS Bit manipulation register allows the user to pass normal, invert, or swap specific CAS receive and/or transmit bits.

EXAMPLE

A-RCV invert and swap results in B' looking like an inverted A-RCV level

B-RCV normal and swap results in A' looking like a normal B-RCV level



CMR SETTINGS

Read @ 0x65

Write @ 0x25

Function	Bit Number							
	7	6	5	4	3	2	1	0
A-RCV Normal	0	0	-	-	-	-	-	-
A-RCV Invert	0	1	-	-	-	-	-	-
A-RCV Normal & Swap	1	0	-	-	-	-	-	-
A-RCV Invert & Swap	1	1	-	-	-	-	-	-
B-RCV Normal	-	-	0	0	-	-	-	-
B-RCV Invert	-	-	0	1	-	-	-	-
B-RCV Normal & Swap	-	-	1	0	-	-	-	-
B-RCV Invert & Swap	-	-	1	1	-	-	-	-
A-XMT Normal	-	-	-	-	0	0	-	-
A-XMT Invert	-	-	-	-	0	1	-	-
A-XMT Normal & Swap	-	-	-	-	1	0	-	-
A-XMT Invert & Swap	-	-	-	-	1	1	-	-
B-XMT Normal	-	-	-	-	-	-	0	0
B-XMT Invert	-	-	-	-	-	-	0	1
B-XMT Normal & Swap	-	-	-	-	-	-	1	0
B-XMT Invert & Swap	-	-	-	-	-	-	1	1

CAS Bit Receive Declaration Register

The CAS bit receive declaration register allows the user to force a specific receive CAS bit to a pre-set state for the selected interface port operation.

RDR SETTINGS

Read @ 0x66

Write @ 0x26

Function	Bit Number							
	7	6	5	4	3	2	1	0
A-RCV Not Set	0	0	-	-	-	-	-	-
A-RCV Set To 0	0	1	-	-	-	-	-	-
A-RCV Set To 1	1	0	-	-	-	-	-	-
A-RCV Set To B	1	1	-	-	-	-	-	-
B-RCV Not Set	-	-	0	0	-	-	-	-
B-RCV Set To 0	-	-	0	1	-	-	-	-
B-RCV Set To 1	-	-	1	0	-	-	-	-
B-RCV Set To A	-	-	1	1	-	-	-	-
C-RCV Set To 0	-	-	-	-	0	0	-	-
C-RCV Set To 1	-	-	-	-	0	1	-	-
C-RCV Set To A	-	-	-	-	1	0	-	-
C-RCV Set To B	-	-	-	-	1	1	-	-
D-RCV Set To 0	-	-	-	-	-	-	0	0
D-RCV Set To 1	-	-	-	-	-	-	0	1
D-RCV Set To A	-	-	-	-	-	-	1	0
D-RCV Set To B	-	-	-	-	-	-	1	1

CAS Bit Transmit Declaration Register

The CAS bit transmit declaration register allows the user to force a specific transmit CAS bit to a pre-set state for the selected interface port operation.

TDR SETTINGS

Read @ 0x67

Write @ 0x27

Function	Bit Number							
	7	6	5	4	3	2	1	0
A-XMT Not Set	0	0	-	-	-	-	-	-
A-XMT Set To 0	0	1	-	-	-	-	-	-
A-XMT Set To 1	1	0	-	-	-	-	-	-
A-XMT Set To B	1	1	-	-	-	-	-	-
B-XMT Not Set	-	-	0	0	-	-	-	-
B-XMT Set To 0	-	-	0	1	-	-	-	-
B-XMT Set To 1	-	-	1	0	-	-	-	-
B-XMT Set To A	-	-	1	1	-	-	-	-
C-XMT Set To 0	-	-	-	-	0	0	-	-
C-XMT Set To 1	-	-	-	-	0	1	-	-
C-XMT Set To A	-	-	-	-	1	0	-	-
C-XMT Set To B	-	-	-	-	1	1	-	-
D-XMT Set To 0	-	-	-	-	-	-	0	0
D-XMT Set To 1	-	-	-	-	-	-	0	1
D-XMT Set To A	-	-	-	-	-	-	1	0
D-XMT Set To B	-	-	-	-	-	-	1	1

Interface Selection Register

The interface selection register allows the user to select specific interface ports for different interface applications. Writing to 0x28 a 00hex inactivates the analog port.

ISR Settings

Read @ 0x68

Write @ 0x28

Function	Bit Number								Hex
	7	6	5	4	3	2	1	0	
Inactive	0	0	0	0	0	0	0	0	0x00
FXO-LS	0	0	0	0	0	0	0	1	0x01
FXS-LS	0	0	0	0	0	0	1	0	0x02
FXO-RB	0	0	0	0	0	0	1	1	0x03
FXS-RB	0	0	0	0	0	1	0	0	0x04
FXO-GS	0	0	0	0	0	1	0	1	0x05
FXS-GS	0	0	0	0	0	1	1	0	0x06
DPO	0	0	0	0	0	1	1	1	0x07
DPT	0	0	0	0	1	0	0	0	0x08
2-W, TO	0	0	0	0	1	0	0	1	0x09
2-W, E&M, I	0	0	0	0	1	0	1	0	0x0A
2-W, E&M, II	0	0	0	0	1	0	1	1	0x0B
2-W, E&M, III	0	0	0	0	1	1	0	0	0x0C
2-W, E&M, IV	0	0	0	0	1	1	0	1	0x0D
2-W, E&M, V	0	0	0	0	1	1	1	0	0x0E
2-W, PLR, I	0	0	0	0	1	1	1	1	0x0F
2-W, PLR, II	0	0	0	1	0	0	0	0	0x10
2-W, PLR, III	0	0	0	1	0	0	0	1	0x11
2-W, PLR, IV	0	0	0	1	0	0	1	0	0x12
2-W, PLR, V	0	0	0	1	0	0	1	1	0x13
4-W, ETO	0	0	0	1	0	1	0	0	0x14
4-W, E&M, I	0	0	0	1	0	1	0	1	0x15
4-W, E&M, II	0	0	0	1	0	1	1	0	0x16
4-W, E&M, III	0	0	0	1	0	1	1	1	0x17
4-W, E&M, IV	0	0	0	1	1	0	0	0	0x18
4-W, E&M, V	0	0	0	1	1	0	0	1	0x19
4-W, PLR, I	0	0	0	1	1	0	1	0	0x1A
4-W, PLR, II	0	0	0	1	1	0	1	1	0x1B
4-W, PLR, III	0	0	0	1	1	1	0	0	0x1C
4-W, PLR, IV	0	0	0	1	1	1	0	1	0x1D
4-W, PLR, V	0	0	0	1	1	1	1	0	0x1E
Not Assigned	0	0	0	1	1	1	1	1	0x1F
Not Assigned	/	/	/	/	/	/	/	/	To
Not Assigned	1	1	1	1	1	1	1	1	0xFF

Ring Pattern Register

The ring pattern register allows the user to select specific alerting patterns for the FXS ports. Standard pre-loaded ringing patterns may be selected:

- DA type 1 code 1 (2.0 s on, 4.0 s off)
- DA type 1 code 2 (1.0 s on, 1.0 s off, 1.0 s on, 3.0 s off)
- DA type 2 (0.8 s on, 0.4 s off, 0.8 s on, 4.0 s off)
- DA type 3 (0.4 s on, 0.2 s off, 0.4 s on, 0.2 s off, 0.8 s on, 4.0 s off)

The ring pattern repeats every 6 seconds. Custom ringing patterns may be created by selecting constant ringing and turning the B-RCV CAS bit on and off to start and stop the individual ring burst.

RPR SETTINGS

Read @ 0x69

Write @ 0x29

Function	Bit Number								Hex
	7	6	5	4	3	2	1	0	
Pattern DA1C1	0	0	0	0	0	0	0	0	0x00
Pattern DA1C2	0	0	0	0	0	0	0	1	0x01
Pattern DA2	0	0	0	0	0	0	1	0	0x02
Pattern DA3	0	0	0	0	0	0	1	1	0x03
Constant Ringing	0	0	0	0	0	1	0	0	0x04
Not Assigned	0	0	0	0	0	1	0	1	0x05
Not Assigned	/	/	/	/	/	/	/	/	To
Not Assigned	1	1	1	1	1	1	1	1	0xFF

Ring Frequency Register

The ring frequency register allows the selection of specific ring generation frequencies for the FXS ports.

RFR SETTINGS:

Read @ 0x6A **Write @ 0x2A**

Function	Bit Number									Ring Frequency in Hz +/- 1%
	7	6	5	4	3	2	1	0	Hex	
Not Assigned	0	0	0	0	0	0	0	0	0x00	-
Not Assigned	\	\	\	\	\	\	\	\	To	-
Not Assigned	0	0	0	0	1	1	1	0	0x0E	-
15 ms	0	0	0	0	1	1	1	1	0x0F	66.67
16 ms	0	0	0	1	0	0	0	0	0x10	62.50
17 ms	0	0	0	1	0	0	0	1	0x11	58.82
18 ms	0	0	0	1	0	0	1	0	0x12	55.56
19 ms	0	0	0	1	0	0	1	1	0x13	52.63
20 ms	0	0	0	1	0	1	0	0	0x14	50.00
21 ms	0	0	0	1	0	1	0	1	0x15	47.62
22 ms	0	0	0	1	0	1	1	0	0x16	45.45
23 ms	0	0	0	1	0	1	1	1	0x17	43.48
24 ms	0	0	0	1	1	0	0	0	0x18	41.67
25 ms	0	0	0	1	1	0	0	1	0x19	40.00
26 ms	0	0	0	1	1	0	1	0	0x1A	38.46
27 ms	0	0	0	1	1	0	1	1	0x1B	37.04
28 ms	0	0	0	1	1	1	0	0	0x1C	35.71
29 ms	0	0	0	1	1	1	0	1	0x1D	34.48
30 ms	0	0	0	1	1	1	1	0	0x1E	33.33
31 ms	0	0	0	1	1	1	1	1	0x1F	32.26
32 ms	0	0	1	0	0	0	0	0	0x20	31.25
33 ms	0	0	1	0	0	0	0	1	0x21	30.30
34 ms	0	0	1	0	0	0	1	0	0x22	29.41
35 ms	0	0	1	0	0	0	1	1	0x23	28.57
36 ms	0	0	1	0	0	1	0	0	0x24	27.78
37 ms	0	0	1	0	0	1	0	1	0x25	27.03
38 ms	0	0	1	0	0	1	1	0	0x26	26.32
39 ms	0	0	1	0	0	1	1	1	0x27	25.64
40 ms	0	0	1	0	1	0	0	0	0x28	25.00
41 ms	0	0	1	0	1	0	0	1	0x29	24.39
42 ms	0	0	1	0	1	0	1	0	0x2A	23.81
43 ms	0	0	1	0	1	0	1	1	0x2B	23.26
44 ms	0	0	1	0	1	1	0	0	0x2C	22.73
45 ms	0	0	1	0	1	1	0	1	0x2D	22.22
46 ms	0	0	1	0	1	1	1	0	0x2E	21.74
47 ms	0	0	1	0	1	1	1	1	0x2F	21.28
48 ms	0	0	1	1	0	0	0	0	0x30	20.83
49 ms	0	0	1	1	0	0	0	1	0x31	20.41
50 ms	0	0	1	1	0	0	1	0	0x32	20.00
51 ms	0	0	1	1	0	0	1	1	0x33	19.61
52 ms	0	0	1	1	0	1	0	0	0x34	19.23
53 ms	0	0	1	1	0	1	0	1	0x35	18.87
54 ms	0	0	1	1	0	1	1	0	0x36	18.52
55 ms	0	0	1	1	0	1	1	1	0x37	18.18
56 ms	0	0	1	1	1	0	0	0	0x38	17.86
57 ms	0	0	1	1	1	0	0	1	0x39	17.54
58 ms	0	0	1	1	1	0	1	0	0x3A	17.24
59 ms	0	0	1	1	1	0	1	1	0x3B	16.95
60 ms	0	0	1	1	1	1	0	0	0x3C	16.67
61 ms	0	0	1	1	1	1	0	1	0x3D	16.39
62 ms	0	0	1	1	1	1	1	0	0x3E	16.13
Not Assigned	0	0	1	1	1	1	1	1	0x3F	-
Not Assigned	\	\	\	\	\	\	\	\	To	-
Not Assigned	1	1	1	1	1	1	1	1	0xFF	-

Ring Voltage Register

The ring voltage register allows the user to select specific ring generation voltages for the FXS ports.

RVR SETTINGS

Read @ 0x6B **Write @ 0x2B**

Function	Bit Number									Ring Voltage in Vrms +/- 5% @ no Load
	7	6	5	4	3	2	1	0	Hex	
Ring Voltage Setting Mid+0	0	0	0	0	0	0	0	0	0x00	51.7
Ring Voltage Setting Mid+1	0	0	0	0	0	0	0	1	0x01	52.6
Ring Voltage Setting Mid+2	0	0	0	0	0	0	1	0	0x02	53.5
Ring Voltage Setting Mid+3	0	0	0	0	0	0	1	1	0x03	54.4
Ring Voltage Setting Mid+4	0	0	0	0	0	1	0	0	0x04	55.3
Ring Voltage Setting Mid+5	0	0	0	0	0	1	0	1	0x05	56.2
Ring Voltage Setting Mid+6	0	0	0	0	0	1	1	0	0x06	57.0
Ring Voltage Setting Mid+7	0	0	0	0	0	1	1	1	0x07	57.9
Ring Voltage Setting Mid+8	0	0	0	0	1	0	0	0	0x08	58.8
Ring Voltage Setting Mid+9	0	0	0	0	1	0	0	1	0x09	59.5
Ring Voltage Setting Mid+10	0	0	0	0	1	0	1	0	0x0A	60.4
Ring Voltage Setting Mid+11	0	0	0	0	1	0	1	1	0x0B	61.3
Ring Voltage Setting Mid+12	0	0	0	0	1	1	0	0	0x0C	62.2
Ring Voltage Setting Mid+13	0	0	0	0	1	1	0	1	0x0D	63.1
Ring Voltage Setting Mid+14	0	0	0	0	1	1	1	0	0x0E	64.0
Ring Voltage Setting Mid+15	0	0	0	0	1	1	1	1	0x0F	64.9
Ring Voltage Setting Mid+16	0	0	0	1	0	0	0	0	0x10	65.8
Ring Voltage Setting Mid+17	0	0	0	1	0	0	0	1	0x11	66.7
Ring Voltage Setting Mid+18	0	0	0	1	0	0	1	0	0x12	67.6
Ring Voltage Setting Mid+19	0	0	0	1	0	0	1	1	0x13	68.5
Ring Voltage Setting Mid+20	0	0	0	1	0	1	0	0	0x14	69.4
Ring Voltage Setting Mid+21	0	0	0	1	0	1	0	1	0x15	70.3
Ring Voltage Setting Min+22	0	0	0	1	0	1	1	0	0x16	71.2
Ring Voltage Setting Min+23	0	0	0	1	0	1	1	1	0x17	72.0
Ring Voltage Setting Min+24	0	0	0	1	1	0	0	0	0x18	72.9
Ring Voltage Setting Min+25	0	0	0	1	1	0	0	1	0x19	73.8
Ring Voltage Setting Min+26	0	0	0	1	1	0	1	0	0x1A	74.7
Ring Voltage Setting Min+27	0	0	0	1	1	0	1	1	0x1B	75.6
Ring Voltage Setting Min+28	0	0	0	1	1	1	0	0	0x1C	76.5
Ring Voltage Setting Min+29	0	0	0	1	1	1	0	1	0x1D	77.3
Ring Voltage Setting Min+30	0	0	0	1	1	1	1	0	0x1E	78.3
Ring Voltage Setting Min+31	0	0	0	1	1	1	1	1	0x1F	79.1
Ring Voltage Setting Min+32	0	0	1	0	0	0	0	0	0x20	23.6
Ring Voltage Setting Min+33	0	0	1	0	0	0	0	1	0x21	24.4
Ring Voltage Setting Min+34	0	0	1	0	0	0	1	0	0x22	25.2
Ring Voltage Setting Mid+35	0	0	1	0	0	0	1	1	0x23	26.1
Ring Voltage Setting Mid+36	0	0	1	0	0	1	0	0	0x24	26.9
Ring Voltage Setting Mid+37	0	0	1	0	0	1	0	1	0x25	27.8
Ring Voltage Setting Mid+38	0	0	1	0	0	1	1	0	0x26	28.6
Ring Voltage Setting Mid+39	0	0	1	0	0	1	1	1	0x27	29.5
Ring Voltage Setting Mid+40	0	0	1	0	1	0	0	0	0x28	30.4
Ring Voltage Setting Mid+41	0	0	1	0	1	0	0	1	0x29	31.2
Ring Voltage Setting Mid+42	0	0	1	0	1	0	1	0	0x2A	32.1
Ring Voltage Setting Mid+43	0	0	1	0	1	0	1	1	0x2B	33.0
Ring Voltage Setting Mid+44	0	0	1	0	1	1	0	0	0x2C	33.9
Ring Voltage Setting Mid+45	0	0	1	0	1	1	0	1	0x2D	34.7
Ring Voltage Setting Mid+46	0	0	1	0	1	1	1	0	0x2E	35.6
Ring Voltage Setting Mid+47	0	0	1	0	1	1	1	1	0x2F	36.5
Ring Voltage Setting Mid+48	0	0	1	1	0	0	0	0	0x30	37.4
Ring Voltage Setting Mid+49	0	0	1	1	0	0	0	1	0x31	38.3
Ring Voltage Setting Mid+50	0	0	1	1	0	0	1	0	0x32	39.2
Ring Voltage Setting Mid+51	0	0	1	1	0	0	1	1	0x33	40.0

Continued from previous page:

Function	Bit Number								Ring Voltage in Vrms +/- 5% @ no Load
	7	6	5	4	3	2	1	0	Hex
Ring Voltage Setting Mid+52	0	0	1	1	0	1	0	0	0x34	40.9
Ring Voltage Setting Mid+53	0	0	1	1	0	1	0	1	0x35	41.8
Ring Voltage Setting Mid+54	0	0	1	1	0	1	1	0	0x36	42.6
Ring Voltage Setting Mid+55	0	0	1	1	0	1	1	1	0x37	43.5
Ring Voltage Setting Mid+56	0	0	1	1	1	0	0	0	0x38	44.4
Ring Voltage Setting Mid+57	0	0	1	1	1	0	0	1	0x39	45.3
Ring Voltage Setting Mid+58	0	0	1	1	1	0	1	0	0x3A	46.2
Ring Voltage Setting Mid+59	0	0	1	1	1	0	1	1	0x3B	47.1
Ring Voltage Setting Mid+60	0	0	1	1	1	1	0	0	0x3C	48.0
Ring Voltage Setting Mid+61	0	0	1	1	1	1	0	1	0x3D	48.9
Ring Voltage Setting Mid+62	0	0	1	1	1	1	1	0	0x3E	49.8
Ring Voltage Setting Mid+63	0	0	1	1	1	1	1	1	0x3F	50.7
Ring Voltage Set to zero Vac	0	1	0	0	0	0	0	0	0x40	00.00
Not Assigned	0	1	0	0	0	0	1	1	0x41	-
Not Assigned	/	/	/	/	/	/	/	/	To	-
Not Assigned	1	1	1	1	1	1	1	1	0xFF	-

Telecom Voltage Register

The telecom voltage register allows the user to select specific telecom voltages for the FXS, DPO, E&M and PLR ports.

TVR SETTINGS

Read @ 0x6C Write @ 0x2C

Function	Bit Number									Telecom Voltage in Vdc +/- 5% @ no Load
	7	6	5	4	3	2	1	0	Hex	
Telecom Voltage Setting Mid+0	0	0	0	0	0	0	0	0	0x00	58.0
Telecom Voltage Setting Mid+1	0	0	0	0	0	0	0	1	0x01	58.8
Telecom Voltage Setting Mid+2	0	0	0	0	0	0	1	0	0x02	59.7
Telecom Voltage Setting Mid+3	0	0	0	0	0	0	1	1	0x03	60.5
Telecom Voltage Setting Mid+4	0	0	0	0	0	1	0	0	0x04	61.6
Telecom Voltage Setting Mid+5	0	0	0	0	0	1	0	1	0x05	62.5
Telecom Voltage Setting Mid+6	0	0	0	0	0	1	1	0	0x06	63.5
Telecom Voltage Setting Mid+7	0	0	0	0	0	1	1	1	0x07	64.3
Telecom Voltage Setting Mid+8	0	0	0	0	1	0	0	0	0x08	65.3
Telecom Voltage Setting Mid+9	0	0	0	0	1	0	0	1	0x09	66.2
Telecom Voltage Setting Mid+10	0	0	0	0	1	0	1	0	0x0A	67.1
Telecom Voltage Setting Mid+11	0	0	0	0	1	0	1	1	0x0B	68.0
Telecom Voltage Setting Mid+12	0	0	0	0	1	1	0	0	0x0C	68.9
Telecom Voltage Setting Mid+13	0	0	0	0	1	1	0	1	0x0D	69.8
Telecom Voltage Setting Mid+14	0	0	0	0	1	1	1	0	0x0E	70.7
Telecom Voltage Setting Mid+15	0	0	0	0	1	1	1	1	0x0F	71.5
Telecom Voltage Setting Mid+16	0	0	0	1	0	0	0	0	0x10	72.4
Telecom Voltage Setting Mid+17	0	0	0	1	0	0	0	1	0x11	73.3
Telecom Voltage Setting Mid+18	0	0	0	1	0	0	1	0	0x12	74.2
Telecom Voltage Setting Mid+19	0	0	0	1	0	0	1	1	0x13	75.0
Telecom Voltage Setting Mid+20	0	0	0	1	0	1	0	0	0x14	75.9
Telecom Voltage Setting Mid+21	0	0	0	1	0	1	0	1	0x15	76.8
Telecom Voltage Setting Min+22	0	0	0	1	0	1	1	0	0x16	77.7
Telecom Voltage Setting Min+23	0	0	0	1	0	1	1	1	0x17	78.6
Telecom Voltage Setting Min+24	0	0	0	1	1	0	0	0	0x18	79.5
Telecom Voltage Setting Min+25	0	0	0	1	1	0	0	1	0x19	80.3
Telecom Voltage Setting Min+26	0	0	0	1	1	0	1	0	0x1A	81.2
Telecom Voltage Setting Min+27	0	0	0	1	1	0	1	1	0x1B	82.1
Telecom Voltage Setting Min+28	0	0	0	1	1	1	0	0	0x1C	83.0
Telecom Voltage Setting Min+29	0	0	0	1	1	1	0	1	0x1D	83.9
Telecom Voltage Setting Min+30	0	0	0	1	1	1	1	0	0x1E	84.7
Telecom Voltage Setting Min+31	0	0	0	1	1	1	1	1	0x1F	85.5
Telecom Voltage Setting Min+32	0	0	1	0	0	0	0	0	0x20	28.6
Telecom Voltage Setting Min+33	0	0	1	0	0	0	0	1	0x21	29.5
Telecom Voltage Setting Min+34	0	0	1	0	0	0	1	0	0x22	30.4
Telecom Voltage Setting Mid+35	0	0	1	0	0	0	1	1	0x23	31.3
Telecom Voltage Setting Mid+36	0	0	1	0	0	1	0	0	0x24	32.3
Telecom Voltage Setting Mid+37	0	0	1	0	0	1	0	1	0x25	33.2
Telecom Voltage Setting Mid+38	0	0	1	0	0	1	1	0	0x26	34.1
Telecom Voltage Setting Mid+39	0	0	1	0	0	1	1	1	0x27	35.0
Telecom Voltage Setting Mid+40	0	0	1	0	1	0	0	0	0x28	36.0
Telecom Voltage Setting Mid+41	0	0	1	0	1	0	0	1	0x29	36.9
Telecom Voltage Setting Mid+42	0	0	1	0	1	0	1	0	0x2A	37.8
Telecom Voltage Setting Mid+43	0	0	1	0	1	0	1	1	0x2B	38.8
Telecom Voltage Setting Mid+44	0	0	1	0	1	1	0	0	0x2C	39.7
Telecom Voltage Setting Mid+45	0	0	1	0	1	1	0	1	0x2D	40.6
Telecom Voltage Setting Mid+46	0	0	1	0	1	1	1	0	0x2E	41.6
Telecom Voltage Setting Mid+47	0	0	1	0	1	1	1	1	0x2F	42.5
Telecom Voltage Setting Mid+48	0	0	1	1	0	0	0	0	0x30	43.4
Telecom Voltage Setting Mid+49	0	0	1	1	0	0	0	1	0x31	44.3
Telecom Voltage Setting Mid+50	0	0	1	1	0	0	1	0	0x32	45.2
Telecom Voltage Setting Mid+51	0	0	1	1	0	0	1	1	0x33	46.1

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Function	Bit Number									Telecom Voltage in Vdc +/- 5% @ no Load
	7	6	5	4	3	2	1	0	Hex	
Telecom Voltage Setting Mid+52	0	0	1	1	0	1	0	0	0x34	47.0
Telecom Voltage Setting Mid+53	0	0	1	1	0	1	0	1	0x35	47.9
Telecom Voltage Setting Mid+54	0	0	1	1	0	1	1	0	0x36	48.8
Telecom Voltage Setting Mid+55	0	0	1	1	0	1	1	1	0x37	49.7
Telecom Voltage Setting Mid+56	0	0	1	1	1	0	0	0	0x38	50.6
Telecom Voltage Setting Mid+57	0	0	1	1	1	0	0	1	0x39	51.5
Telecom Voltage Setting Mid+58	0	0	1	1	1	0	1	0	0x3A	52.4
Telecom Voltage Setting Mid+59	0	0	1	1	1	0	1	1	0x3B	53.3
Telecom Voltage Setting Mid+60	0	0	1	1	1	1	0	0	0x3C	54.3
Telecom Voltage Setting Mid+61	0	0	1	1	1	1	0	1	0x3D	55.1
Telecom Voltage Setting Mid+62	0	0	1	1	1	1	1	0	0x3E	56.0
Telecom Voltage Setting Mid+63	0	0	1	1	1	1	1	1	0x3F	56.9
Telecom Voltage Set to zero Vac	0	1	0	0	0	0	0	0	0x40	00.00
Not Assigned	0	1	0	0	0	0	0	1	0x41	-
Not Assigned	/	/	/	/	/	/	/	/	To	-
Not Assigned	1	X	X	X	X	X	X	X	0xFF	-

Upper Ring Frequency Detection Limit Register

The upper ring frequency detection limit register allows the user to select the detection limit for the upper ring frequencies for the FXO port operation. When the incoming ringing frequency is greater than the selected frequency then the ring detector will not trigger a response and the received ringing is being ignored.

RING FREQUENCY DETECTION RANGE

LRFDLR	Ringing	URFDLR
15.87 Hz to 71.42 Hz	16.13 Hz to 66.67 Hz	15.87 Hz to 71.42 Hz
Reject Range	Accept Range	Reject Range

URFDLR SETTINGS

Read @ 0x6D

Write @ 0x2D

Function	Bit Number									Ring Frequency in Hz +/- 1%
	7	6	5	4	3	2	1	0	Hex	
Not Assigned	0	0	0	0	0	0	0	0	0x00	71.42
Not Assigned	/	/	/	/	/	/	/	/	To	71.42
Not Assigned	0	0	0	0	1	1	0	1	0x0D	71.42
14 ms	0	0	0	0	1	1	1	0	0x0E	71.42
15 ms	0	0	0	0	1	1	1	1	0x0F	66.67
16 ms	0	0	0	1	0	0	0	0	0x10	62.50
17 ms	0	0	0	1	0	0	0	1	0x11	58.82
18 ms	0	0	0	1	0	0	1	0	0x12	55.56
19 ms	0	0	0	1	0	0	1	1	0x13	52.63
20 ms	0	0	0	1	0	1	0	0	0x14	50.00
21 ms	0	0	0	1	0	1	0	1	0x15	47.62
22 ms	0	0	0	1	0	1	1	0	0x16	45.45
23 ms	0	0	0	1	0	1	1	1	0x17	43.48
24 ms	0	0	0	1	1	0	0	0	0x18	41.67
25 ms	0	0	0	1	1	0	0	1	0x19	40.00
26 ms	0	0	0	1	1	0	1	0	0x1A	38.46
27 ms	0	0	0	1	1	0	1	1	0x1B	37.04
28 ms	0	0	0	1	1	1	0	0	0x1C	35.71
29 ms	0	0	0	1	1	1	0	1	0x1D	34.48
30 ms	0	0	0	1	1	1	1	0	0x1E	33.33
31 ms	0	0	0	1	1	1	1	1	0x1F	32.26
32 ms	0	0	1	0	0	0	0	0	0x20	31.25
33 ms	0	0	1	0	0	0	0	1	0x21	30.30
34 ms	0	0	1	0	0	0	1	0	0x22	29.41
35 ms	0	0	1	0	0	0	1	1	0x23	28.57
36 ms	0	0	1	0	0	1	0	0	0x24	27.78
37 ms	0	0	1	0	0	1	0	1	0x25	27.03
38 ms	0	0	1	0	0	1	1	0	0x26	26.32
39 ms	0	0	1	0	0	1	1	1	0x27	25.64
40 ms	0	0	1	0	1	0	0	0	0x28	25.00
41 ms	0	0	1	0	1	0	0	1	0x29	24.39
42 ms	0	0	1	0	1	0	1	0	0x2A	23.81
43 ms	0	0	1	0	1	0	1	1	0x2B	23.26
44 ms	0	0	1	0	1	1	0	0	0x2C	22.73
45 ms	0	0	1	0	1	1	0	1	0x2D	22.22
46 ms	0	0	1	0	1	1	1	0	0x2E	21.74
47 ms	0	0	1	0	1	1	1	1	0x2F	21.28
48 ms	0	0	1	1	0	0	0	0	0x30	20.83
49 ms	0	0	1	1	0	0	0	1	0x31	20.41
50 ms	0	0	1	1	0	0	1	0	0x32	20.00
51 ms	0	0	1	1	0	0	1	1	0x33	19.61
52 ms	0	0	1	1	0	1	0	0	0x34	19.23
53 ms	0	0	1	1	0	1	0	1	0x35	18.87

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Function	Bit Number									Ring Frequency in Hz +/- 1%
	7	6	5	4	3	2	1	0	Hex	
54 ms	0	0	1	1	0	1	1	0	0x36	18.52
55 ms	0	0	1	1	0	1	1	1	0x37	18.18
56 ms	0	0	1	1	1	0	0	0	0x38	17.86
57 ms	0	0	1	1	1	0	0	1	0x39	17.54
58 ms	0	0	1	1	1	0	1	0	0x3A	17.24
59 ms	0	0	1	1	1	0	1	1	0x3B	16.95
60 ms	0	0	1	1	1	1	0	0	0x3C	16.67
61 ms	0	0	1	1	1	1	0	1	0x3D	16.39
62 ms	0	0	1	1	1	1	1	0	0x3E	16.13
63 ms	0	0	1	1	1	1	1	1	0x3F	15.87
Not Assigned	0	1	0	0	0	0	0	0	0x40	15.87
Not Assigned	/	/	/	/	/	/	/	/	To	15.87
Not Assigned	1	1	1	1	1	1	1	1	0xFF	15.87

Lower Ring Frequency Detection Limit Register

The lower ring frequency detection limit register allows the user to select the detection limit for the lower ring frequencies for the FXS port operation. When the incoming ringing frequency is less than the selected frequency then the ring detector will not trigger a response and the received ring signal is being ignored.

RING FREQUENCY DETECTION RANGE EXAMPLE

LRFDLR	Ringing	URFDLR
15.87 Hz to 25.00 Hz	25.64 Hz to 38.46 Hz	40.00 Hz to 71.42 Hz
Reject	Accept	Reject

LRFDLR SETTINGS

Read @ 0x6E
Write @ 0x2E

Function	Bit Number									Ring Frequency in Hz +/- 1%
	7	6	5	4	3	2	1	0	Hex	
Not Assigned	-	-	0	0	0	0	0	0	0x00	-
Not Assigned	/	/	/	/	/	/	/	/	To	-
Not Assigned	-	-	0	0	1	1	0	1	0x0D	-
14 ms	-	-	0	0	1	1	1	0	0x0E	71.42
15 ms	-	-	0	0	1	1	1	1	0x0F	66.67
16 ms	-	-	0	1	0	0	0	0	0x10	62.50
17 ms	-	-	0	1	0	0	0	1	0x11	58.82
18 ms	-	-	0	1	0	0	1	0	0x12	55.56
19 ms	-	-	0	1	0	0	1	1	0x13	52.63
20 ms	-	-	0	1	0	1	0	0	0x14	50.00
21 ms	-	-	0	1	0	1	0	1	0x15	47.62
22 ms	-	-	0	1	0	1	1	0	0x16	45.45
23 ms	-	-	0	1	0	1	1	1	0x17	43.48
24 ms	-	-	0	1	1	0	0	0	0x18	41.67
25 ms	-	-	0	1	1	0	0	1	0x19	40.00
26 ms	-	-	0	1	1	0	1	0	0x1A	38.46
27 ms	-	-	0	1	1	0	1	1	0x1B	37.04
28 ms	-	-	0	1	1	1	0	0	0x1C	35.71
29 ms	-	-	0	1	1	1	0	1	0x1D	34.48
30 ms	-	-	0	1	1	1	1	0	0x1E	33.33
31 ms	-	-	0	1	1	1	1	1	0x1F	32.26
32 ms	-	-	1	0	0	0	0	0	0x20	31.25
33 ms	-	-	1	0	0	0	0	1	0x21	30.30
34 ms	-	-	1	0	0	0	1	0	0x22	29.41
35 ms	-	-	1	0	0	0	1	1	0x23	28.57
36 ms	-	-	1	0	0	1	0	0	0x24	27.78
37 ms	-	-	1	0	0	1	0	1	0x25	27.03
38 ms	-	-	1	0	0	1	1	0	0x26	26.32
39 ms	-	-	1	0	0	1	1	1	0x27	25.64
40 ms	-	-	1	0	1	0	0	0	0x28	25.00
41 ms	-	-	1	0	1	0	0	1	0x29	24.39
42 ms	-	-	1	0	1	0	1	0	0x2A	23.81
43 ms	-	-	1	0	1	0	1	1	0x2B	23.26
44 ms	-	-	1	0	1	1	0	0	0x2C	22.73
45 ms	-	-	1	0	1	1	0	1	0x2D	22.22
46 ms	-	-	1	0	1	1	1	0	0x2E	21.74
47 ms	-	-	1	0	1	1	1	1	0x2F	21.28
48 ms	-	-	1	1	0	0	0	0	0x30	20.83
49 ms	-	-	1	1	0	0	0	1	0x31	20.41
50 ms	-	-	1	1	0	0	1	0	0x32	20.00
51 ms	-	-	1	1	0	0	1	1	0x33	19.61
52 ms	-	-	1	1	0	1	0	0	0x34	19.23

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Function	Bit Number									Ring Frequency in Hz +/- 1%
	7	6	5	4	3	2	1	0	Hex	
53 ms	-	-	1	1	0	1	0	1	0x35	18.87
54 ms	-	-	1	1	0	1	1	0	0x36	18.52
55 ms	-	-	1	1	0	1	1	1	0x37	18.18
56 ms	-	-	1	1	1	0	0	0	0x38	17.86
57 ms	-	-	1	1	1	0	0	1	0x39	17.54
58 ms	-	-	1	1	1	0	1	0	0x3A	17.24
59 ms	-	-	1	1	1	0	1	1	0x3B	16.95
60 ms	-	-	1	1	1	1	0	0	0x3C	16.67
61 ms	-	-	1	1	1	1	0	1	0x3D	16.39
62 ms	-	-	1	1	1	1	1	0	0x3E	16.13
63 ms	0	0	1	1	1	1	1	1	0x3F	15.87
Not Assigned	0	1	0	0	0	0	0	0	0x40	-
Not Assigned	\	\	\	\	\	\	\	\	To	-
Not Assigned	1	1	1	1	1	1	1	1	0xFF	-

Special Function Register

The special function register allows the selection of telephony functions that are optional to the operation of the selected telephony interface. The following special functions are currently supported:

- Caller ID Pass-Through
- Pass Loop Disconnect
- AutoWINK ™
- Flash-to-Answer
- Originate Loop Disconnect

SFR SETTINGS

Read @ 0x6F

Write @ 0x2F

Function	Bit Number							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	0	-	-	-	-	-	-	-
Reserved	-	0	-	-	-	-	-	-
Reserved	-	-	0	-	-	-	-	-
Originate FXS Loop Disconnect Disabled	-	-	-	0	-	-	-	-
Originate FXS Loop Disconnect Enabled	-	-	-	1	-	-	-	-
FXS Flash-to-Answer Supervision Disabled	-	-	-	-	0	-	-	-
FXS Flash-to-Answer Supervision Enabled	-	-	-	-	1	-	-	-
FXS autoWINK Operation Disabled	-	-	-	-	-	0	-	-
FXS autoWINK Operation Enabled	-	-	-	-	-	1	-	-
Pass FXS/FXO Loop Disconnect Disabled	-	-	-	-	-	-	0	-
Pass FXS/FXO Loop Disconnect Enabled	-	-	-	-	-	-	1	-
Caller ID Pass-Through Disabled	-	-	-	-	-	-	-	0
Caller ID Pass-Through Enabled	-	-	-	-	-	-	-	1

Codec Control Register

The codec control register allows the user to select the specific operation for the digital port of the module.

A TDM master clock must be provided to the module for operation of the TDM, filter coding/decoding functions. The BCLK frequency must be 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz.

Bits 4 and 5 in the CCR permit the selection of u-law coding or A-law coding, with or without even bit inversion.

The analog loopback mode is entered by setting the AL and DL bits in the CCR. In the analog loopback mode, the analog transmit input is isolated from the input and internally passed to the analog output, forming a loop from the TDM input (DR) back to TDM output (DX). The programmed settings of transmit and receive gains remain unchanged. Care must be taken to ensure that overload levels are not exceeded anywhere in the loop. It is recommended that the hybrid-balance filter be disabled during analog loopback.

The digital loopback mode is entered by setting the AL and DL bits in the CCR. This mode provides another level of path verification by enabling data written into receive TDM register to be read back from that register in any transmit time-slot at DX. In digital loopback mode, the decoder remains functional and outputs signals at the analog port. If this is undesirable, receive output can be disabled by programming receive gain register to all 0s.

The module can operate in either fixed time-slot or time-slot assignment modes for selecting transmit and receive TDM time-slots. Following power-up, the module is automatically in non-delayed timing mode, in which the time-slot always begins with the leading (rising) edge of the frame-sync input (FS). Time-slot assignment can only be used with delayed-data timing. The internal time-slot counter can be used to access any time-slot in a frame by using the frame- sync (FS) input as a marker pulse for the beginning of transmit and receive time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction. The last 6 bits of the second byte indicate the selected time-slot from 0 to 63 using a straight binary notation. A new assignment becomes active on the second frame following the end of the following the end of the chip select (CS) for the second control byte. Time-slot assignment mode requires that the FS pulse must conform to the delayed-data-timing format.

CCR SETTINGS

Read @ 0x70

Write @ 0x30

Function	Bit Number and Name							
	7	6	5	4	3	2	1	0
Reserved	0	0	-	-	-	-	-	-
BCLK = 1.536 MHz or 1.544 MHz	0	1	-	-	-	-	-	-
BCLK = 2.048 MHz*	1	0	-	-	-	-	-	-
BCLK = 4.096 MHz	1	1	-	-	-	-	-	-
u-Law*	-	-	0	X	-	-	-	-
A-Law, Including Even Bit Inversion	-	-	1	0	-	-	-	-
A-Law, No Even Bit Inversion	-	-	1	1	-	-	-	-
Delayed Data Timing	-	-	-	-	0	-	-	-
Non-delayed Data Timing*	-	-	-	-	1	-	-	-
Normal Operation*	-	-	-	-	-	0	0	-
Digital Loopback (DL)	-	-	-	-	-	1	X	-
Analog Loopback (AL)	-	-	-	-	-	0	1	-
Power Amp Enabled in Shut-down	-	-	-	-	-	-	-	0
Power Amp Disabled in Shut-down*	-	-	-	-	-	-	-	1

***Note:* State at power-up *initialization* (bit 4 = 0)**

Receive Gain Register

The receive gain register allows the user to select the gain or loss between the digital interface port and the analog interface port.

Receive gain can be programmed in 0.1 dB steps from –17.3 dB to +2.1 dB. This corresponds to a range of 0 dBm0 levels at the analog output between 0.987 Vrms and 0.106 Vrms driving into 600-Ohm termination impedance.

Telephony signals are usually referenced to a 0-dB TLP (transmission level point) level at the digital signal cross connect (DSX) interface. In this case, the digital port is considered the 0 dB TLP (0 dezi Bell level referenced to the zero transmission level point)

To set the receive gain, determine the gain required of the module in order to achieve the desired TLP at the TDM interface. (Usually 0 dBm or –4.0 dBm)

To convert the signal gain to the analog output voltage, use the following formula:

$$V = 0.7746 \text{ Vrms} * 10^{(Gr/20)}$$

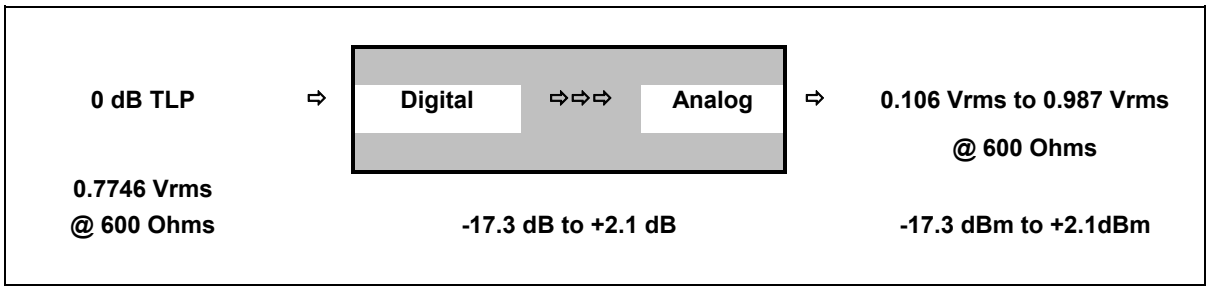
To convert the analog output voltage to the signal gain, use the following formula:

$$Gr = 20 * \log_{10} (V/0.7746 \text{ Vrms})$$

For example, the factory default setting for transmit gain is +2.0 dB. A signal with a level of 0 dBm presented at the digital input produces an output of 2 dBm at the analog output.

When attenuated by 17.3 dB a 0-dBm0 level at the digital input produces a 0.106 Vrms signal into 600 Ohms at the analog output.

RECEIVE PATH



RGR Settings [0x00 to 0x3F]

Read @ 0x74 Write @ 0x34

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
0	0	0	0	0	0	0	0	0x00	0.000	-∞
0	0	0	0	0	0	0	1	0x01	0.106	-24.3
0	0	0	0	0	0	1	0	0x02	0.107	-24.2
0	0	0	0	0	0	1	1	0x03	0.108	-24.1
0	0	0	0	0	1	0	0	0x04	0.109	-24.0
0	0	0	0	0	1	0	1	0x05	0.111	-23.9
0	0	0	0	0	1	1	0	0x06	0.112	-23.8
0	0	0	0	0	1	1	1	0x07	0.113	-23.7
0	0	0	0	1	0	0	0	0x08	0.115	-23.6
0	0	0	0	1	0	0	1	0x09	0.116	-23.5
0	0	0	0	1	0	1	0	0x0A	0.117	-23.4
0	0	0	0	1	0	1	1	0x0B	0.119	-23.3
0	0	0	0	1	1	0	0	0x0C	0.120	-23.2
0	0	0	0	1	1	0	1	0x0D	0.121	-23.1
0	0	0	0	1	1	1	0	0x0E	0.123	-23.0
0	0	0	0	1	1	1	1	0x0F	0.124	-22.9
0	0	0	1	0	0	0	0	0x10	0.126	-22.8
0	0	0	1	0	0	0	1	0x11	0.127	-22.7
0	0	0	1	0	0	1	0	0x12	0.129	-22.6
0	0	0	1	0	0	1	1	0x13	0.130	-22.5
0	0	0	1	0	1	0	0	0x14	0.132	-22.4
0	0	0	1	0	1	0	1	0x15	0.133	-22.3
0	0	0	1	0	1	1	0	0x16	0.135	-22.2
0	0	0	1	0	1	1	1	0x17	0.136	-22.1
0	0	0	1	1	0	0	0	0x18	0.138	-22.0
0	0	0	1	1	0	0	1	0x19	0.139	-21.9
0	0	0	1	1	0	1	0	0x1A	0.141	-21.8
0	0	0	1	1	0	1	1	0x1B	0.143	-21.7
0	0	0	1	1	1	0	0	0x1C	0.144	-21.6
0	0	0	1	1	1	0	1	0x1D	0.146	-21.5
0	0	0	1	1	1	1	0	0x1E	0.148	-21.4
0	0	0	1	1	1	1	1	0x1F	0.149	-21.3
0	0	0	0	0	0	0	0	0x20	0.151	-21.2
0	0	0	0	0	0	0	1	0x21	0.153	-21.1
0	0	0	0	0	0	1	0	0x22	0.155	-21.0
0	0	0	0	0	0	1	1	0x23	0.156	-20.9
0	0	0	0	0	1	0	0	0x24	0.158	-20.8
0	0	0	0	0	1	0	1	0x25	0.160	-20.7
0	0	0	0	0	1	1	0	0x26	0.162	-20.6
0	0	0	0	0	1	1	1	0x27	0.164	-20.5
0	0	0	0	1	0	0	0	0x28	0.166	-20.4
0	0	0	0	1	0	0	1	0x29	0.168	-20.3
0	0	0	0	1	0	1	0	0x2A	0.169	-20.2
0	0	0	0	1	0	1	1	0x2B	0.171	-20.1
0	0	0	0	1	1	0	0	0x2C	0.173	-20.0
0	0	0	0	1	1	0	1	0x2D	0.175	-19.9
0	0	0	0	1	1	1	0	0x2E	0.177	-19.8
0	0	0	0	1	1	1	1	0x2F	0.180	-19.7
0	0	0	1	0	0	0	0	0x30	0.182	-19.6
0	0	0	1	0	0	0	1	0x31	0.184	-19.5
0	0	0	1	0	0	1	0	0x32	0.186	-19.4
0	0	0	1	0	0	1	1	0x33	0.188	-19.3
0	0	0	1	0	1	0	0	0x34	0.190	-19.2
0	0	0	1	0	1	0	1	0x35	0.192	-19.1
0	0	0	1	0	1	1	0	0x36	0.195	-19.0
0	0	0	1	0	1	1	1	0x37	0.197	-18.9
0	0	0	1	1	0	0	0	0x38	0.199	-18.8
0	0	0	1	1	0	0	1	0x39	0.201	-18.7
0	0	0	1	1	0	1	0	0x3A	0.204	-18.6
0	0	0	1	1	0	1	1	0x3B	0.206	-18.5
0	0	0	1	1	1	0	0	0x3C	0.209	-18.4
0	0	0	1	1	1	0	1	0x3D	0.211	-18.3
0	0	0	1	1	1	1	0	0x3E	0.213	-18.2
0	0	0	1	1	1	1	1	0x3F	0.216	-18.1

RGR Settings [0x40 to 0x7F]

Read @ 0x74 Write @ 0x34

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
0	0	1	0	0	0	0	0	0x40	0.218	-18.0
0	0	1	0	0	0	0	1	0x41	0.221	-17.9
0	0	1	0	0	0	1	0	0x42	0.223	-17.8
0	0	1	0	0	0	1	1	0x43	0.226	-17.7
0	0	1	0	0	1	0	0	0x44	0.229	-17.6
0	0	1	0	0	1	0	1	0x45	0.231	-17.5
0	0	1	0	0	1	1	0	0x46	0.234	-17.4
0	0	1	0	0	1	1	1	0x47	0.237	-17.3
0	0	1	0	1	0	0	0	0x48	0.239	-17.2
0	0	1	0	1	0	0	1	0x49	0.242	-17.1
0	0	1	0	1	0	1	0	0x4A	0.245	-17.0
0	0	1	0	1	0	1	1	0x4B	0.248	-16.9
0	0	1	0	1	1	0	0	0x4C	0.251	-16.8
0	0	1	0	1	1	0	1	0x4D	0.254	-16.7
0	0	1	0	1	1	1	0	0x4E	0.257	-16.6
0	0	1	0	1	1	1	1	0x4F	0.259	-16.5
0	0	1	1	0	0	0	0	0x50	0.262	-16.4
0	0	1	1	0	0	0	1	0x51	0.266	-16.3
0	0	1	1	0	0	1	0	0x52	0.269	-16.2
0	0	1	1	0	0	1	1	0x53	0.272	-16.1
0	0	1	1	0	1	0	0	0x54	0.275	-16.0
0	0	1	1	0	1	0	1	0x55	0.278	-15.9
0	0	1	1	0	1	1	0	0x56	0.281	-15.8
0	0	1	1	0	1	1	1	0x57	0.285	-15.7
0	0	1	1	1	0	0	0	0x58	0.288	-15.6
0	0	1	1	1	0	0	1	0x59	0.291	-15.5
0	0	1	1	1	0	1	0	0x5A	0.295	-15.4
0	0	1	1	1	0	1	1	0x5B	0.298	-15.3
0	0	1	1	1	1	0	0	0x5C	0.301	-15.2
0	0	1	1	1	1	0	1	0x5D	0.305	-15.1
0	0	1	1	1	1	1	0	0x5E	0.308	-15.0
0	0	1	1	1	1	1	1	0x5F	0.312	-14.9
0	0	1	0	0	0	0	0	0x60	0.316	-14.8
0	0	1	0	0	0	0	1	0x61	0.319	-14.7
0	0	1	0	0	0	1	0	0x62	0.323	-14.6
0	0	1	0	0	0	1	1	0x63	0.327	-14.5
0	0	1	0	0	1	0	0	0x64	0.330	-14.4
0	0	1	0	0	1	0	1	0x65	0.334	-14.3
0	0	1	0	0	1	1	0	0x66	0.338	-14.2
0	0	1	0	0	1	1	1	0x67	0.342	-14.1
0	0	1	0	1	0	0	0	0x68	0.346	-14.0
0	0	1	0	1	0	0	1	0x69	0.350	-13.9
0	0	1	0	1	0	1	0	0x6A	0.354	-13.8
0	0	1	0	1	0	1	1	0x6B	0.358	-13.7
0	0	1	0	1	1	0	0	0x6C	0.362	-13.6
0	0	1	0	1	1	0	1	0x6D	0.367	-13.5
0	0	1	0	1	1	1	0	0x6E	0.371	-13.4
0	0	1	0	1	1	1	1	0x6F	0.375	-13.3
0	0	1	1	0	0	0	0	0x70	0.379	-13.2
0	0	1	1	0	0	0	1	0x71	0.384	-13.1
0	0	1	1	0	0	1	0	0x72	0.388	-13.0
0	0	1	1	0	0	1	1	0x73	0.393	-12.9
0	0	1	1	0	1	0	0	0x74	0.397	-12.8
0	0	1	1	0	1	0	1	0x75	0.402	-12.7
0	0	1	1	0	1	1	0	0x76	0.407	-12.6
0	0	1	1	0	1	1	1	0x77	0.411	-12.5
0	0	1	1	1	0	0	0	0x78	0.416	-12.4
0	0	1	1	1	0	0	1	0x79	0.421	-12.3
0	0	1	1	1	0	1	0	0x7A	0.426	-12.2
0	0	1	1	1	0	1	1	0x7B	0.431	-12.1
0	0	1	1	1	1	0	0	0x7C	0.436	-12.0
0	0	1	1	1	1	0	1	0x7D	0.441	-11.9
0	0	1	1	1	1	1	0	0x7E	0.446	-11.8
0	0	1	1	1	1	1	1	0x7F	0.451	-11.7

RGR Settings [0x80 to 0xBF]

Read @ 0x74 Write @ 0x34 ***0 dB receive path gain setting is 0xAE.***

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
0	1	0	0	0	0	0	0	0x80	0.456	-11.6
0	1	0	0	0	0	0	1	0x81	0.461	-11.5
0	1	0	0	0	0	1	0	0x82	0.467	-11.4
0	1	0	0	0	0	1	1	0x83	0.472	-11.3
0	1	0	0	0	1	0	0	0x84	0.478	-11.2
0	1	0	0	0	1	0	1	0x85	0.483	-11.1
0	1	0	0	0	1	1	0	0x86	0.489	-11.0
0	1	0	0	0	1	1	1	0x87	0.494	-10.9
0	1	0	0	1	0	0	0	0x88	0.500	-10.8
0	1	0	0	1	0	0	1	0x89	0.506	-10.7
0	1	0	0	1	0	1	0	0x8A	0.512	-10.6
0	1	0	0	1	0	1	1	0x8B	0.518	-10.5
0	1	0	0	1	1	0	0	0x8C	0.524	-10.4
0	1	0	0	1	1	0	1	0x8D	0.530	-10.3
0	1	0	0	1	1	1	0	0x8E	0.536	-10.2
0	1	0	0	1	1	1	1	0x8F	0.542	-10.1
0	1	0	1	0	0	0	0	0x90	0.548	-10.0
0	1	0	1	0	0	0	1	0x91	0.555	-9.9
0	1	0	1	0	0	1	0	0x92	0.561	-9.8
0	1	0	1	0	0	1	1	0x93	0.568	-9.7
0	1	0	1	0	1	0	0	0x94	0.574	-9.6
0	1	0	1	0	1	0	1	0x95	0.581	-9.5
0	1	0	1	0	1	1	0	0x96	0.588	-9.4
0	1	0	1	0	1	1	1	0x97	0.594	-9.3
0	1	0	1	1	0	0	0	0x98	0.601	-9.2
0	1	0	1	1	0	0	1	0x99	0.608	-9.1
0	1	0	1	1	0	1	0	0x9A	0.615	-9.0
0	1	0	1	1	0	1	1	0x9B	0.622	-8.9
0	1	0	1	1	1	0	0	0x9C	0.630	-8.8
0	1	0	1	1	1	0	1	0x9D	0.637	-8.7
0	1	0	1	1	1	1	0	0x9E	0.644	-8.6
0	1	0	1	1	1	1	1	0x9F	0.652	-8.5
1	0	1	0	0	0	0	0	0xA0	0.659	-8.4
1	0	1	0	0	0	0	1	0xA1	0.667	-8.3
1	0	1	0	0	0	1	0	0xA2	0.675	-8.2
1	0	1	0	0	0	1	1	0xA3	0.683	-8.1
1	0	1	0	0	1	0	0	0xA4	0.690	-8.0
1	0	1	0	0	1	0	1	0xA5	0.698	-7.9
1	0	1	0	0	1	1	0	0xA6	0.707	-7.8
1	0	1	0	0	1	1	1	0xA7	0.715	-7.7
1	0	1	0	1	0	0	0	0xA8	0.723	-7.6
1	0	1	0	1	0	0	1	0xA9	0.731	-7.5
1	0	1	0	1	0	1	0	0xAA	0.740	-7.4
1	0	1	0	1	0	1	1	0xAB	0.748	-7.3
1	0	1	0	1	1	0	0	0xAC	0.757	-7.2
1	0	1	0	1	1	0	1	0xAD	0.766	-7.1
1	0	1	0	1	1	1	0	0xAE	0.775	-7.0
1	0	1	0	1	1	1	1	0xAF	0.784	-6.9
1	0	1	1	0	0	0	0	0xB0	0.793	-6.8
1	0	1	1	0	0	0	1	0xB1	0.802	-6.7
1	0	1	1	0	0	1	0	0xB2	0.811	-6.6
1	0	1	1	0	0	1	1	0xB3	0.821	-6.5
1	0	1	1	0	1	0	0	0xB4	0.830	-6.4
1	0	1	1	0	1	0	1	0xB5	0.840	-6.3
1	0	1	1	0	1	1	0	0xB6	0.849	-6.2
1	0	1	1	0	1	1	1	0xB7	0.859	-6.1
1	0	1	1	1	0	0	0	0xB8	0.869	-6.0
1	0	1	1	1	0	0	1	0xB9	0.879	-5.9
1	0	1	1	1	0	1	0	0xBA	0.889	-5.8
1	0	1	1	1	0	1	1	0xBB	0.900	-5.7
1	0	1	1	1	1	0	0	0xBC	0.910	-5.6
1	0	1	1	1	1	0	1	0xBD	0.921	-5.5
1	0	1	1	1	1	1	0	0xBE	0.931	-5.4
1	0	1	1	1	1	1	1	0xBF	0.942	-5.3

RGR Settings [0xC0 to 0xFF]

Read @ 0x74 Write @ 0x34 ***Receive path gain settings greater than 0xC3 are permitted; however, large signals may cause overload.***

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
1	1	0	0	0	0	0	0	0xC0	0.953	-5.2
1	1	0	0	0	0	0	1	0xC1	0.964	-5.1
1	1	0	0	0	0	1	0	0xC2	0.975	-5.0
1	1	0	0	0	0	1	1	0xC3	0.987	-4.9
1	1	0	0	0	1	0	0	0xC4	0.998	-4.8
1	1	0	0	0	1	0	1	0xC5	1.010	-4.7
1	1	0	0	0	1	1	0	0xC6	1.021	-4.6
1	1	0	0	0	1	1	1	0xC7	1.033	-4.5
1	1	0	0	1	0	0	0	0xC8	1.045	-4.4
1	1	0	0	1	0	0	1	0xC9	1.057	-4.3
1	1	0	0	1	0	1	0	0xCA	1.069	-4.2
1	1	0	0	1	0	1	1	0xCB	1.082	-4.1
1	1	0	0	1	1	0	0	0xCC	1.094	-4.0
1	1	0	0	1	1	0	1	0xCD	1.107	-3.9
1	1	0	0	1	1	1	0	0xCE	1.120	-3.8
1	1	0	0	1	1	1	1	0xCF	1.133	-3.7
1	1	0	1	0	0	0	0	0xD0	1.146	-3.6
1	1	0	1	0	0	0	1	0xD1	1.159	-3.5
1	1	0	1	0	0	1	0	0xD2	1.173	-3.4
1	1	0	1	0	0	1	1	0xD3	1.186	-3.3
1	1	0	1	0	1	0	0	0xD4	1.200	-3.2
1	1	0	1	0	1	0	1	0xD5	1.214	-3.1
1	1	0	1	0	1	1	0	0xD6	1.228	-3.0
1	1	0	1	0	1	1	1	0xD7	1.242	-2.9
1	1	0	1	1	0	0	0	0xD8	1.256	-2.8
1	1	0	1	1	0	0	1	0xD9	1.271	-2.7
1	1	0	1	1	0	1	0	0xDA	1.286	-2.6
1	1	0	1	1	0	1	1	0xDB	1.301	-2.5
1	1	0	1	1	1	0	0	0xDC	1.316	-2.4
1	1	0	1	1	1	0	1	0xDD	1.331	-2.3
1	1	0	1	1	1	1	0	0xDE	1.346	-2.2
1	1	0	1	1	1	1	1	0xDF	1.362	-2.1
1	1	1	0	0	0	0	0	0xE0	1.378	-2.0
1	1	1	0	0	0	0	1	0xE1	1.394	-1.9
1	1	1	0	0	0	1	0	0xE2	1.410	-1.8
1	1	1	0	0	0	1	1	0xE3	1.426	-1.7
1	1	1	0	0	1	0	0	0xE4	1.443	-1.6
1	1	1	0	0	1	0	1	0xE5	1.459	-1.5
1	1	1	0	0	1	1	0	0xE6	1.476	-1.4
1	1	1	0	0	1	1	1	0xE7	1.493	-1.3
1	1	1	0	1	0	0	0	0xE8	1.510	-1.2
1	1	1	0	1	0	0	1	0xE9	1.528	-1.1
1	1	1	0	1	0	1	0	0xEA	1.546	-1.0
1	1	1	0	1	0	1	1	0xEB	1.564	-0.9
1	1	1	0	1	1	0	0	0xEC	1.582	-0.8
1	1	1	0	1	1	0	1	0xED	1.600	-0.7
1	1	1	0	1	1	1	0	0xEE	1.619	-0.6
1	1	1	0	1	1	1	1	0xEF	1.637	-0.5
1	1	1	1	0	0	0	0	0xF0	1.656	-0.4
1	1	1	1	0	0	0	1	0xF1	1.675	-0.3
1	1	1	1	0	0	1	0	0xF2	1.695	-0.2
1	1	1	1	0	0	1	1	0xF3	1.714	-0.1
1	1	1	1	0	1	0	0	0xF4	1.734	0.0
1	1	1	1	0	1	0	1	0xF5	1.754	+0.1
1	1	1	1	0	1	1	0	0xF6	1.775	+0.2
1	1	1	1	0	1	1	1	0xF7	1.795	+0.3
1	1	1	1	1	0	0	0	0xF8	1.816	+0.4
1	1	1	1	1	0	0	1	0xF9	1.837	+0.5
1	1	1	1	1	0	1	0	0xFA	1.858	+0.6
1	1	1	1	1	0	1	1	0xFB	1.880	+0.7
1	1	1	1	1	1	0	0	0xFC	1.902	+0.8
1	1	1	1	1	1	0	1	0xFD	1.924	+0.9
1	1	1	1	1	1	1	0	0xFE	1.946	+1.0
1	1	1	1	1	1	1	1	0xFF	1.968	+1.1

Transmit Gain Register

The transmit gain register allows the user to select the gain or loss between the analog interface port and the digital interface port.

Transmit gain can be programmed in 0.1 dB steps from –0.4 dB to +19.0 dB. This corresponds to a range of 0 dBm0 levels at the analog input between 0.811 Vrms and 0.087 Vrms driving into the 600-ohm termination impedance.

Telephony signals are usually referenced to a 0-dB TLP (transmission level point) level at the digital signal cross connect (DSX) interface. In this case, the digital port is considered the 0 dB TLP (0 dezi Bell level referenced to the zero transmission level point).

To set the transmit gain, determine the gain required of the module in order to achieve the desired TLP at the digital interface (usually 0 dBm or –2 dBm).

In order for the internal hybrid-balance circuitry to be effective, the portion of the module analog output to the analog input must be between –2.5 dB to –10.25 dB of the analog output. For instance, if the input signal is –6.0 dBm when the output signal produces 0 dBm, good hybrid balance can be achieved.

To convert the signal gain to the analog output voltage, use the following formula:

$$V = 0.7746 \text{ Vrms} * 10^{(Gx/20)}$$

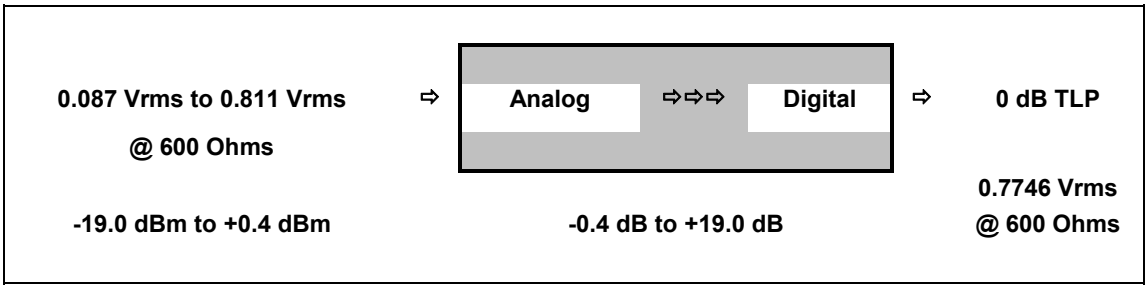
To convert the analog output voltage to the signal gain, use the following formula:

$$Gx = 20 * \log_{10} (V/0.7746 \text{ Vrms})$$

For example: The factory default setting for transmit gain is +6.0 dB. A signal with a level of –6.0 dBm presented at the analog input port produces an output of 0 dBm at the digital port.

When amplified by 19.0 dB, a 0.087 Vrms signal at analog input produces 0 dBm at digital port.

TRANSMIT PATH



TGR Settings [0x00 to 0x3F]

Read @ 0x75 Write @ 0x35

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
0	0	0	0	0	0	0	0	0x00		
0	0	0	0	0	0	0	1	0x01	0.087	+12.0
0	0	0	0	0	0	1	0	0x02	0.088	+11.9
0	0	0	0	0	0	1	1	0x03	0.089	+11.8
0	0	0	0	0	1	0	0	0x04	0.090	+11.7
0	0	0	0	0	1	0	1	0x05	0.091	+11.6
0	0	0	0	0	1	1	0	0x06	0.092	+11.5
0	0	0	0	0	1	1	1	0x07	0.093	+11.4
0	0	0	0	1	0	0	0	0x08	0.094	+11.3
0	0	0	0	1	0	0	1	0x09	0.095	+11.2
0	0	0	0	1	0	1	0	0x0A	0.096	+11.1
0	0	0	0	1	0	1	1	0x0B	0.098	+11.0
0	0	0	0	1	1	0	0	0x0C	0.099	+10.9
0	0	0	0	1	1	0	1	0x0D	0.100	+10.8
0	0	0	0	1	1	1	0	0x0E	0.101	+10.7
0	0	0	0	1	1	1	1	0x0F	0.102	+10.6
0	0	0	1	0	0	0	0	0x10	0.103	+10.5
0	0	0	1	0	0	0	1	0x11	0.104	+10.4
0	0	0	1	0	0	1	0	0x12	0.106	+10.3
0	0	0	1	0	0	1	1	0x13	0.107	+10.2
0	0	0	1	0	1	0	0	0x14	0.108	+10.1
0	0	0	1	0	1	0	1	0x15	0.109	+10.0
0	0	0	1	0	1	1	0	0x16	0.111	+9.9
0	0	0	1	0	1	1	1	0x17	0.112	+9.8
0	0	0	1	1	0	0	0	0x18	0.113	+9.7
0	0	0	1	1	0	0	1	0x19	0.115	+9.6
0	0	0	1	1	0	1	0	0x1A	0.116	+9.5
0	0	0	1	1	0	1	1	0x1B	0.117	+9.4
0	0	0	1	1	1	0	0	0x1C	0.119	+9.3
0	0	0	1	1	1	0	1	0x1D	0.120	+9.2
0	0	0	1	1	1	1	0	0x1E	0.121	+9.1
0	0	0	1	1	1	1	1	0x1F	0.123	+9.0
0	0	0	0	0	0	0	0	0x20	0.124	+8.9
0	0	0	0	0	0	0	1	0x21	0.126	+8.8
0	0	0	0	0	0	1	0	0x22	0.127	+8.7
0	0	0	0	0	0	1	1	0x23	0.129	+8.6
0	0	0	0	0	1	0	0	0x24	0.130	+8.5
0	0	0	0	0	1	0	1	0x25	0.132	+8.4
0	0	0	0	0	1	1	0	0x26	0.133	+8.3
0	0	0	0	0	1	1	1	0x27	0.135	+8.2
0	0	0	0	1	0	0	0	0x28	0.136	+8.1
0	0	0	0	1	0	0	1	0x29	0.138	+8.0
0	0	0	0	1	0	1	0	0x2A	0.139	+7.9
0	0	0	0	1	0	1	1	0x2B	0.141	+7.8
0	0	0	0	1	1	0	0	0x2C	0.143	+7.7
0	0	0	0	1	1	0	1	0x2D	0.144	+7.6
0	0	0	0	1	1	1	0	0x2E	0.146	+7.5
0	0	0	0	1	1	1	1	0x2F	0.148	+7.4
0	0	0	1	0	0	0	0	0x30	0.149	+7.3
0	0	0	1	0	0	0	1	0x31	0.151	+7.2
0	0	0	1	0	0	1	0	0x32	0.153	+7.1
0	0	0	1	0	0	1	1	0x33	0.155	+7.0
0	0	0	1	0	1	0	0	0x34	0.156	+6.9
0	0	0	1	0	1	0	1	0x35	0.158	+6.8
0	0	0	1	0	1	1	0	0x36	0.160	+6.7
0	0	0	1	0	1	1	1	0x37	0.162	+6.6
0	0	0	1	1	0	0	0	0x38	0.164	+6.5
0	0	0	1	1	0	0	1	0x39	0.166	+6.4
0	0	0	1	1	0	1	0	0x3A	0.168	+6.3
0	0	0	1	1	0	1	1	0x3B	0.169	+6.2
0	0	0	1	1	1	0	0	0x3C	0.171	+6.1
0	0	0	1	1	1	0	1	0x3D	0.173	+6.0
0	0	0	1	1	1	1	0	0x3E	0.175	+5.9
0	0	0	1	1	1	1	1	0x3F	0.177	+5.8

TGR Settings [0x40 to 0x7F]

Read @ 0x75 Write @ 0x35

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
0	0	1	0	0	0	0	0	0x40	0.180	+5.7
0	0	1	0	0	0	0	1	0x41	0.182	+5.6
0	0	1	0	0	0	1	0	0x42	0.184	+5.5
0	0	1	0	0	0	1	1	0x43	0.186	+5.4
0	0	1	0	0	1	0	0	0x44	0.188	+5.3
0	0	1	0	0	1	0	1	0x45	0.190	+5.2
0	0	1	0	0	1	1	0	0x46	0.192	+5.1
0	0	1	0	0	1	1	1	0x47	0.195	+5.0
0	0	1	0	1	0	0	0	0x48	0.197	+4.9
0	0	1	0	1	0	0	1	0x49	0.199	+4.8
0	0	1	0	1	0	1	0	0x4A	0.201	+4.7
0	0	1	0	1	0	1	1	0x4B	0.204	+4.6
0	0	1	0	1	1	0	0	0x4C	0.206	+4.5
0	0	1	0	1	1	0	1	0x4D	0.208	+4.4
0	0	1	0	1	1	1	0	0x4E	0.211	+4.3
0	0	1	0	1	1	1	1	0x4F	0.213	+4.2
0	0	1	1	0	0	0	0	0x50	0.216	+4.1
0	0	1	1	0	0	0	1	0x51	0.218	+4.0
0	0	1	1	0	0	1	0	0x52	0.221	+3.9
0	0	1	1	0	0	1	1	0x53	0.223	+3.8
0	0	1	1	0	1	0	0	0x54	0.226	+3.7
0	0	1	1	0	1	0	1	0x55	0.229	+3.6
0	0	1	1	0	1	1	0	0x56	0.231	+3.5
0	0	1	1	0	1	1	1	0x57	0.234	+3.4
0	0	1	1	1	0	0	0	0x58	0.237	+3.3
0	0	1	1	1	0	0	1	0x59	0.239	+3.2
0	0	1	1	1	0	1	0	0x5A	0.242	+3.1
0	0	1	1	1	0	1	1	0x5B	0.245	+3.0
0	0	1	1	1	1	0	0	0x5C	0.248	+2.9
0	0	1	1	1	1	0	1	0x5D	0.251	+2.8
0	0	1	1	1	1	1	0	0x5E	0.254	+2.7
0	0	1	1	1	1	1	1	0x5F	0.257	+2.6
0	0	1	0	0	0	0	0	0x60	0.259	+2.5
0	0	1	0	0	0	0	1	0x61	0.262	+2.4
0	0	1	0	0	0	1	0	0x62	0.266	+2.3
0	0	1	0	0	0	1	1	0x63	0.269	+2.2
0	0	1	0	0	1	0	0	0x64	0.272	+2.1
0	0	1	0	0	1	0	1	0x65	0.275	+2.0
0	0	1	0	0	1	1	0	0x66	0.278	+1.9
0	0	1	0	0	1	1	1	0x67	0.281	+1.8
0	0	1	0	1	0	0	0	0x68	0.285	+1.7
0	0	1	0	1	0	0	1	0x69	0.288	+1.6
0	0	1	0	1	0	1	0	0x6A	0.291	+1.5
0	0	1	0	1	0	1	1	0x6B	0.295	+1.4
0	0	1	0	1	1	0	0	0x6C	0.298	+1.3
0	0	1	0	1	1	0	1	0x6D	0.301	+1.2
0	0	1	0	1	1	1	0	0x6E	0.305	+1.1
0	0	1	0	1	1	1	1	0x6F	0.308	+1.0
0	0	1	1	0	0	0	0	0x70	0.312	+0.9
0	0	1	1	0	0	0	1	0x71	0.316	+0.8
0	0	1	1	0	0	1	0	0x72	0.319	+0.7
0	0	1	1	0	0	1	1	0x73	0.323	+0.6
0	0	1	1	0	1	0	0	0x74	0.327	+0.5
0	0	1	1	0	1	0	1	0x75	0.330	+0.4
0	0	1	1	0	1	1	0	0x76	0.334	+0.3
0	0	1	1	0	1	1	1	0x77	0.338	+0.2
0	0	1	1	1	0	0	0	0x78	0.342	+0.1
0	0	1	1	1	0	0	1	0x79	0.346	+0.0
0	0	1	1	1	0	1	0	0x7A	0.350	-0.1
0	0	1	1	1	0	1	1	0x7B	0.354	-0.2
0	0	1	1	1	1	0	0	0x7C	0.358	-0.3
0	0	1	1	1	1	0	1	0x7D	0.362	-0.4
0	0	1	1	1	1	1	0	0x7E	0.367	-0.5
0	0	1	1	1	1	1	1	0x7F	0.371	-0.6

TGR Settings [0x80 to 0xBF]

Read @ 0x75 Write @ 0x35 ***0 dB transmit path gain setting is 0xBF***

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
0	1	0	0	0	0	0	0	0x80	0.375	-0.7
0	1	0	0	0	0	0	1	0x81	0.379	-0.8
0	1	0	0	0	0	1	0	0x82	0.384	-0.9
0	1	0	0	0	0	1	1	0x83	0.388	-1.0
0	1	0	0	0	1	0	0	0x84	0.393	-1.1
0	1	0	0	0	1	0	1	0x85	0.397	-1.2
0	1	0	0	0	1	1	0	0x86	0.402	-1.3
0	1	0	0	0	1	1	1	0x87	0.407	-1.4
0	1	0	0	1	0	0	0	0x88	0.411	-1.5
0	1	0	0	1	0	0	1	0x89	0.416	-1.6
0	1	0	0	1	0	1	0	0x8A	0.421	-1.7
0	1	0	0	1	0	1	1	0x8B	0.426	-1.8
0	1	0	0	1	1	0	0	0x8C	0.431	-1.9
0	1	0	0	1	1	0	1	0x8D	0.436	-2.0
0	1	0	0	1	1	1	0	0x8E	0.441	-2.1
0	1	0	0	1	1	1	1	0x8F	0.446	-2.2
0	1	0	1	0	0	0	0	0x90	0.451	-2.3
0	1	0	1	0	0	0	1	0x91	0.456	-2.4
0	1	0	1	0	0	1	0	0x92	0.461	-2.5
0	1	0	1	0	0	1	1	0x93	0.467	-2.6
0	1	0	1	0	1	0	0	0x94	0.472	-2.7
0	1	0	1	0	1	0	1	0x95	0.478	-2.8
0	1	0	1	0	1	1	0	0x96	0.483	-2.9
0	1	0	1	0	1	1	1	0x97	0.489	-3.0
0	1	0	1	1	0	0	0	0x98	0.494	-3.1
0	1	0	1	1	0	0	1	0x99	0.500	-3.2
0	1	0	1	1	0	1	0	0x9A	0.506	-3.3
0	1	0	1	1	0	1	1	0x9B	0.512	-3.4
0	1	0	1	1	1	0	0	0x9C	0.518	-3.5
0	1	0	1	1	1	0	1	0x9D	0.524	-3.6
0	1	0	1	1	1	1	0	0x9E	0.530	-3.7
0	1	0	1	1	1	1	1	0x9F	0.536	-3.8
1	0	1	0	0	0	0	0	0xA0	0.542	-3.9
1	0	1	0	0	0	0	1	0xA1	0.548	-4.0
1	0	1	0	0	0	1	0	0xA2	0.555	-4.1
1	0	1	0	0	0	1	1	0xA3	0.561	-4.2
1	0	1	0	0	1	0	0	0xA4	0.568	-4.3
1	0	1	0	0	1	0	1	0xA5	0.574	-4.4
1	0	1	0	0	1	1	0	0xA6	0.581	-4.5
1	0	1	0	0	1	1	1	0xA7	0.588	-4.6
1	0	1	0	1	0	0	0	0xA8	0.594	-4.7
1	0	1	0	1	0	0	1	0xA9	0.601	-4.8
1	0	1	0	1	0	1	0	0xAA	0.608	-4.9
1	0	1	0	1	0	1	1	0xAB	0.615	-5.0
1	0	1	0	1	1	0	0	0xAC	0.622	-5.1
1	0	1	0	1	1	0	1	0xAD	0.630	-5.2
1	0	1	0	1	1	1	0	0xAE	0.637	-5.3
1	0	1	0	1	1	1	1	0xAF	0.644	-5.4
1	0	1	1	0	0	0	0	0xB0	0.652	-5.5
1	0	1	1	0	0	0	1	0xB1	0.659	-5.6
1	0	1	1	0	0	1	0	0xB2	0.667	-5.7
1	0	1	1	0	0	1	1	0xB3	0.675	-5.8
1	0	1	1	0	1	0	0	0xB4	0.682	-5.9
1	0	1	1	0	1	0	1	0xB5	0.690	-6.0
1	0	1	1	0	1	1	0	0xB6	0.698	-6.1
1	0	1	1	0	1	1	1	0xB7	0.706	-6.2
1	0	1	1	1	0	0	0	0xB8	0.715	-6.3
1	0	1	1	1	0	0	1	0xB9	0.723	-6.4
1	0	1	1	1	0	1	0	0xBA	0.731	-6.5
1	0	1	1	1	0	1	1	0xBB	0.740	-6.6
1	0	1	1	1	1	0	0	0xBC	0.748	-6.7
1	0	1	1	1	1	0	1	0xBD	0.757	-6.8
1	0	1	1	1	1	1	0	0xBE	0.766	-6.9
1	0	1	1	1	1	1	1	0xBF	0.775	-7.0

TGR Settings [0xC0 to 0xFF]

Read @ 0x75 Write @ 0x35 ***Transmit path gain settings greater than 0xC3 are permitted; however, large signals may cause overload.***

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Gain Vrms	Gain dB
1	1	0	0	0	0	0	0	0xC0	0766	-7.1
1	1	0	0	0	0	0	1	0xC1	0.793	-7.2
1	1	0	0	0	0	1	0	0xC2	0.802	-7.3
1	1	0	0	0	0	1	1	0xC3	0.811	-7.4
1	1	0	0	0	1	0	0	0xC4	0.821	-7.5
1	1	0	0	0	1	0	1	0xC5	0.830	-7.6
1	1	0	0	0	1	1	0	0xC6	0.840	-7.7
1	1	0	0	0	1	1	1	0xC7	0.849	-7.8
1	1	0	0	1	0	0	0	0xC8	0.859	-7.9
1	1	0	0	1	0	0	1	0xC9	0.869	-8.0
1	1	0	0	1	0	1	0	0xCA	0.879	-8.1
1	1	0	0	1	0	1	1	0xCB	0.889	-8.2
1	1	0	0	1	1	0	0	0xCC	0.900	-8.3
1	1	0	0	1	1	0	1	0xCD	0.910	-8.4
1	1	0	0	1	1	1	0	0xCE	0.921	-8.5
1	1	0	0	1	1	1	1	0xCF	0.931	-8.6
1	1	0	1	0	0	0	0	0xD0	0.942	-8.7
1	1	0	1	0	0	0	1	0xD1	0.953	-8.8
1	1	0	1	0	0	1	0	0xD2	0.964	-8.9
1	1	0	1	0	0	1	1	0xD3	0.975	-9.0
1	1	0	1	0	1	0	0	0xD4	0.986	-9.1
1	1	0	1	0	1	0	1	0xD5	0.998	-9.2
1	1	0	1	0	1	1	0	0xD6	1.009	-9.3
1	1	0	1	0	1	1	1	0xD7	1.021	-9.4
1	1	0	1	1	0	0	0	0xD8	1.033	-9.5
1	1	0	1	1	0	0	1	0xD9	1.045	-9.6
1	1	0	1	1	0	1	0	0xDA	1.057	-9.7
1	1	0	1	1	0	1	1	0xDB	1.069	-9.8
1	1	0	1	1	1	0	0	0xDC	1.082	-9.9
1	1	0	1	1	1	0	1	0xDD	1.094	-10.0
1	1	0	1	1	1	1	0	0xDE	1.107	-10.1
1	1	0	1	1	1	1	1	0xDF	1.120	-10.2
1	1	1	0	0	0	0	0	0xE0	1.133	-10.3
1	1	1	0	0	0	0	1	0xE1	1.146	-10.4
1	1	1	0	0	0	1	0	0xE2	1.159	-10.5
1	1	1	0	0	0	1	1	0xE3	1.172	-10.6
1	1	1	0	0	1	0	0	0xE4	1.186	-10.7
1	1	1	0	0	1	0	1	0xE5	1.200	-10.8
1	1	1	0	0	1	1	0	0xE6	1.214	-10.9
1	1	1	0	0	1	1	1	0xE7	1.228	-11.0
1	1	1	0	1	0	0	0	0xE8	1.242	-11.1
1	1	1	0	1	0	0	1	0xE9	1.256	-11.2
1	1	1	0	1	0	1	0	0xEA	1.271	-11.3
1	1	1	0	1	0	1	1	0xEB	1.286	-11.4
1	1	1	0	1	1	0	0	0xEC	1.300	-11.5
1	1	1	0	1	1	0	1	0xED	1.316	-11.6
1	1	1	0	1	1	1	0	0xEE	1.331	-11.7
1	1	1	0	1	1	1	1	0xEF	1.346	-11.8
1	1	1	1	0	0	0	0	0xF0	1.362	-11.9
1	1	1	1	0	0	0	1	0xF1	1.378	-12.0
1	1	1	1	0	0	1	0	0xF2	1.393	-12.1
1	1	1	1	0	0	1	1	0xF3	1.410	-12.2
1	1	1	1	0	1	0	0	0xF4	1.426	-12.3
1	1	1	1	0	1	0	1	0xF5	1.442	-12.4
1	1	1	1	0	1	1	0	0xF6	1.459	-12.5
1	1	1	1	0	1	1	1	0xF7	1.476	-12.6
1	1	1	1	1	0	0	0	0xF8	1.493	-12.7
1	1	1	1	1	0	0	1	0xF9	1.510	-12.8
1	1	1	1	1	0	1	0	0xFA	1.528	-12.9
1	1	1	1	1	0	1	1	0xFB	1.546	-13.0
1	1	1	1	1	1	0	0	0xFC	1.563	-13.1
1	1	1	1	1	1	0	1	0xFD	1.582	-13.2
1	1	1	1	1	1	1	0	0xFE	1.600	-13.3
1	1	1	1	1	1	1	1	0xFF	1.618	-13.4

Hybrid-Balance Registers

The Codec Hybrid-Balance Software Program from Lucent Technologies defines the correct settings for the Hybrid Balance Registers 1, 2, and 3. The settings are dependent on internal component parameters, external circuit parameters, and the termination impedance. Extensive knowledge of transmission theory and complex mathematics is required to set-up the transfer functions and run the program which computes the hybrid register settings.

The Hybrid-Balance filter is selected for two-wire interfaces. The Hybrid-Balance filter is deselected for four-wire interfaces.

HBR1 Settings

Read @ 0x76

Write @ 0x36

Function	Byte 2 of Register 1							
	7	6	5	4	3	2	1	0
	SEL	INV	SEL2	GAIN (ALL "0" = MAX)				
HYBAL Filter Deselected	0	-	-	-	-	-	-	-
HYBAL Filter Selected	1	-	-	-	-	-	-	-
Cancellation Signal Non-Inverted	-	0	-	-	-	-	-	-
Cancellation Signal Inverted	-	1	-	-	-	-	-	-
HYBAL2 Filter Deselected	-	-	0	-	-	-	-	-
HYBAL2 Filter Selected	-	-	1	-	-	-	-	-
Attenuator Values	-	-	-	X	X	X	X	X

HBR2 Settings

Read @ 0x77

Write @ 0x37

Function	Byte 2 of Register 2							
	7	6	5	4	3	2	1	0
	SEL1	SET	ZERO			POLE		
HYBAL1 Filter Deselected	0	-	-	-	-	-	-	-
HYBAL1 Filter Selected	1	-	-	-	-	-	-	-
HYBAL1 Filter First Order Selected	-	0	-	-	-	-	-	-
HYBAL1 Filter Bi-quad Selected	-	1	-	-	-	-	-	-
HYBAL1 Filter Zero Frequencies	-	-	X	X	X	-	-	-
HYBAL1 Filter Pole Frequencies	-	-	-	-	-	X	X	X

HBR3 Settings

Read @ 0x78

Write @ 0x38

Function	Byte 2 of Register 3							
	7	6	5	4	3	2	1	0
	ZERO				POLE			
HYBAL2 Filter Zero Frequencies	X	X	X	X	-	-	-	-
HYBAL2 Filter Pole Frequencies	-	-	-	-	X	X	X	X

Receive Time-Slot Register

The Receive Time-slot Register byte 2 functions are identical to the Receive Time-slot Register byte 2 functions.
The new time-slot assignment becomes active on the second frame following end of the CS for the second control byte.

RTR Settings

Read @ 0x79

Write @ 0x39

T5 is the MSB of the time-slot assignment.

Function	Bit Number and Name							
	7	6	5	4	3	2	1	0
	EN	PS	T5	T4	T3	T2	T1	T0
DR TDM Input Disabled	0	0	X	X	X	X	X	X
DR TDM Input Enabled	1	0	Assign One Binary Coded Time-slot from 0 - 63					

Note: T5 is the MSB of the time-slot assignment.

Transmit Time-Slot Register

The Transmit Time-slot Register byte 2 functions are identical to the Receive Time-slot Register byte 2 functions.
The new time-slot assignment becomes active on the second frame following end of the CS for the second control byte.

TTR Settings

Read @ 0x7A

Write @ 0x3A ***Note: T5 is the MSB of the time-slot assignment.***

Function	Bit Number and Name							
	7	6	5	4	3	2	1	0
	EN	PS	T5	T4	T3	T2	T1	T0
DX TDM Output Disabled	0	0	X	X	X	X	X	X
DX TDM Output Enabled	1	0	Assign One Binary Coded Time-slot from 0 - 63					

Note: T5 is the MSB of the time-slot assignment.

Delay Dial Register

The Delay Dial Register (**DDR**) allows the user to select the duration of the wink signal when the FXS port is set-up for AutoWINK operation. The delay between the start of the wink signal and the end of the wink signal can be set in 10ms increments. The answer delay timing range is adjustable from 10ms to 2.54s.

DDR Settings

Read @ 0x7B

Write @ 0x3B

Function	Bit Number								
	7	6	5	4	3	2	1	0	Hex
INVALID	0	0	0	0	0	0	0	0	0x00
10ms	0	0	0	0	0	0	0	1	0x01
20ms	0	0	0	0	0	0	1	0	0x02
30ms	0	0	0	0	0	0	1	1	0x03
40ms	0	0	0	0	0	1	0	0	0x04
50ms	0	0	0	0	0	1	0	1	0x05
60ms	0	0	0	0	0	1	1	0	0x06
70ms	0	0	0	0	0	1	1	1	0x07
80ms	0	0	0	0	1	0	0	0	0x08
90ms	0	0	0	0	1	0	0	1	0x09
100ms	0	0	0	0	1	0	1	0	0x0A
110ms	0	0	0	0	1	0	1	1	0x0B
120ms	0	0	0	0	1	1	0	0	0x0C
130ms	0	0	0	0	1	1	0	1	0x0D
140ms	0	0	0	0	1	1	1	0	0x0E
150ms	0	0	0	0	1	1	1	1	0x0F
160ms	0	0	0	1	0	0	0	0	0x10
170ms	0	0	0	1	0	0	0	1	0x11
180ms	0	0	0	1	0	0	1	0	0x12
190ms	0	0	0	1	0	0	1	1	0x13
200ms	0	0	0	1	0	1	0	0	0x14
210ms	0	0	0	1	0	1	0	1	0x15
220ms	0	0	0	1	0	1	1	0	0x16
230ms	0	0	0	1	0	1	1	1	0x17
240ms	0	0	0	1	1	0	0	0	0x18
250ms	0	0	0	1	1	0	0	1	0x19
260ms	0	0	0	1	1	0	1	0	0x1A
270ms	0	0	0	1	1	0	1	1	0x1B
280ms	0	0	0	1	1	1	0	0	0x1C
290ms	0	0	0	1	1	1	0	1	0x1D
300ms	0	0	0	1	1	1	1	0	0x1E
310ms	0	0	0	1	1	1	1	1	0x1F
320ms	0	0	1	0	0	0	0	0	0x20
330ms	0	0	1	0	0	0	0	1	0x21
340ms	0	0	1	0	0	0	1	0	0x22
350ms	0	0	1	0	0	0	1	1	0x23
360ms	0	0	1	0	0	1	0	0	0x24
370ms	0	0	1	0	0	1	0	1	0x25
380ms	0	0	1	0	0	1	1	0	0x26
390ms	0	0	1	0	0	1	1	1	0x27
400ms	0	0	1	0	1	0	0	0	0x28
410ms	0	0	1	0	1	0	0	1	0x29
420ms	0	0	1	0	1	0	1	0	0x2A
430ms	0	0	1	0	1	0	1	1	0x2B
440ms	0	0	1	0	1	1	0	0	0x2C
450ms	0	0	1	0	1	1	0	1	0x2D
460ms	0	0	1	0	1	1	1	0	0x2E
470ms	0	0	1	1	1	1	1	1	0x2F
480ms	0	0	1	1	0	0	0	0	0x30
490ms	0	0	1	1	0	0	0	1	0x31
500ms	0	0	1	1	0	0	1	0	0x32
510ms	0	0	1	1	0	0	1	1	0x33
520ms	0	0	1	1	0	1	0	0	0x34
530ms	0	0	1	1	0	1	0	1	0x35
540ms	0	0	1	1	0	1	1	0	0x36
550ms	0	0	1	1	0	1	1	1	0x37

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Function	Bit Number								
	7	6	5	4	3	2	1	0	Hex
560ms	0	0	1	1	1	0	0	0	0x38
570ms	0	0	1	1	1	0	0	1	0x39
580ms	0	0	1	1	1	0	1	0	0x3A
590ms	0	0	1	1	1	0	1	1	0x3B
600ms	0	0	1	1	1	1	0	0	0x3C
610ms	0	0	1	1	1	1	0	1	0x3D
	\	\	\	\	\	\	\	\	To
2.54s	1	1	1	1	1	1	1	0	0xFE
DISABLED	1	1	1	1	1	1	1	1	0xFF

SPI Control Register

The SPI control register allows the user to set specific SPI modes.

- **Writing to bit 2 selects the SPI Clock Phase**
- **Writing to bit 3 selects the SPI Clock Polarity**
- **Writing to bit 5 selects the SPI Data Order**

SPCR Settings

Read @ 0x7C

Write @ 0x3C

Function	Bit Number							
	7	6	5	4	3	2	1	0
Reserved	1	-	-	-	-	-	-	-
Reserved	-	1	-	-	-	-	-	-
SPI Data Order MSB First (default)	-	-	0	-	-	-	-	-
SPI Data Order LSB First	-	-	1	-	-	-	-	-
Reserved	-	-	-	0	-	-	-	-
SPI Clock Polarity Low When Idle (default)	-	-	-	-	0	-	-	-
SPI Clock Polarity High When Idle	-	-	-	-	1	-	-	-
Reserved	-	-	-	-	X	-	-	-
SPI Clock Phase Trailing Edge	-	-	-	-	-	0	-	-
SPI Clock Phase Leading Edge (default)	-	-	-	-	-	1	-	-
Reserved	-	-	-	-	-	-	1	-
Reserved	-	-	-	-	-	-	-	1

Wink Delay Register

The wink delay register allows the user to select the wink timing delay when the FXS port is set-up for AutoWink operation. When the ringing FXS analog port is answered then an automatic wink signal of 200ms duration is being issued on the digital CAS bit side. The timing delay between the analog off-hook and digital wink signal can be set in 100ms increments. The wink-delay timing range is adjustable from 100ms to 25.4 seconds.

WDR Settings

Read @ 0x7D

Write @ 0x3D

Function	Bit Number								
	7	6	5	4	3	2	1	0	Hex
INVALID	0	0	0	0	0	0	0	0	0x00
100ms	0	0	0	0	0	0	0	1	0x01
200ms	0	0	0	0	0	0	1	0	0x02
300ms	0	0	0	0	0	0	1	1	0x03
400ms	0	0	0	0	0	1	0	0	0x04
500ms	0	0	0	0	0	1	0	1	0x05
600ms	0	0	0	0	0	1	1	0	0x06
700ms	0	0	0	0	0	1	1	1	0x07
800ms	0	0	0	0	1	0	0	0	0x08
900ms	0	0	0	0	1	0	0	1	0x09
1s	0	0	0	0	1	0	1	0	0x0A
1.1s	0	0	0	0	1	0	1	1	0x0B
1.2s	0	0	0	0	1	1	0	0	0x0C
1.3s	0	0	0	0	1	1	0	1	0x0D
1.4s	0	0	0	0	1	1	1	0	0x0E
1.5s	0	0	0	0	1	1	1	1	0x0F
1.6s	0	0	0	1	0	0	0	0	0x10
1.7s	0	0	0	1	0	0	0	1	0x11
1.8s	0	0	0	1	0	0	1	0	0x12
1.9s	0	0	0	1	0	0	1	1	0x13
2.0s	0	0	0	1	0	1	0	0	0x14
2.1s	0	0	0	1	0	1	0	1	0x15
2.2s	0	0	0	1	0	1	1	0	0x16
2.3s	0	0	0	1	0	1	1	1	0x17
2.4s	0	0	0	1	1	0	0	0	0x18
2.5s	0	0	0	1	1	0	0	1	0x19
2.6s	0	0	0	1	1	0	1	0	0x1A
2.7s	0	0	0	1	1	0	1	1	0x1B
2.8s	0	0	0	1	1	1	0	0	0x1C
2.9s	0	0	0	1	1	1	0	1	0x1D
3.0s	0	0	0	1	1	1	1	0	0x1E
3.1s	0	0	0	1	1	1	1	1	0x1F
3.2s	0	0	1	0	0	0	0	0	0x20
3.3s	0	0	1	0	0	0	0	1	0x21
3.4s	0	0	1	0	0	0	1	0	0x22
3.5s	0	0	1	0	0	0	1	1	0x23
3.6s	0	0	1	0	0	1	0	0	0x24
3.7s	0	0	1	0	0	1	0	1	0x25
3.8s	0	0	1	0	0	1	1	0	0x26
3.9s	0	0	1	0	0	1	1	1	0x27
4.0s	0	0	1	0	1	0	0	0	0x28
4.1s	0	0	1	0	1	0	0	1	0x29
4.2s	0	0	1	0	1	0	1	0	0x2A
4.3s	0	0	1	0	1	0	1	1	0x2B
4.4s	0	0	1	0	1	1	0	0	0x2C
4.5s	0	0	1	0	1	1	0	1	0x2D
4.6s	0	0	1	0	1	1	1	0	0x2E
4.7s	0	0	1	1	1	1	1	1	0x2F
4.8s	0	0	1	1	0	0	0	0	0x30
4.9s	0	0	1	1	0	0	0	1	0x31
5.0s	0	0	1	1	0	0	1	0	0x32
5.1s	0	0	1	1	0	0	1	1	0x33
5.2s	0	0	1	1	0	1	0	0	0x34

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Function	Bit Number								
	7	6	5	4	3	2	1	0	Hex
5.3s	0	0	1	1	0	1	0	1	0x35
5.4s	0	0	1	1	0	1	1	0	0x36
5.5s	0	0	1	1	0	1	1	1	0x37
5.6s	0	0	1	1	1	0	0	0	0x38
5.7s	0	0	1	1	1	0	0	1	0x39
5.8s	0	0	1	1	1	0	1	0	0x3A
5.9s	0	0	1	1	1	0	1	1	0x3B
6.0s	0	0	1	1	1	1	0	0	0x3C
6.1s	0	0	1	1	1	1	0	1	0x3D
6.2s	0	0	1	1	1	1	1	0	0x3E
	\	\	\	\	\	\	\	\	To
25.4	1	1	1	1	1	1	1	0	0xFE
DISABLED	1	1	1	1	1	1	1	1	0xFF

Answer Delay Register

The answer delay register allows the user to select the answer timing delay when the FXS port is set-up for AutoFlash operation. When the ringing FXS analog port is answered then an answer signal is being issued on the digital CAS bit side either through hook-flash control or through the answer delay time-out. The timing delay between the analog off-hook and digital answer signal can be set in 100ms increments. The answer delay timing range is adjustable from 100ms to 25.4 seconds.

ADR Settings

Read @ 0x7E

Write @ 0x3E

Function	Bit Number								
	7	6	5	4	3	2	1	0	Hex
INVALID	0	0	0	0	0	0	0	0	0x00
100ms	0	0	0	0	0	0	0	1	0x01
200ms	0	0	0	0	0	0	1	0	0x02
300ms	0	0	0	0	0	0	1	1	0x03
400ms	0	0	0	0	0	1	0	0	0x04
500ms	0	0	0	0	0	1	0	1	0x05
600ms	0	0	0	0	0	1	1	0	0x06
700ms	0	0	0	0	0	1	1	1	0x07
800ms	0	0	0	0	1	0	0	0	0x08
900ms	0	0	0	0	1	0	0	1	0x09
1s	0	0	0	0	1	0	1	0	0x0A
1.1s	0	0	0	0	1	0	1	1	0x0B
1.2s	0	0	0	0	1	1	0	0	0x0C
1.3s	0	0	0	0	1	1	0	1	0x0D
1.4s	0	0	0	0	1	1	1	0	0x0E
1.5s	0	0	0	0	1	1	1	1	0x0F
1.6s	0	0	0	1	0	0	0	0	0x10
1.7s	0	0	0	1	0	0	0	1	0x11
1.8s	0	0	0	1	0	0	1	0	0x12
1.9s	0	0	0	1	0	0	1	1	0x13
2.0s	0	0	0	1	0	1	0	0	0x14
2.1s	0	0	0	1	0	1	0	1	0x15
2.2s	0	0	0	1	0	1	1	0	0x16
2.3s	0	0	0	1	0	1	1	1	0x17
2.4s	0	0	0	1	1	0	0	0	0x18
2.5s	0	0	0	1	1	0	0	1	0x19
2.6s	0	0	0	1	1	0	1	0	0x1A
2.7s	0	0	0	1	1	0	1	1	0x1B
2.8s	0	0	0	1	1	1	0	0	0x1C
2.9s	0	0	0	1	1	1	0	1	0x1D
3.0s	0	0	0	1	1	1	1	0	0x1E
3.1s	0	0	0	1	1	1	1	1	0x1F
3.2s	0	0	1	0	0	0	0	0	0x20
3.3s	0	0	1	0	0	0	0	1	0x21
3.4s	0	0	1	0	0	0	1	0	0x22
3.5s	0	0	1	0	0	0	1	1	0x23
3.6s	0	0	1	0	0	1	0	0	0x24
3.7s	0	0	1	0	0	1	0	1	0x25
3.8s	0	0	1	0	0	1	1	0	0x26
3.9s	0	0	1	0	0	1	1	1	0x27
4.0s	0	0	1	0	1	0	0	0	0x28
4.1s	0	0	1	0	1	0	0	1	0x29
4.2s	0	0	1	0	1	0	1	0	0x2A
4.3s	0	0	1	0	1	0	1	1	0x2B
4.4s	0	0	1	0	1	1	0	0	0x2C
4.5s	0	0	1	0	1	1	0	1	0x2D
4.6s	0	0	1	0	1	1	1	0	0x2E
4.7s	0	0	1	1	1	1	1	1	0x2F
4.8s	0	0	1	1	0	0	0	0	0x30
4.9s	0	0	1	1	0	0	0	1	0x31
5.0s	0	0	1	1	0	0	1	0	0x32
5.1s	0	0	1	1	0	0	1	1	0x33
5.2s	0	0	1	1	0	1	0	0	0x34

Continued from previous page:

Function	Bit Number								
	7	6	5	4	3	2	1	0	Hex
5.3s	0	0	1	1	0	1	0	1	0x35
5.4s	0	0	1	1	0	1	1	0	0x36
5.5s	0	0	1	1	0	1	1	1	0x37
5.6s	0	0	1	1	1	0	0	0	0x38
5.7s	0	0	1	1	1	0	0	1	0x39
5.8s	0	0	1	1	1	0	1	0	0x3A
5.9s	0	0	1	1	1	0	1	1	0x3B
6.0s	0	0	1	1	1	1	0	0	0x3C
6.1s	0	0	1	1	1	1	0	1	0x3D
	\	\	\	\	\	\	\	\	To
25.4	1	1	1	1	1	1	1	0	0xFE
DISABLED	1	1	1	1	1	1	1	1	0xFF

Reset Count Register

The RCR keeps track of how often the module has been reset since start of operation. The RCR can be "reset" by writing zeros into it. A module reset can occur due to the following events:

- Regular Power-Up Operation
- Module Reset Pin Asserted
- Internal Watchdog Timer Triggered

RCR Settings

Read @ 0x7F

Write @ 0x3F

Function	Bit Number and Name							
	7	6	5	4	3	2	1	0
Current Reset Count Value	X	X	X	X	X	X	X	X

Chapter 5 – System Design Considerations

System Design Considerations:
- Power
- Grounding
- Safety
- Telecom
- Emissions

To Protect the Product Against Outside World Threats:
- Power Line Crossings
- Transient Voltage Surges
- Electrostatic Discharges

To Prevent System Noise from Reaching the Outside World:
- Conducted Emissions
- Radiated Emissions

To Stabilize the Module's +5Vdc Power Source:
- Power Entry Filtering
- Current Spike Smoothing
- Temporary Energy Storage

To Meet Telecom and Safety Requirements:
- Domestically
- Globally

Electromagnetic Interference (EMI) Considerations

The following guidelines are offered specifically to help minimize EMI generation. Some of these guidelines are the same as, or similar to, the general guidelines but are mentioned again to reinforce their importance. In order to minimize the contribution of the SocketModem-based design to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

1. Keep traces carrying high frequency signals as short as possible.
2. Provide a good ground plane or grid. In some cases, a multilayer board may be required with full layers for ground and power distribution.
3. Decouple power from ground with decoupling capacitors as close to the SocketModem power pins as possible.
4. Eliminate ground loops, which are unexpected current return paths to the power source and ground.
5. Decouple the telephone line cables at the telephone line jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines; however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
6. Decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.
7. Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
8. Locate cables and connectors so as to avoid coupling from high frequency circuits.
9. Lay out the highest frequency signal traces next to the ground grid.
10. If a multilayer board design is used, make no cuts in the ground or power planes and be sure the ground plane covers all traces.
11. Minimize the number of through-hole connections on traces carrying high frequency signals.
12. Avoid right angle turns on high frequency traces. Forty-five degree corners are good; however, radius turns are better.

13. On 2-layer boards with no ground grid, provide a shadow ground trace on the opposite side of the board to traces carrying high frequency signals. This will be effective as a high frequency ground return if it is three times the width of the signal traces.
14. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.

Electrostatic Discharge Control

- All electronic devices should be handled with certain precautions to avoid damage due to the accumulation of static charge.
- See the ANSI/ESD Association Standard (ANSI/ESD S20.20-1999) – a document "for the Development of an Electrostatic Discharge Control for Protection of Electrical and Electronic Parts, Assemblies and Equipment." This document covers ESD Control Program Administrative Requirements, ESD Training, ESD Control Program Plan Technical Requirements (grounding/bonding systems, personnel grooming, protected areas, packaging, marking, equipment, and handling), and Sensitivity Testing.
- Multi-Tech Systems, Inc. strives to follow all of these recommendations. Input protection circuitry has been incorporated into the Multi-Tech devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling.
- Multi-Tech uses and recommends that others use anti-static boxes that create a faraday cage (packaging designed to exclude electromagnetic fields). Multi-Tech recommends that you use our packaging when returning a product and when you ship your products to your customers.

Phone Line Warning Statement for the Developer Board

Use extreme caution when the phone line is installed due to live energized components. In fact, do not touch any components on the board while the phone line is installed.

In addition, the phone line should be detached when making modifications to or servicing the developer board.

For other telephone warnings, refer to the Telecom Warnings listed earlier in this chapter.

Chapter 6 – Power Considerations

In order to achieve low power dissipation the following considerations should be followed:

- Power Supply
- Power Dissipation
- Power Management

Power Supply

It is recommended that the standard CMOS practice of applying ground to the device before any other connections are made should always be followed. The module by itself is not designed for hot-swap ability. A by-pass capacitor of 47 uF, 6.3Vdc, low ESR should be connected between the each modules power pins. The board power supply input should also be de-coupled with a low effective series resistance (ESR) capacitor of at least 10uF located at the printed circuit board power entry point. For electromagnetic compatibility (EMC) use of at least one set of power and ground planes within a multi-layer printed circuit board (PCB) is strongly recommended. A stable, low ESR and regulated power supply is required for optimum and trouble-free module operation.

Power Dissipation

The SocketSLIC power dissipation varies between different interface and mode settings. Refer to the table below for power budget requirements in multi-port system designs under the following conditions:

1. Interface is at idle condition "On-Hook" (no ringing, no AC or DC load)
2. Interface is at alerting condition "Ringing" (ringing into an AC load)
3. Interface is at seize condition "Off-Hook" (powering a DC load)

INTERFACE	Supply Current MA	Supply Current mA	Supply Current MA
	1. ON-HOOK No load	2. RINGING 2.2uF//3.9 kOhms	3. OFF-HOOK 100 Ohms
SHUT-DOWN	4	-	-
RESET	11	-	-
INACTIVE	22	-	-
FXS-LS	60	360	435
FXS-RB	60	360	430
FXS-GS	50	350	425
DPO	60	-	435
FXO-LS	40	-	-
FXO-RB	40	-	-
FXO-GS	40	-	-
DPT	40	-	-
TO/ETO	40	-	-
E&M, I	55	-	425
E&M, II	55	-	425
E&M, III	52	-	425
E&M, IV	48	-	425
E&M, V	52	-	420
PLR, I	52	-	420
PLR, II	52	-	420
PLR, III	52	-	420
PLR, IV	52	-	420
PLR, V	52	-	420

Power Management

Considering the management of the following registers reduces power consumption during operation:

- **Module Mode Register** (shut down the module when the port is not assigned)
- **Telecom Voltage Register** (reduce telecom voltage for short haul applications)
- **Ring Voltage Register** (reduce ringing voltage for short haul applications)
- **Ring Pattern Register** (see below)

When operating multiple modules on the same power supply consider managing the alerting pattern (ring cadence) via the CAS bits from the host controller. That way each module can be instructed to ring while the other modules are not ringing.

Power-Up

When power is first applied, the module should be held in the reset state. After the supply voltage and the externally applied logic levels have been stabilized the reset may be released. After reset has been released, the module reverts to the factory default settings.

Shut-Down

Writing 0x01 to the module mode register (MMR) instructs the module to shutdown and go to sleep. The power consumption is the lowest while in this state. The processor is shutdown thus reading and writing to and from the internal registers is not possible. A hard module reset is required to power-up the module from this state and start the initialization sequence.

Reset

Pulling the reset pin high causes the module to enter its reset state. There is no limit on how long the reset state may remain active. The power consumption is reduced while in this state. All module functions are disabled. Pulling the reset pin low releases the module from the reset state and starts the initialization sequence. For normal operation the reset pin must be pulled low. It is recommended to use a reset generator integrated circuit (IC) to provide proper power-up reset control. The module has a user accessible reset count register that keeps track of how often the module reset has been released. This feature comes in handy to check how often the module-reset pin or power supply has been cycled. The reset counter can be preset or cleared as needed.

Inactive

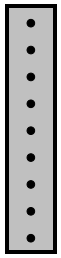
Writing 0x00 to the interface selection register (ISR) instructs the analog port to enter the inactive state. All analog interface operation stops, the Codec is shut down and the telecom power supply is shut-off. The power consumption in this state is about half of the interface idle state. The processor is still active and reading and writing through the control interface port is possible. A different interface selection is required to change this state. All registers are initialized.

Power-Off

We recommend that data not be written to the module before and during removal of power.

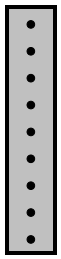
Chapter 7 – Port Hook-Ups

FXO, FXS, DPO AND DPT



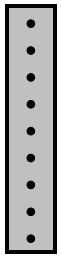
SB			(not used)
SG			(not used)
T			(not used)
E/TIP	↔	Tip Lead	(transmit/receive talk-path and signaling)
M/RING	↔	Ring Lead	(transmit/receive talk-path and signaling)
R			(not used)
TRC			(not used)
R1			(not used)
T1			(not used)

2-W, E&M I



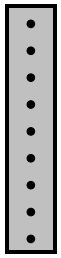
SB			(not used)
SG			(not used)
T	↔	T-Lead	(transmit/receive talk-path)
E	→	E-Lead	(transmit signaling)
M	←	M-Lead	(receive signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC	→←	Ground	(common ground)
R1			(not used)
T1			(not used)

2-W, E&M II



SB		SB-Lead	(receive signaling/battery)
SG		SG-Lead	(transmit signaling/looped)
T	↔	T-Lead	(transmit/receive talk-path)
E	→	E-Lead	(transmit signaling)
M	←	M-Lead	(receive signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC			(not used)
R1			(not used)
T1			(not used)

2-W, E&M III

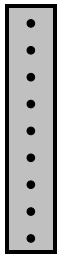


SB		SB-Lead	(receive signaling/battery)
SG		SG-Lead	(receive signaling/ground)
T	↔	T-Lead	(transmit/receive talk-path)
E	→	E-Lead	(transmit signaling)
M	←	M-Lead	(receive signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC	→←	Ground	(common ground)
R1			(not used)
T1			(not used)

2-W, E&M IV

Notes: The following module pins must be re-labeled for E&M type IV interface operation:

The E-lead pin becomes the M-lead.
The M-lead pin becomes the E-lead.
The SG-lead pin becomes the SB-lead.
The SB-lead pin becomes the SG-lead.



SB		SG-Lead	(receive signaling/ground)
SG		SB-Lead	(transmit signaling/looped)
T	↔	T-Lead	(transmit/receive talk-path)
E	→	M-Lead	(transmit signaling)
M	←	E-Lead	(receive signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC			(not used)
R1			(not used)
T1			(not used)

2-W, E&M V

SB			(not used)
SG			(not used)
T	↔	T-Lead	(transmit/receive talk-path)
E	→	E-Lead	(transmit signaling)
M	←	M-Lead	(receive signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC	→←	Ground	(common ground)
R1			(not used)
T1			(not used)

2-W, TO

SB			(not used)
SG			(not used)
T	↔	T-Lead	(transmit/receive talk-path)
E			(not used)
M			(not used)
R	↔	R-Lead	(transmit/receive talk-path)
TRC			(not used)
R1			(not used)
T1			(not used)

2-W, PLR I

SB			(not used)
SG			(not used)
T	↔	T-Lead	(transmit/receive talk-path)
E	←	E-Lead	(receive signaling)
M	→	M-Lead	(transmit signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC	→←	Ground	(common ground)
R1			(not used)
T1			(not used)

2-W, PLR II

SB		SB-Lead	(transmit signaling/looped)
SG		SG-Lead	(receive signaling/ground)
T	↔	T-Lead	(transmit/receive talk-path)
E	←	E-Lead	(receive signaling)
M	→	M-Lead	(transmit signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC			(not used)
R1			(not used)
T1			(not used)

2-W, PLR III

SB		SB-Lead	(transmit signaling/looped/active)
SG		SG-Lead	(transmit signaling/looped/idle)
T	↔	T-Lead	(transmit/receive talk-path)
E	←	E-Lead	(receive signaling)
M	→	M-Lead	(transmit signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC	→←	Ground	(common ground)
R1			(not used)
T1			(not used)

2-W, PLR IV

SB	→	SB-Lead	(transmit signaling/looped)
SG	→	SG-Lead	(receive signaling/ground)
T	↔	T-Lead	(transmit/receive talk-path)
E	←	E-Lead	(receive signaling)
M	→	M-Lead	(transmit signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC			(not used)
R1			(not used)
T1			(not used)

2-W, PLR V

SB			(not used)
SG			(not used)
T	↔	T-Lead	(transmit/receive talk-path)
E	←	E-Lead	(receive signaling)
M	→	M-Lead	(transmit signaling)
R	↔	R-Lead	(transmit/receive talk-path)
TRC	→←	Ground	(common ground)
R1			(not used)
T1			(not used)

4-W, ETO

SB			(not used)
SG			(not used)
T	←	T-Lead	(receive talk-path)
E			(not used)
M			(not used)
R	←	R-Lead	(receive talk-path)
TRC			(not used)
R1	→	R1-Lead	(transmit talk-path)
T1	→	T1-Lead	(transmit talk-path)

4-W, E&M I

SB			(not used)
SG			(not used)
T	←	T-Lead	(receive talk-path)
E	→	E-Lead	(transmit signaling)
M	←	M-Lead	(receive signaling)
R	←	R-Lead	(receive talk-path)
TRC	→←	Ground	(common ground)
R1	→	R1-Lead	(transmit talk-path)
T1	→	T1-Lead	(transmit talk-path)

4-W, E&M II

SB		SB-Lead	(receive signaling/battery)
SG		SG-Lead	(transmit signaling/looped)
T	←	T-Lead	(receive talk-path)
E	→	E-Lead	(transmit signaling)
M	←	M-Lead	(receive signaling)
R	←	R-Lead	(receive talk-path)
TRC			(not used)
R1	→	R1-Lead	(transmit talk-path)
T1	→	T1-Lead	(transmit talk-path)

4-W, E&M III

SB		SB-Lead	(receive signaling/battery)
SG		SG-Lead	(receive signaling/ground)
T	←	T-Lead	(receive talk-path)
E	→	E-Lead	(transmit signaling)
M	←	M-Lead	(receive signaling)
R	←	R-Lead	(receive talk-path)
TRC	→←	Ground	(common ground)
R1	→	R1-Lead	(transmit talk-path)
T1	→	T1-Lead	(transmit talk-path)

4-W, E&M IV

Note: The following module pins must be re-labeled for E&M type IV interface operation:

The E-lead pin becomes the M-lead.

The M-lead pin becomes the E-lead.

The SG-lead pin becomes the SB-lead.

The SB-lead pin becomes the SG-lead.

SB	•		**SG-Lead**	**(receive signaling/ground)**
SG	•		**SB-Lead**	**(transmit signaling/looped)**
T	•	←	**T-Lead**	**(receive talk-path)**
E	•	→	**M-Lead**	**(transmit signaling)**
M	•	←	**E-Lead**	**(receive signaling)**
R	•	←	**R-Lead**	**(receive talk-path)**
TRC	•			**(not used)**
R1	•	→	**R1-Lead**	**(transmit talk-path)**
T1	•	→	**T1-Lead**	**(transmit talk-path)**

4-W, E&M V

SB	•			**(not used)**
SG	•			**(not used)**
T	•	←	**T-Lead**	**(receive talk-path)**
E	•	→	**E-Lead**	**(transmit signaling)**
M	•	←	**M-Lead**	**(receive signaling)**
R	•	←	**R-Lead**	**(receive talk-path)**
TRC	•	→←	**Ground**	**(common ground)**
R1	•	←	**R1-Lead**	**(transmit talk-path)**
T1	•	←	**T1-Lead**	**(transmit talk-path)**

4-W, PLR I

SB	•			**(not used)**
SG	•			**(not used)**
T	•	←	**T-Lead**	**(receive talk-path)**
E	•	←	**E-Lead**	**(receive signaling)**
M	•	→	**M-Lead**	**(transmit signaling)**
R	•	←	**R-Lead**	**(receive talk-path)**
TRC	•	→←	**Ground**	**(common ground)**
R1	•	→	**R1-Lead**	**(transmit talk-path)**
T1	•	→	**T1-Lead**	**(transmit talk-path)**

4-W, PLR II

SB	•		**SB-Lead**	**(transmit signaling/looped)**
SG	•		**SB-Lead**	**(receive signaling/ground)**
T	•	←	**T-Lead**	**(receive talk-path)**
E	•	←	**E-Lead**	**(receive signaling)**
M	•	→	**M-Lead**	**(transmit signaling)**
R	•	←	**R-Lead**	**(receive talk-path)**
TRC	•			**(not used)**
R1	•	→	**R1-Lead**	**(transmit talk-path)**
T1	•	→	**T1-Lead**	**(transmit talk-path)**

4-W, PLR III

SB	•		**SB-Lead**	**((transmit signaling/looped/active)**
SG	•		**SG-Lead**	**(transmit signaling/looped/idle)**
T	•	←	**T-Lead**	**(receive talk-path)**
E	•	←	**E-Lead**	**(receive signaling)**
M	•	→	**M-Lead**	**(transmit signaling)**
R1	•	←	**R-Lead**	**(receive talk-path)**
TRC	•	→←	**Ground**	**(common ground)**
R1	•	→	**R1-Lead**	**(transmit talk-path)**
T1	•	→	**T1-Lead**	**(transmit talk-path)**

4-W, PLR IV

SB	•		SB-Lead	(transmit signaling/looped)
SG	•		SG-Lead	(receive signaling/ground)
T	•	←	T-Lead	(receive talk-path)
E	•	←	E-Lead	(receive signaling)
M	•	→	M-Lead	(transmit signaling)
R	•	←	R-Lead	(receive talk-path)
TRC	•			(not used)
R1	•	→	R1-Lead	(transmit talk-path)
T1	•	→	T1-Lead	(transmit talk-path)

4-W, PLR V

SB	•			(not used)
SG	•			(not used)
T	•	←	T-Lead	(receive talk-path)
E	•	←	E-Lead	(receive signaling)
M	•	→	M-Lead	(transmit signaling)
R	•	←	R-Lead	(receive talk-path)
TRC	•	→←	Ground	(common ground)
R1	•	→	R1-Lead	(transmit talk-path)
T1	•	→	T1-Lead	(transmit talk-path)

Chapter 8 – Specifications

Ports Per Module		
Analog Port	1	
Digital Port	1	
Control Port	1	
Analog Interfaces		
Foreign Exchange Subscriber	**FXS**	(Loop-Start, Ground-Start or Reverse Battery)
Foreign Exchange Office	**FXO**	(Loop-Start, Ground-Start or Reverse Battery)
Dial Pulse Originating	**DPO**	(Loop-Reverse-Battery-Signaling, “DID”)
Dial Pulse Terminating	**DPT**	(Loop-Reverse-Battery-Signaling, “DOD”)
E&M Lead Signaling	**E&M**	(2-Wire or 4-Wire)
Pulse Link Repeater	**PLR**	(2-Wire or 4-Wire)
Equalized Transmission Only	**ETO**	(4-Wire)
Transmission Only	**TO**	(2-Wire)
Digital Interfaces		
AT&T	**CHI**	(Concentration Highway Interface)
Multi-Vendor Integration Protocol	**MVIP**	(sub-set)
Mitel	**ST-Bus**	(2.048 Mbps)
Command Interfaces		
SPI Interface	**Synchronous Serial**	
UART Interface	**Asynchronous Serial**	
Termination		
Analog Port	**9-Pin**	(Header with 2-mm pitch)
Digital Port	**9-Pin**	(Header with 2-mm pitch)
Command Port	**9-Pin**	(Header with 2-mm pitch)
Power Requirements		
Voltage	**+5 Vdc**	(Nominal)
Tolerance	**+/-5 %**	(Maximum)
Current	**0.425 A**	(Maximum)
Power	**2.1250 W**	(Maximum)
Dimensions		
Length	**3.750 “**	(9.525 cm)
Depth	**1.065 “**	(2.705 cm)
Height (seated)	**0.540 “**	(1.372 cm)
Environmental		
Operating Temperature	**+32 °F to +104 °F**	(0 °C to 40 °C)
Storage Temperature	**-40 °F to +185 °F**	(-40 °C to +85 °C)
Humidity	**5 % to 95 %**	(non-condensing)
Weight		
Net Weight	**1 oz**	(28 g)

Technical Data

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITION
AUDIO FREQUENCY RESPONSE	300.00		3,400.00	Hz	0.5 dB
AUDIO IMPEDANCE	576.50	600.00	623.50	Ohms	300 Hz-3000 Hz
TRANSMIT GAIN RANGE	-0.40		+19.00	dB	@600 Ohms
TRANSMIT GAIN STEP		0.10		dB	
RECEIVE GAIN RANGE	-17.30		+2.10	dB	@600 Ohms
RECEIVE GAIN STEP		0.10		dB	
RETURN LOSS	34.00			dB	300 Hz-3000 Hz
TRANS-HYBRID LOSS	24.00			dB	@600 Ohms
CROSS TALK	80.00			dB	@600 Ohms
LONGITUDINAL BALANCE	60.00			dB	200 Hz-1000 Hz
LONGITUDINAL BALANCE	40.00			dB	1000 Hz-4000 Hz
DISTORTION, SINGLE FREQUENCY		-46.00		dB	1004 Hz @ 0 dBm
DISTORTION, INTER MODULATION		-41.00		dB	@600 Ohms
IDLE CHANNEL NOISE			20.00	dBrNC0	@600 Ohms
BATTERY RESISTANCE	360.00	400.00	440.00	Ohms	
BATTERY VOLTAGE (typical)	-43.20	-48.00	-52.80	Vdc	
BATTERY CURRENT	16.00		50.00	mA	
LOOP RESISTANCE			2,400.00	Ohms	
LOOP VOLTAGE	3.20		52.80	Vdc	
LOOP CURRENT	16.00		40.00	mA	
OFF-HOOK RESISTANCE			200.00	Ohms	
OFF-HOOK VOLTAGE	3.20		45.00	Vdc	
OFF-HOOK CURRENT	16.00		40.00	mA	
ON-HOOK RESISTANCE	30,000.00			Ohms	
ON-HOOK VOLTAGE	43.50		52.80	Vdc	
ON-HOOK CURRENT	0.00		1.76	mA	
RING FREQUENCY	16.00	20.00	68.00	Hz	
RING LOAD	0.00		5.00	REN	
RING VOLTAGE	45.00		150.00	Vrms	
RING TRIP TIME	50.00		200.00	ms	@1,500 Ohms
LOOP DETECT CURRENT FOR Tip/E	16.00			mA	
LOOP DETECT CURRENT FOR Ring/M	3.00			mA	

Characteristics

ELECTRICAL

TDM	(as per Lucent Codec T7570)
SPI	(as per Atmel Microcontroller AT89S8252)
UART	(as per Atmel Microcontroller AT89S8252)

TRANSMISSION

TDM	(as per Lucent Codec T7570)
SPI	(as per Atmel Microcontroller AT89S8252)
UART	(as per Atmel Microcontroller AT89S8252)

TIMING

TDM	(as per Lucent Codec T7570)
SPI	(as per Atmel Microcontroller AT89S8252)
UART	(as per Atmel Microcontroller AT89S8252)

Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings can cause permanent damage to the module. These are absolute stress ratings only. Functional operation of the module is not implied at these or any other conditions in excess of those given in the technical data sections of this manual. Exposure to absolute maximum rating conditions for extended periods can affect the module reliability.

PARAMETERS	MIN	MAX	UNIT
Storage Temperature	-55.00	+150.00	C
Operating Temperature	0.00	+70.00	C
Logic Power Supply Voltage		+6.50	V
Logic Pins in Reference to Ground	-0.50	+5.50	V
Logic DC Output Current		15.0	mA

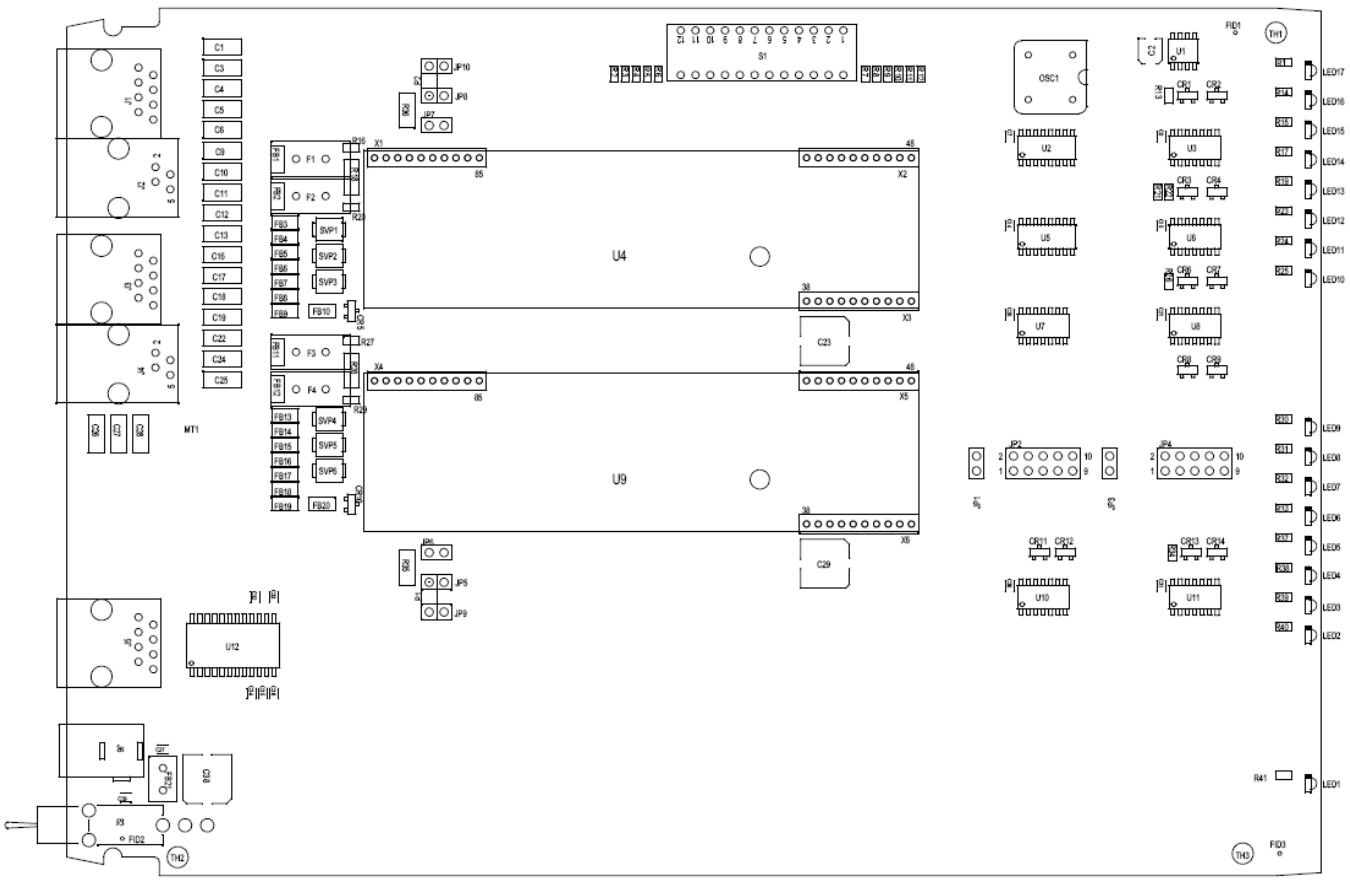
Facility Interface Codes

The Federal Communications Commission (FCC) has established different Facility Interface Codes (FIC) defining registered interfaces. Those codes are tariff references used by customers to order the type of service from the local servicing Phone Company. Please note that the FCC does not issue FIC codes for certain interfaces. Those interfaces are typically associated either with CO switches or PBX station interfaces.

FACILITY	INTERFACE	CODE
LOOP	FXS-LS	-
LOOP	FXS-RB	-
LOOP	FXS-GS	-
LOOP	DPO	02RV2-T
LOOP	FXO-LS	02LS2
LOOP	FXO-RB	-
LOOP	FXO-GS	02GS-2
LOOP	DPT	-
E&M	2-W, E&M, I	TL11-E
E&M	2-W, E&M, II	TL12-E
E&M	2-W, E&M, III	-
E&M	2-W, E&M, IV	-
E&M	2-W, E&M, V	-
E&M	2-W, PLR, I	TL11-M
E&M	2-W, PLR, II	TL12-M
E&M	2-W, PLR, III	-
E&M	2-W, PLR, IV	-
E&M	2-W, PLR, V	-
E&M	4-W, E&M, I	TL31-E
E&M	4-W, E&M, II	TL32-E
E&M	4-W, E&M, III	-
E&M	4-W, E&M, IV	-
E&M	4-W, E&M, V	-
E&M	4-W, PLR, I	TL31-M
E&M	4-W, PLR, II	TL32-M
E&M	4-W, PLR, III	-
E&M	4-W, PLR, IV	-
E&M	4-W, PLR, V	-

Appendix A – SocketSLIC Developer Board

Customers planning to use the SocketSLIC in an application of any significant complexity will need to conduct tests using it in a prototype of the system in which it will ultimately operate. Multi-Tech developed the IFM Developer's Board for this purpose. Customers who have identified their SocketSLIC application or are considering an application can use the Developer Board for evaluation and development.



SocketSLIC Developer Board

SocketSLIC Developer Kit Contents

The SocketSLIC Developer Kit contains the following:

- Two SocketSLIC units are included so that a full bi-directional coding/decoding path can be constructed.
- One Developer Test Card/Developer Board
- One Universal Power Supply
- One DB9 to RJ-45 cable
- One SocketSLIC CD

LED Descriptions

LEDs FOR CHANNELS 1 & 0	DESCRIPTION
RSG	**RECEIVE SIGNALING –** This active high output indicates the outgoing analog signaling state.
XSG	**TRANMIT SIGNALING –** This active high output indicates the incoming analog signaling state.
ARCV	**RECEIVE A CAS BIT –** This input receives the ***A*** signaling bit that controls the outgoing analog signaling state.
BRCV	**RECEIVE B CAS BIT –** This input receives the ***B*** signaling bit that controls the outgoing analog signaling state.
AXMT	**TRANSMIT A CAS BIT –** This output transmits the ***A*** signaling bit that indicates the incoming analog signaling state.
BXMT	**TRANSMIT B CAS BIT –** This output transmits the ***B*** signaling bit that indicates the incoming analog signaling state.
CS	**CHIP SELECT –** This input receives the chip select signal for the SPI and UART ports.
RESET	**RESET –** This active high input must be pulled low for normal operation. When pulled momentarily high for at least 1us, (LED lights during RESET) all programmable registers in the device are reset to the states specified under power-up utilization.
POWER	**Power –** The Power LED lights when the power is applied.

Dip Switches

Dip Switches 1 through 4 correspond to the MTIFM in location 0 (Channel 0)

Switch 1 Closed	RESET0	MTIFM is held in reset.
Switch 2 Closed	CS0	Active chip-select signal to MTIFM. CS0 and CS1 should not be activated at the same time.
Switch 3 Closed	AXMT0	***A*** signaling bit to MTIFM.
Switch 4 Closed	BXMT0	***B*** signaling bit to MTIFM.

Dip Switches 5 through 8 correspond to the MTIFM in location 1 (Channel 1)

Switch 5 Closed	RESET1	MTIFM is held in reset.
Switch 6 Closed	CS1	Active chip-select signal to MTIFM. CS1 and CS0 should not be activated at the same time.
Switch 7 Closed	AXMT1	***A*** signaling bit to MTIFM.
Switch 8 Closed	BXMT1	***B*** signaling bit to MTIFM.

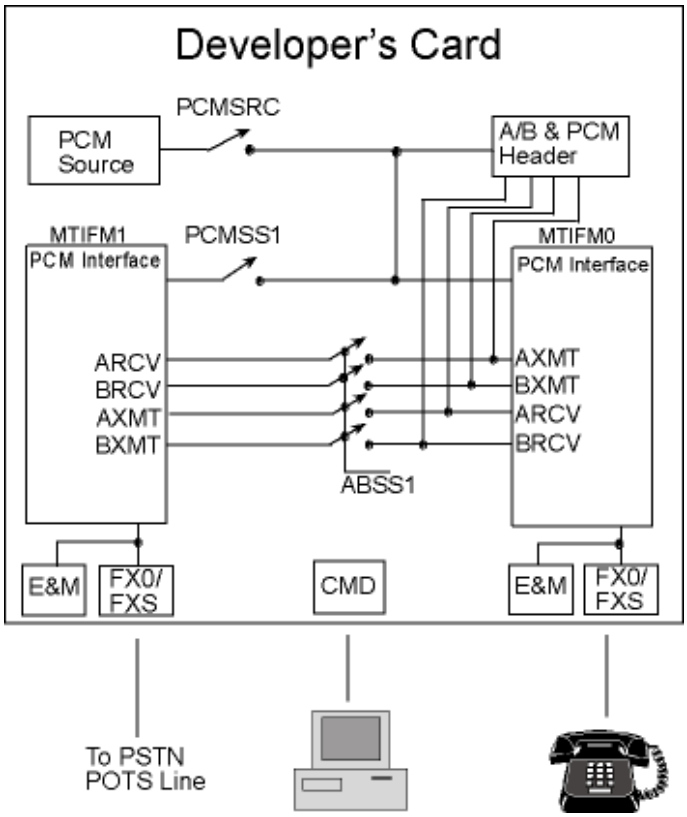
Dip Switches 9 through 12 allow flexibility in connecting the PCM source and MTIFMs

Switch 9 Closed	PCMSRC	PCM clock and frame sync sources connected to MTIFM0.
Switch 9 Open	PCMSRC	Disconnects the PCM source from MTIFM0 allowing an external source to be connected on the header pins.
Switch 10 Closed	PCMSS1	PCM signals of MTIFM1 are connected to MTIFM0. If PCMSRC is also closed, MTIFM1 and MTIFM 0 receive the PCM clock and frame sync from the on-board source.
Switch 10 Open	PCMSS1	Isolates the PCM interface of MTIFM1 from the PCM source and MTIFM0.
Switch 11 Closed	ABSS1	XMT and RCV A&B signaling bits are connected between MTIFM0 and MTIFM1. The ARCV signaling bit connects to AXMT and BRCV to BXMT in both directions.
Switch 11 Open	ABSS1	Allows A&B bit control via the header pins for MTIFM0 or Dip Switches for both MTIFMs.

Example

Using the Developer Board to Test an Application

The following block diagram shows a simple configuration that can be used to check voice quality through the MTIFMs.



To Setup the Test Card:

- Connect an analog telephone to the FXO0/FXS0 jack on the test card
- Connect a telephone cable to the FXO1/FXS1 jack on the test card. This connects the PSTN POTS line to the analog telephone through the MTIFMs.

To Configure the Module on Channel 0:

- Set Dip Switch 2 down
- Set Dip Switch 6 up
- Set Dip Switches 9 through 11 down
- Set the remaining switches up
- Then connect a COM port from your PC to the Command port jack on the test card
- Set the PC COM port for 19.2K bps in order to communicate with the test card.
- Using Hyperterminal to configure Channel 0, enter the following values:

  Important: Be sure to use upper case letters.

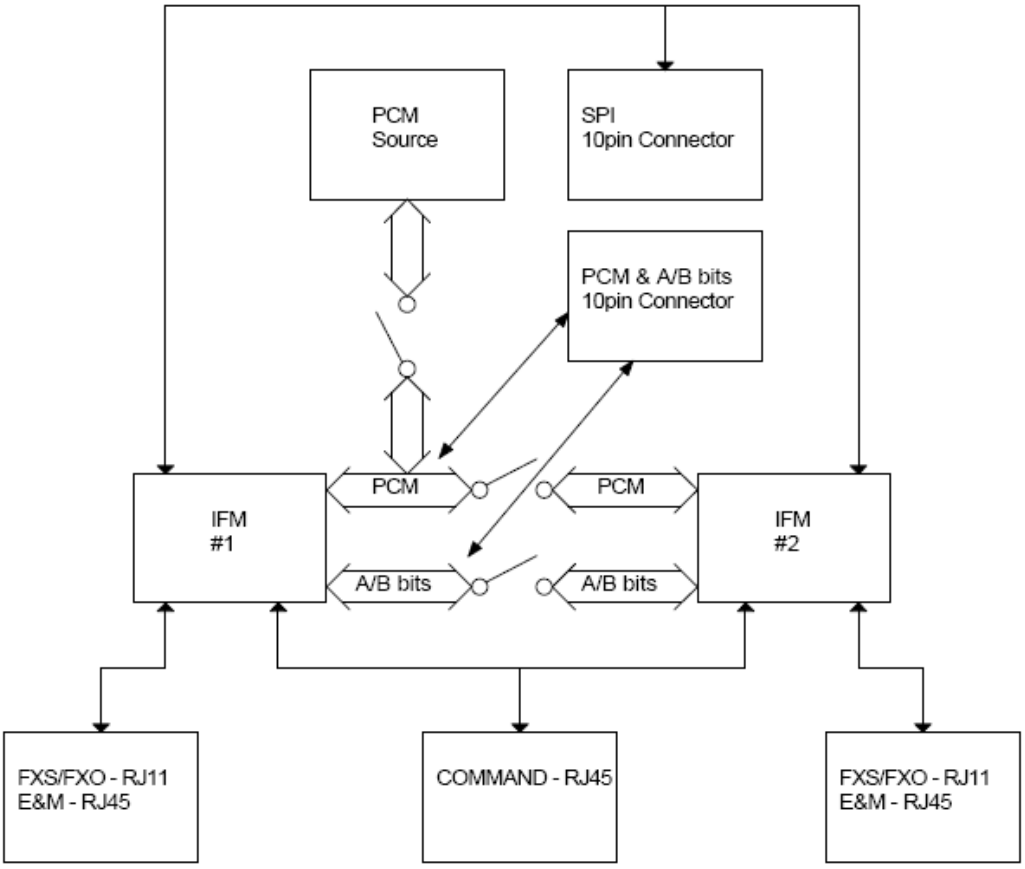
Command	Description
2002	Defaults the MTIFM
2802	Set FXS interface – Telephone
3980	PCM Receive time slot
3A81	PCM Transmit time slot

To Configure the Module on Channel 1:

- Set Dip Switch 6 down
- Set Dip Switch 2 up
- Set Dip Switches 9 through 11 down
- Set the remaining switches up
- Then enter the following values:

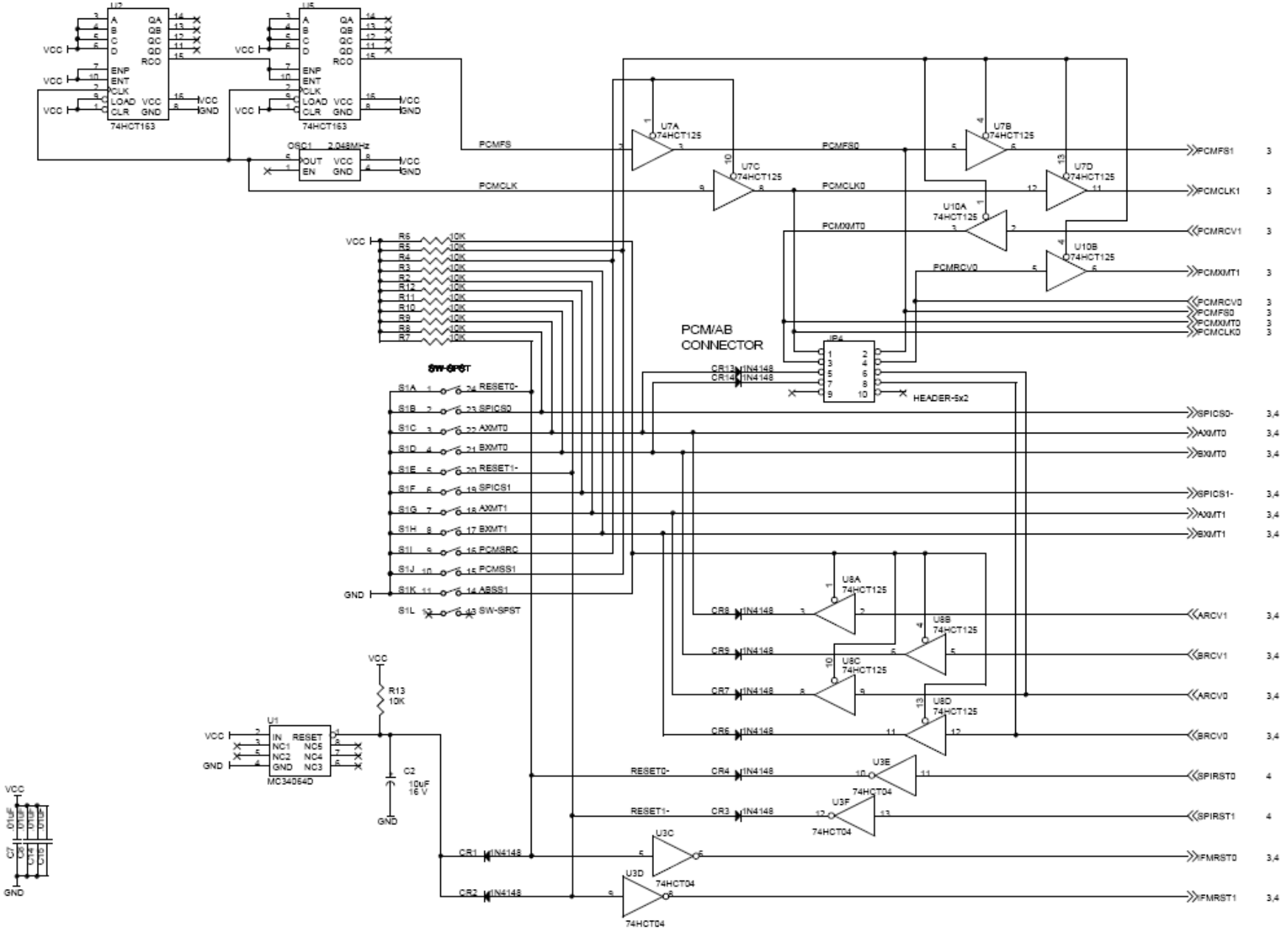
Command	Description
2002	Defaults the MTIFM
2801	Set FXO interface – Phone Line
3981	PCM Receive time slot
3A80	PCM Transmit time slot

Appendix B – SocketSLIC Developer Board Schematics and Recommended Parts

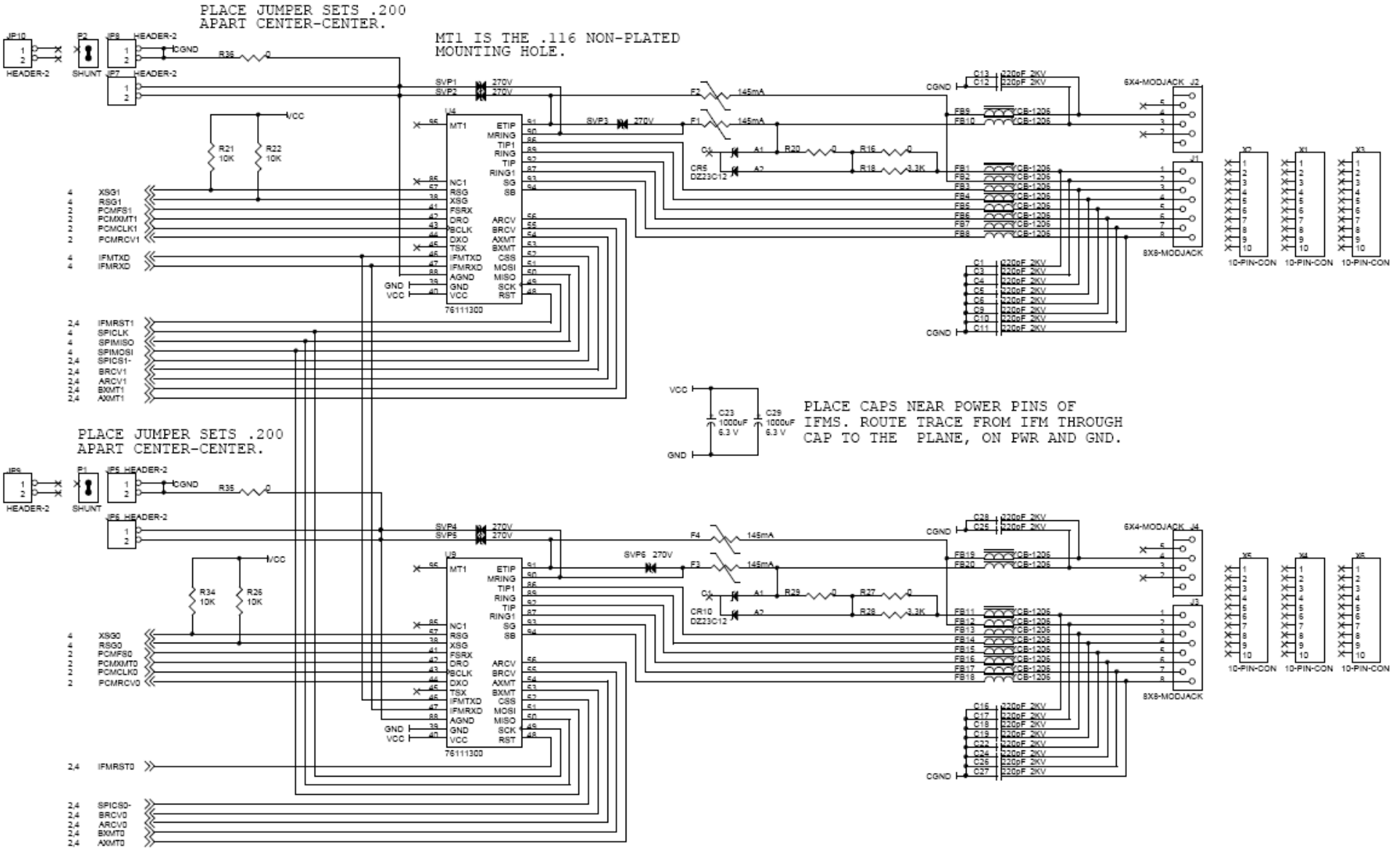


General Block Diagram

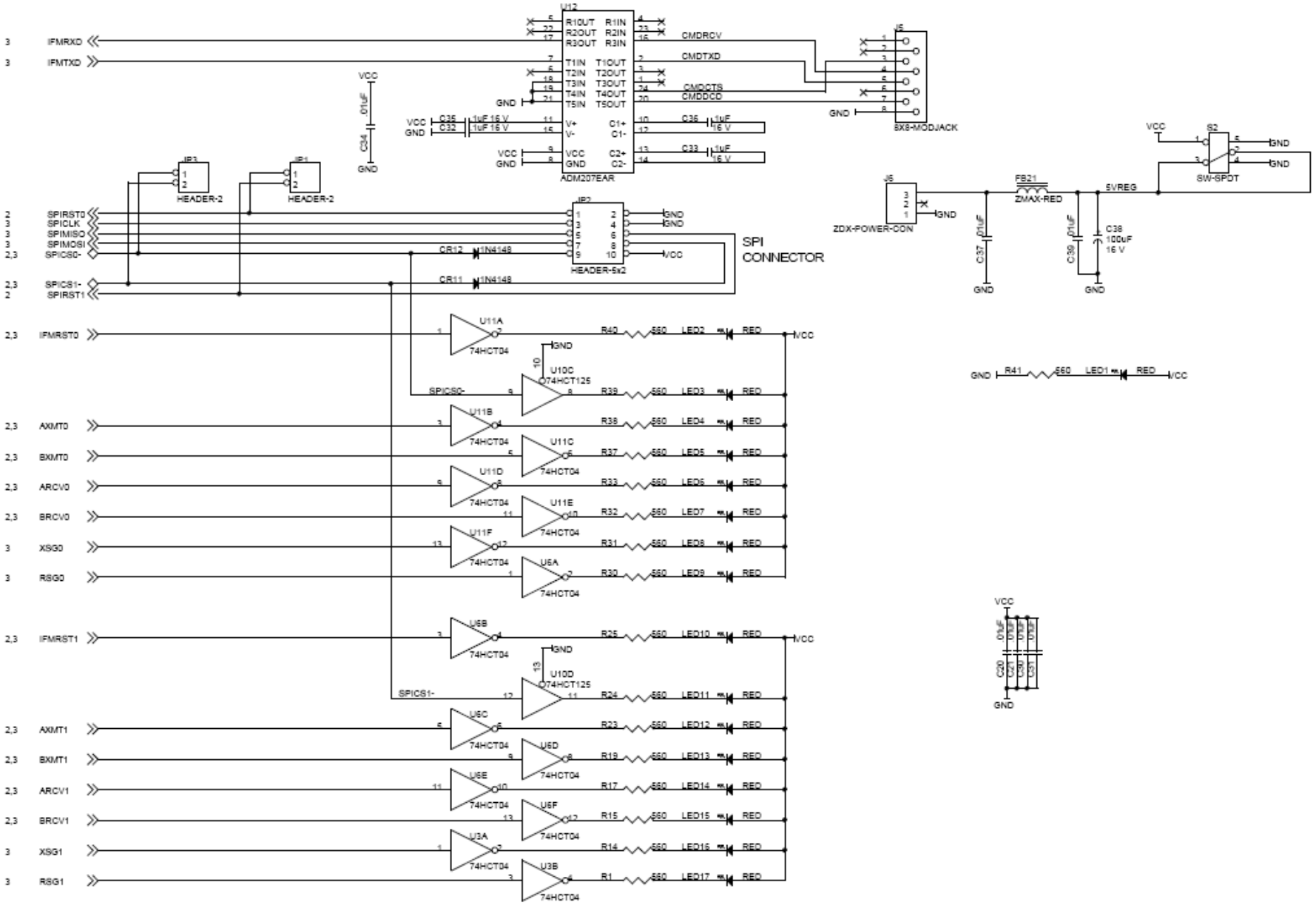
Developer Board Schematics



Developer Board Schematics



Developer Board Schematics



Recommended Parts

Disclaimer: Multi-Tech Systems makes no warranty claims for vendor product recommendations listed below. Other vendor products may or may not operate satisfactorily. Multi-Tech System's recommended vendor products only indicate that the product has been tested in controlled conditions and were found to perform satisfactorily.

Surface mount ferrites are used on T&R (Tip and Ring) to mitigate emission levels out the RJ-11 cable. 220pF capacitors are also used on T&R to reduce the common mode emissions that may be present in certain systems.

The ferrite and capacitors also aid in reducing the effects of transients that may be present on the line.

Note: These parts are RoHS compliant.

Recommended Ferrite (SMT)
Manufacturer – Associated Component Technology (ACT) Part # CBZ1206-202-30-LF
Manufacturer – Murata Erie Part # BLM31AJ601SN1L

Recommended Ferrite (Thru-Hole)
Manufacturer – Associated Component Technology (ACT) Part # WB2-2.OT

Recommended Capacitor (SMT)
Manufacturer – NOVACAP Part # ES2211N221K502NXT
Manufacturer – Murata Erie Part # GA355DR7GC221KY02L

Recommended Capacitor (Thru-Hole)
Manufacturer – Ever Grace Electronic Industrials Part # YP221K2EA7PS-8.0
Manufacturer – Murata Erie Part # DE2B3KH221KA3B
Note: Capacitors used on T&R must have the Y2 safety rating.

Recommended RJ-11 Connector
Manufacturer – Full Rise Electronic Co. Part # E5964-00P045

Recommended Sidactor Tip to Ground, Ring to Ground
Manufacturer – RayChem / Tyco Electronics Part # TVB400MSC-L
Manufacturer – ST Microelectronics Part# SMPMC-400

Recommended Sidactor Across Tip and Ring
Manufacturer – ST Microelectronics Part# SMTPA-270

Recommended Poly Switch Thermal Fuse (Thru-Hole)
Manufacturer – RayChem (Tyco Electronics) Part# TRF600-150 or TRF600-150-2

Note: The Fuse & Sidactor are required in order to comply with UL60950 for protection against over-voltages from power line cross. Fuse can be reset type.

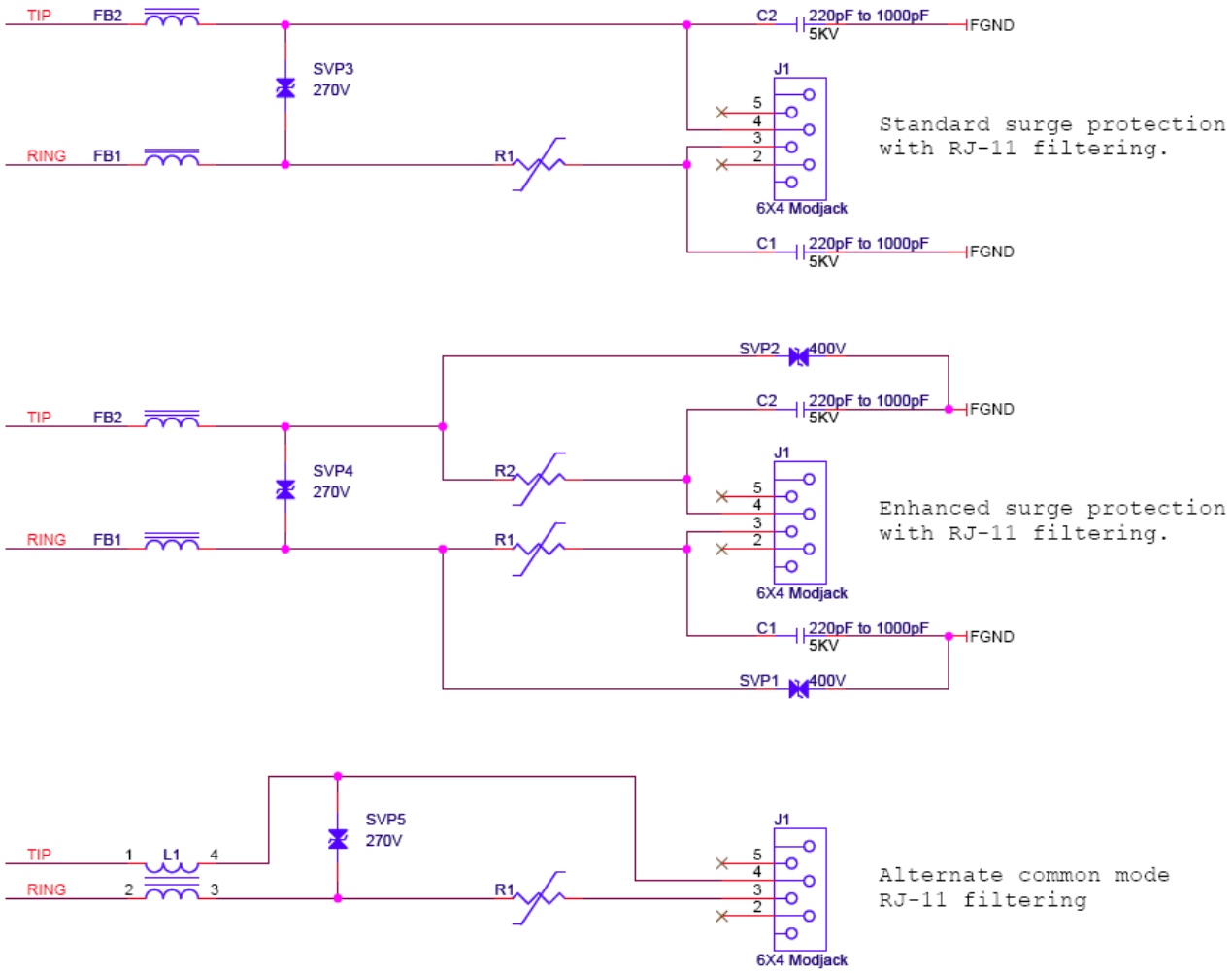
Common Mode Choke
Manufacturer – TDK Part # ZJYS51R5-2PT-01

Recommended Transceiver
Manufacturer – Analog Devices Part # ADM207EARZ

SIP Connector
Manufacturer – Neltron Industrial Co. (http://www.neltron.com.tw/) Part #2209S-xxSG
4-Pin 2.0mm SIP Socket (2 Each)
10-Pin 2.0mm SIP Socket (2 Each)

Telecom
The RJ-11 connector must meet FCC Part 68 requirements. Refer to FCC Part 68 section 68.500 subpart F for connector specifications. A self-healing fuse is used in series with line to help prevent damage to the DAA circuit. This fuse is required in order to comply with compliance regulations.

Appendix C – Tip and Ring Interface



Tip and Ring for the SocketSLIC

Appendix D – Regulatory and Compliance Statements

EMC Compliance and Requirements

EMC, Safety, and R&TTE Directive Compliance

CE

The CE mark is affixed to this product to confirm compliance with the following European Community Directives:
Council Directive 2004/108/EC of 15 December 2004 on the approximation of the laws of Member States relating to electromagnetic compatibility;
and
Council Directive 2006/95/EC of 12 December 2006 on the harmonization of the laws of Member States relating to electrical equipment designed for use within certain voltage limits;
and
Council Directive 1999/5/EC of 9 March 1999 on radio equipment and telecommunications terminal equipment and the mutual recognition of their conformity.

International Modem Restrictions

Some dialing and answering defaults and restrictions may vary for international modems. Changing settings may cause a modem to become non-compliant with national telecom requirements in specific countries. Also note that some software packages may have features or lack restrictions that may cause the modem to become non-compliant.

EMC Requirements for the United States

FCC 47 CFR Part 15 Regulations

This equipment has been tested and found to comply with the limits for a **Class A** digital device, pursuant to 47 CFR Part 15 regulations. The stated limits in this regulation are designed to provide reasonable protection against harmful interference in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Plug the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the 47 CFR rules. Operation of this device is subject to the following conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference that may cause undesired operation.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

EMC Requirements for Industry Canada

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.
Cet appareil numérique de la classe A respecte toutes les exigences du Reglement Canadien sur le matériel brouilleur.

FCC Part 68

The Federal Communications Commission (FCC) has established rules that permit this equipment to be directly connected to the public switched telephone network (PSTN). Standardized jacks are used for these connections. This equipment should not be used on party lines or coin lines.

If this equipment is malfunctioning, it may be causing harm to the telephone network. This equipment should be disconnected until the source of the problem can be determined and until repair has been made. If repair is not done, the Telephone Company may temporarily disconnect service.

The Telephone Company may make changes in its technical operations and procedures; if such changes affect the compatibility of this equipment, the Telephone Company is required to give adequate notice of the changes. You will be advised of your right to file a complaint with the FCC.

If the Telephone Company requests information on what equipment is connected to their lines, please inform them of the following:

- The Telephone Number This Unit Is Connected To (NBR #)
- The Ringer Equivalence Number (REN #)
- The Universal Service Order Code Jack Required (USOC #)
- The Service Order Code (SOC #)
- The Facility Interface Code (FIC #)
- The FCC Registration Number (FCC #)

DID Information

Notice: Allowing this equipment to be operated in such a manner as not to provide PROPER ANSWER SUPERVISION is in violation of Part 68 of the FCC – 47 CFR rules.

and

PROPER ANSWER SUPERVISION is when this equipment returns answer supervision to the PSTN when DID calls are:

- Answered by the called station
- Answered by an attendant
- Routed to a recorded announcement that can be administered by the CPE user
- Routed to a dial prompt

This equipment returns answer supervision for all direct-inward-dialing calls forwarded to the PSTN. Permissible exceptions are:

- A call is unanswered
- A busy tone is received
- A reorder tone is received

Waste Electrical and Electronic Equipment Statement

Note to OEMs: The statement is included for your information and may be used in the documentation of your final product applications.

WEEE Directive

The WEEE directive places an obligation on EU-based manufacturers, distributors, retailers, and importers to take-back electronics products at the end of their useful life. A sister Directive, ROHS (Restriction of Hazardous Substances) complements the WEEE Directive by banning the presence of specific hazardous substances in the products at the design phase. The WEEE Directive covers all Multi-Tech products imported into the EU as of August 13, 2005. EU-based manufacturers, distributors, retailers and importers are obliged to finance the costs of recovery from municipal collection points, reuse, and recycling of specified percentages per the WEEE requirements.

Instructions for Disposal of WEEE by Users in the European Union

The symbol shown below is on the product or on its packaging, which indicates that this product must not be disposed of with other waste. Instead, it is the user's responsibility to dispose of their waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or where you purchased the product.

July, 2005

Restriction of the Use of Hazardous Substances (RoHS)

Multi-Tech Systems, Inc.

Certificate of Compliance

2002/95/EC

Multi-Tech Systems Inc. confirms that its embedded products now comply with the chemical concentration limitations set forth in the directive **2002/95/EC** of the European Parliament (Restriction Of the use of certain Hazardous Substances in electrical and electronic equipment - **RoHS**)

These Multi-Tech Systems, Inc. products do not contain the following banned chemicals:

Lead, [Pb] < 1000 PPM

Mercury, [Hg] < 1000 PPM

Hexavalent Chromium, [Cr+6] < 1000 PPM

Cadmium, [Cd] < 100 PPM

Polybrominated Biphenyl, [PBB] < 1000 PPM

Polybrominated Diphenyl Ether, [PBDE] < 1000 PPM

Moisture Sensitivity Level (MSL) =1

Maximum Soldering temperature = 260C (wave only)

Notes:

1. Lead usage in some components is exempted by the following RoHS annex; therefore, higher lead concentration would be found in some SocketModems (>1000ppm).
    a. Lead in high melting temperature type solders (i.e., tin-lead solder alloys containing more than 85% lead).
    b. Lead in electronic ceramic parts (e.g., piezoelectronic devices).
2. Moisture Sensitivity Level (MSL) – Analysis is based on the components/material used on the board.

Information on HS/TS Substances According to Chinese Standards

In accordance with China's Administrative Measures on the Control of Pollution Caused by Electronic Information Products (EIP) # 39, also known as China RoHS, the following information is provided regarding the names and concentration levels of Toxic Substances (TS) or Hazardous Substances (HS) which may be contained in Multi-Tech Systems Inc. products relative to the EIP standards set by China's Ministry of Information Industry (MII).

Name of the Component	Hazardous/Toxic Substance/Elements					
	Lead (PB)	Mercury (Hg)	Cadmium (CD)	Hexavalent Chromium (CR6+)	Polybrominated Biphenyl (PBB)	Polybrominated Diphenyl Ether (PBDE)
Printed Circuit Boards	O	O	O	O	O	O
Resistors	X	O	O	O	O	O
Capacitors	X	O	O	O	O	O
Ferrite Beads	O	O	O	O	O	O
Relays/Opticals	O	O	O	O+	O	O
ICs	O	O	O	O	O	O
Diodes/ Transistors	O	O	O	O	O	O
Oscillators and Crystals	X	O	O	O	O	O
Regulator	O	O	O	O	O	O
Voltage Sensor	O	O	O	O	O	O
Transformer	O	O	O	O	O	O
Speaker	O	O	O	O	O	O
Connectors	O	O	O	O	O	O
LEDs	O	O	O	O	O	O
Screws, Nuts, and other Hardware	X	O	O	O	O	O
AC-DC Power Supplies	O	O	O	O	O	O
Software / Documentation CDs	O	O	O	O	O	O
Booklets and Paperwork	O	O	O	O	O	O
Chassis	O	O	O	O	O	O

X Represents that the concentration of such hazardous/toxic substance in all the units of homogeneous material of such component is higher than the SJ/Txxx-2006 Requirements for Concentration Limits.

O Represents that no such substances are used or that the concentration is within the aforementioned limits.

Information on HS/TS Substances According to Chinese Standards (in Chinese)

依照中国标准的有毒有害物质信息

根据中华人民共和国信息产业部 (MII) 制定的电子信息产品 (EIP)
标准 - 中华人民共和国《电子信息产品污染控制管理办法》（第 39 号），也称作中国 RoHS，下表列出了 Multi-Tech Systems, Inc. 产品中可能含有的有毒物质 (TS) 或有害物质 (HS) 的名称及含量水平方面的信息。

成分名称	有害/有毒物质/元素					
	铅 (PB)	汞 (Hg)	镉 (CD)	六价铬 (CR6+)	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板	O	O	O	O	O	O
电阻器	X	O	O	O	O	O
电容器	X	O	O	O	O	O
铁氧体磁环	O	O	O	O	O	O
继电器/光学部件	O	O	O	O	O	O
IC	O	O	O	O	O	O
二极管/晶体管	O	O	O	O	O	O
振荡器和晶振	X	O	O	O	O	O
调节器	O	O	O	O	O	O
电压传感器	O	O	O	O	O	O
变压器	O	O	O	O	O	O
扬声器	O	O	O	O	O	O
连接器	O	O	O	O	O	O
LED	O	O	O	O	O	O
螺丝、螺母以及其它五金件	X	O	O	O	O	O
交流-直流电源	O	O	O	O	O	O
软件/文档 CD	O	O	O	O	O	O
手册和纸页	O	O	O	O	O	O
底盘	O	O	O	O	O	O

X 表示所有使用类似材料的设备中有害/有毒物质的含量水平高于 SJ/Txxx-2006 限量要求。

O 表示不含该物质或者该物质的含量水平在上述限量要求之内。