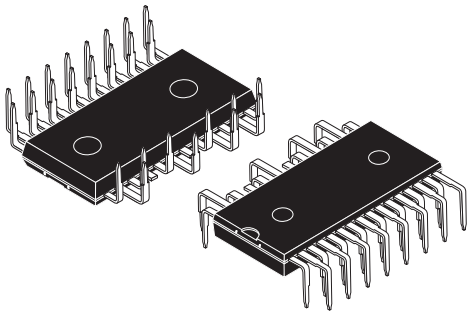
STGIPN3H60

SLLIMM™-nano small low-loss intelligent molded module IPM, 3 A, 600 V, 3-phase IGBT inverter bridge

Datasheet - production data



NDIP-26L

Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interference
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down/pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- Op-amp for advanced current sensing
- Optimized pinout for easy board layout

Applications

- 3-phase inverters for motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

Description

This SLLIMM (small low-loss intelligent molded module) nano provides a compact, high performance AC motor drive in a simple, rugged design. It is composed of six MOSFETs and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Table 1: Device summary

Order code	Marking	Package	Packing
STGIPN3H60	GIPN3H60	NDIP-26L	Tube

Contents

1 Internal schematic diagram and pin configuration

Figure 1: Internal schematic diagram

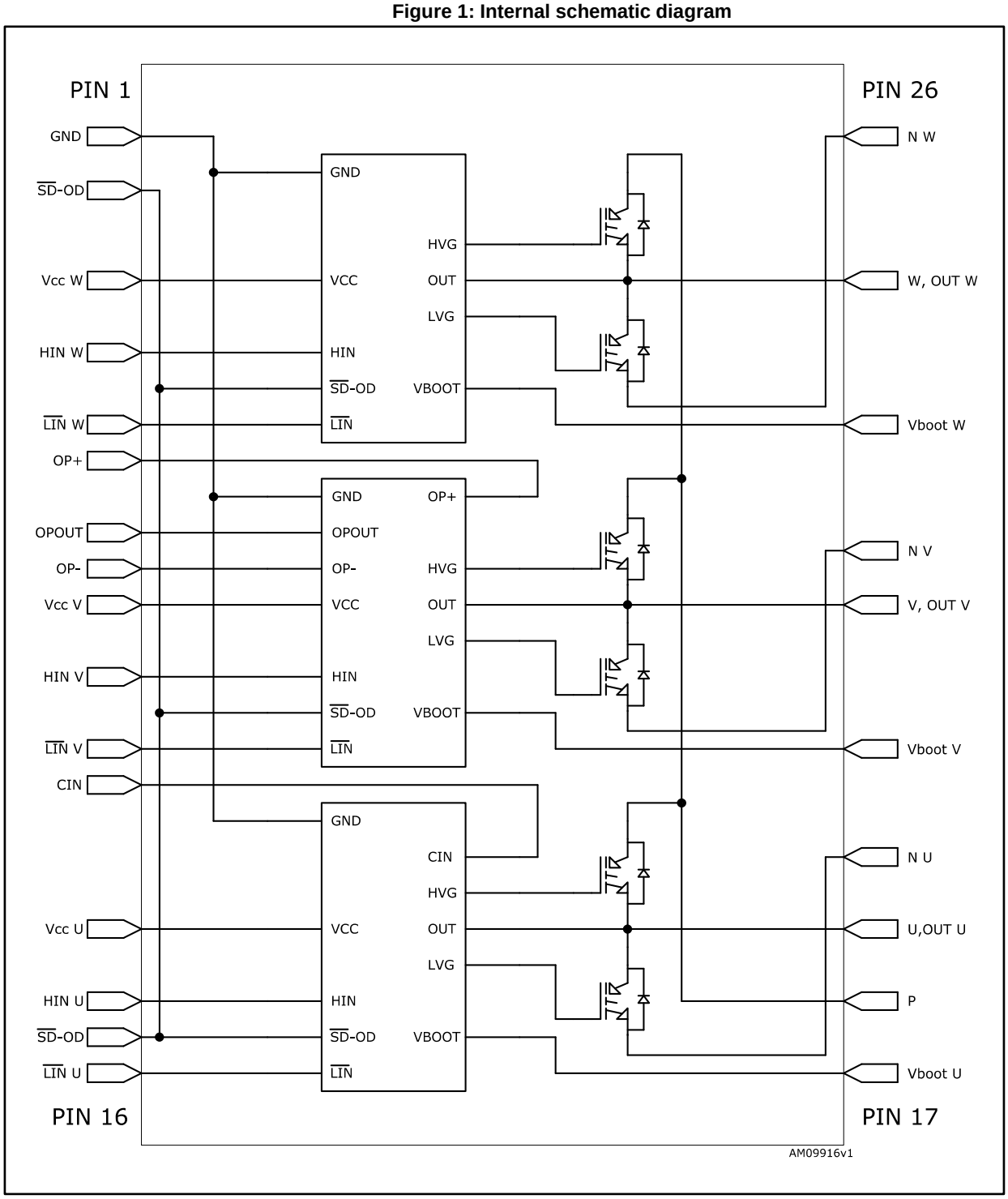
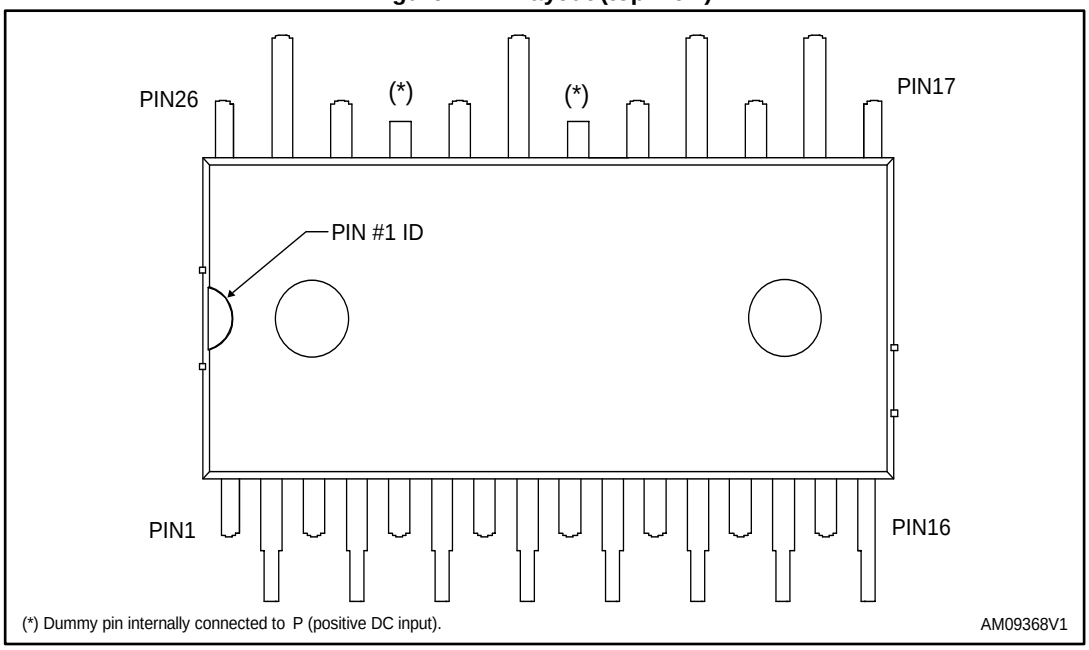


Table 2: Pin description

Pin	Symbol	Description
1	GND	Ground
2	$\overline{SD}$ / OD	Shutdown logic input (active low) / open-drain (comparator output)
3	V_{CC} W	Low voltage power supply W phase
4	HIN W	High-side logic input for W phase
5	$\overline{LIN}$ W	Low-side logic input for W phase
6	OP+	Op-amp non inverting input
7	OP_{OUT}	Op-amp output
8	OP-	Op-amp inverting input
9	V_{CC} V	Low voltage power supply V phase
10	HIN V	High-side logic input for V phase
11	$\overline{LIN}$ V	Low-side logic input for V phase
12	CIN	Comparator input
13	V_{CC} U	Low voltage power supply for U phase
14	HIN U	High-side logic input for U phase
15	$\overline{SD}$ / OD	Shutdown logic input (active low) / open-drain (comparator output)
16	$\overline{LIN}$ U	Low-side logic input for U phase
17	V_{BOOT} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT_U	U phase output
20	N_U	Negative DC input for U phase
21	V_{BOOT} V	Bootstrap voltage for V phase
22	V, OUT_V	V phase output
23	N_V	Negative DC input for V phase
24	V_{BOOT} W	Bootstrap voltage for W phase
25	W, OUT_W	W phase output
26	N_W	Negative DC input for W phase

Figure 2: Pin layout (top view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3: Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Each IGBT collector emitter voltage (V_{IN}[(1)]= 0)	600	V
± I_C[(2)]	Each IGBT continuous collector current at T_C = 25 °C	3	A
± I_{CP}[(3)]	Each IGBT pulsed collector current	18	A
P_{TOT}	Each IGBT total dissipation at T_C = 25 °C	8	W

Notes:

(1)Applied among HIN_i, $\overline{LIN}_i$ and G_{ND} for i = U, V, W.

(2)Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

(3)Pulse width limited by max. junction temperature.

Table 4: Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied among OUT_U, OUT_V, OUT_W - GND	V_{boot} - 21	V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	- 0.3	21	V
V_{CIN}	Comparator input voltage	- 0.3	V_{CC} + 0.3	V
V_{op+}	Op-amp non-inverting input	- 0.3	V_{CC} + 0.3	V
V_{op-}	Op-amp inverting input	- 0.3	V_{CC} + 0.3	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{IN}	Logic input voltage applied among HIN, $\overline{LIN}$ and GND	- 0.3	15	V
$V_{\overline{SD}/OD}$	Open-drain voltage	- 0.3	15	V
$\Delta V_{OUT/dT}$	Allowed output slew rate		50	V/ns

Table 5: Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied among each pin and heatsink plate (AC voltage, t = 60 s)	1000	V
T_j	Power chip operating junction temperature range	-40 to 150	°C
T_C	Module operation case temperature range	-40 to 125	°C

2.2 Thermal data

Table 6: Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	50	°C/W

3 Electrical characteristics

3.1 Inverter part

T_J = 25 °C unless otherwise specified.

Table 7: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 1 A	-	2.15	2.6	V
		V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 1 A, T_J = 125 °C	-	1.65		
I_{CES}	Collector cut-off current (V_{IN}(1) = 0 “logic state”)	V_{CE} = 550 V, V_{CC} = V_{Boot} = 15 V	-		250	µA
V_F	Diode forward voltage	V_{IN}(1) = 0 “logic state”, I_C = 1 A	-		1.7	V

Notes:

(1)Applied among HIN_i, $\overline{LIN}_i$ and G_{ND} for i = U, V, W ($\overline{LIN}$ inputs are active low).

Table 8: Inductive load switching time and energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}(1)	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(2) = 0 - 5 V, I_C = 1 A (see *Figure 4: "Switching time definition"*)	-	275	-	ns
$t_{c(on)}$(1)	Crossover time (on)		-	90	-	
t_{off}(1)	Turn-off time		-	890	-	
$t_{c(off)}$(1)	Crossover time (off)		-	125	-	
t_{rr}	Reverse recovery time		-	50	-	
E_{on}	Turn-on switching energy		-	18	-	µJ
E_{off}	Turn-off switching energy		-	13	-	

Notes:

(1)t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of MOSFET itself under the internally given gate driving conditions.

(2)Applied among HIN_i, $\overline{LIN}_i$ and G_{ND} for i = U, V, W ($\overline{LIN}$ inputs are active low).

Figure 3: Switching time test circuit

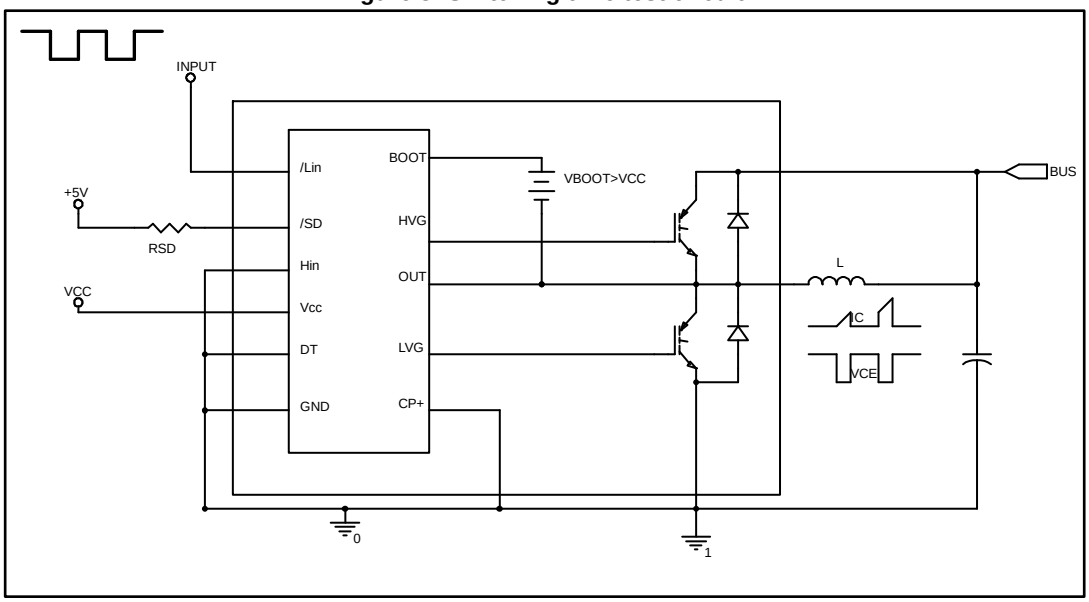


Figure 4: Switching time definition

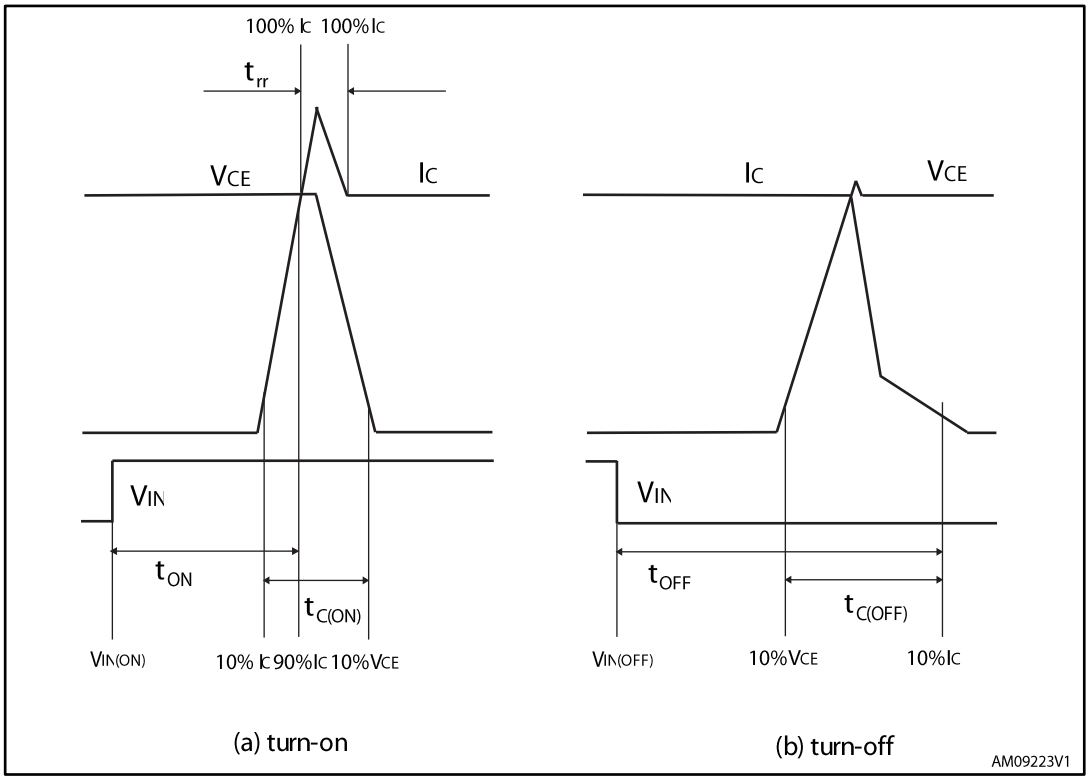


Figure 4: "Switching time definition" refers to HIN inputs (active high). For $\overline{\text{LIN}}$ inputs (active low), VIN polarity must be inverted for turn-on and turn-off.

3.2 Control part

Table 9: Low voltage power supply (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn-ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn-OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V, $\overline{SD}$ /OD = 5 V, $\overline{LIN}$ = 5 V, H_{IN} = 0, C_{IN} = 0 V			150	µA
I_{qcc}	Quiescent current	V_{cc} = 15 V, $\overline{SD}$ /OD = 5 V, $\overline{LIN}$ = 5 V, H_{IN} = 0, C_{IN} = 0 V			1	mA
V_{ref}	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

Table 10: Bootstrapped voltage (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn-ON threshold		11.1	11.5	12.1	V
V_{BS_thOFF}	V_{BS} UV turn-OFF threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} < 9 V $\overline{SD}$ /OD = 5 V, $\overline{LIN}$ and HIN = 5 V, C_{IN} = 0 V		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V $\overline{SD}$ /OD = 5 V, $\overline{LIN}$ and HIN = 5 V, C_{IN} = 0 V		200	300	µA
$R_{DS(on)}$	Bootstrap driver on-resistance	LVG ON		120		Ω

Table 11: Logic inputs (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage		0.8		1.1	V
V_{ih}	High logic level voltage		1.9		2.25	V
I_{HINh}	HIN logic “1” input bias current	HIN = 15 V	110	175	260	µA
I_{HINl}	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 0 V	3	6	20	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LINh}	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 15 V			1	µA
I_{SDh}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 15 V	30	120	300	µA
I_{SDl}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 0 V			3	µA
Dt	Dead time	see *Figure 5: "Dead time and interlocking waveform definitions"*		180		ns

Table 12: Op-amp characteristics (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V			6	mV
I_{io}	Input offset current	V_{ic} = 0 V, V_o = 7.5 V		4	40	nA
I_{ib}	Input bias current (1)			100	200	nA
V_{icm}	Input common mode voltage range		0			V
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage	R_L = 10 kΩ to GND	14	14.7		V
I_o	Output short-circuit current	Source, V_{id} = + 1 V; V_o = 0 V	16	30		mA
		Sink, V_{id} = -1 V; V_o = V_{CC}	50	80		mA
SR	Slew rate	V_i = 1 - 4 V; C_L = 100 pF; unity gain	2.5	3.8		V/µs
GBWP	Gain bandwidth product	V_o = 7.5 V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L = 2 kΩ	70	85		dB
SVR	Supply voltage rejection ratio	vs. V_{CC}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

Notes:

(1)The direction of the input current is out of the IC.

Table 13: Sense comparator characteristics (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ib}	Input bias current	V_{CIN} = 1 V			3	µA
V_{ol}	Open-drain low level output voltage	I_{od} = 3 mA			0.5	V
t_{d_comp}	Comparator delay	$\overline{SD}$ /OD pulled to 5 V through 100 kΩ resistor		90	130	ns
SR	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ		60		V/µs
t_{sd}	Shutdown to high / low-side driver propagation delay	V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0 to 3.3 V	50	125	200	ns
t_{isd}	Comparator triggering to high / low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN	50	200	250	

Table 14: Truth table

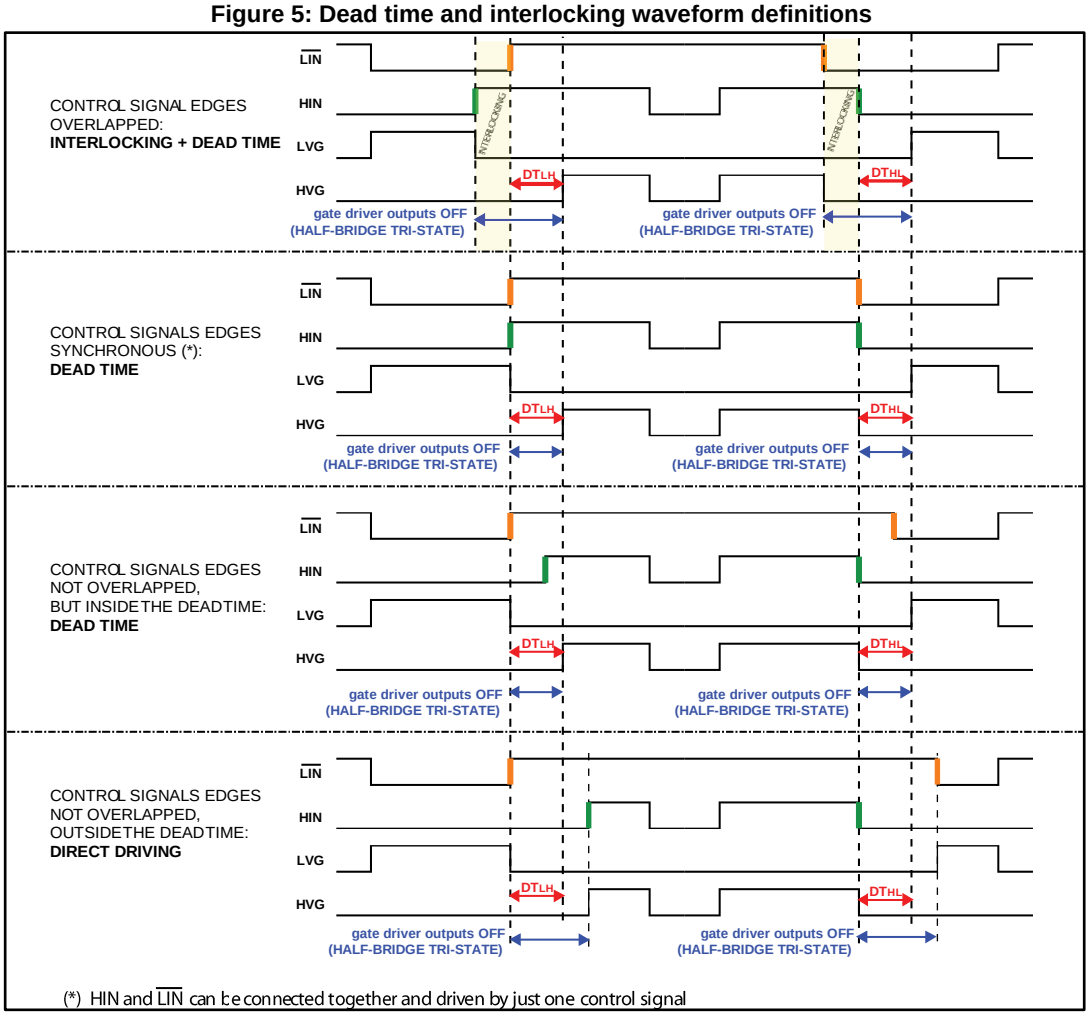
Condition	Logic input (V_i)			Output	
	$\overline{SD}$ /OD	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X(1)	X(1)	L	L
Interlocking half-bridge tri-state	H	L	H	L	L
0 “logic state” half-bridge tri-state	H	H	L	L	L
1 “logic state” low-side direct driving	H	L	L	H	L
1 “logic state” high-side direct driving	H	H	H	L	H

Notes:

(1)X: don’t care.

3.3 Waveform definitions

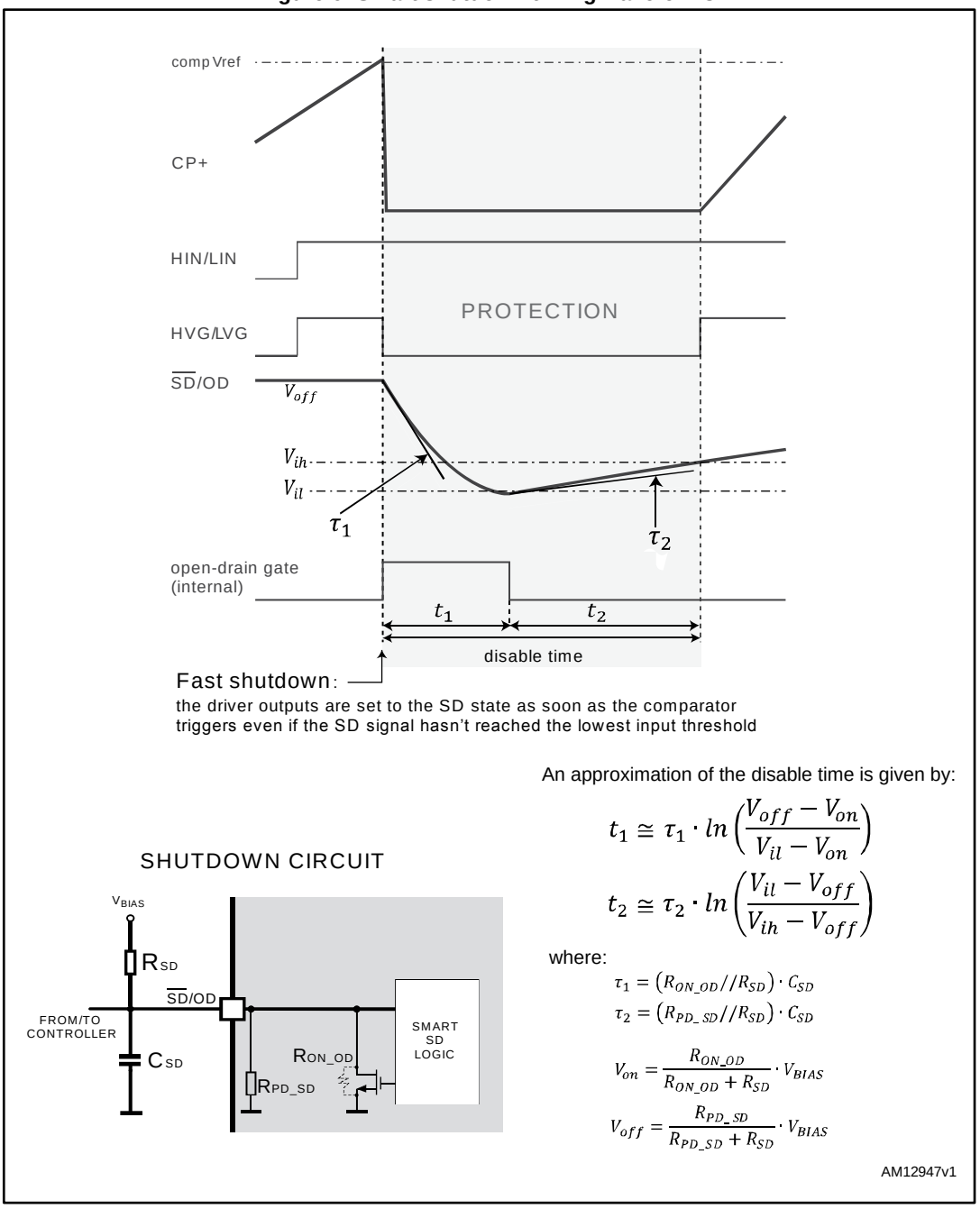
Figure 5: Dead time and interlocking waveform definitions



4 Smart shutdown function

The STGIPN3H60 integrates a comparator for fault sensing purposes. The comparator non-inverting input (C_{IN}) can be connected to an external shunt resistor so to implement a simple overcurrent protection function. When the comparator triggers, the device is set in shutdown state and both of its outputs are set to low level to lead the half-bridge to tri-state. In common overcurrent protection architectures, the comparator output is usually connected to the shutdown input through an RC network, to provide a mono-stable circuit, which implements a protection time following to the fault condition. Our smart shutdown architecture allows the output gate driver to immediately turn off in case of overcurrent, the fault signal has a preferential path, which directly switches off the outputs. The time delay between the fault and the output turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time, the internal logic turns on the open-drain output and holds it on until the shutdown voltage goes below the logic input threshold. Finally the smart shutdown function increases the real disable time without increasing the constant time of the external RC network.

Figure 6: Smart shutdown timing waveforms



An approximation of the disable time is given by:

$$t_1 \cong \tau_1 \cdot ln\left(\frac{V_{off} - V_{on}}{V_{il} - V_{on}}\right)$$

$$t_2 \cong \tau_2 \cdot ln\left(\frac{V_{il} - V_{off}}{V_{ih} - V_{off}}\right)$$

where:

$$\tau_1 = \left(R_{ON\_OD} // R_{SD}\right) \cdot C_{SD}$$

$$\tau_2 = \left(R_{PD\_SD} // R_{SD}\right) \cdot C_{SD}$$

$$V_{on} = \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{SD}} \cdot V_{BIAS}$$

$$V_{off} = \frac{R_{PD\_SD}}{R_{PD\_SD} + R_{SD}} \cdot V_{BIAS}$$

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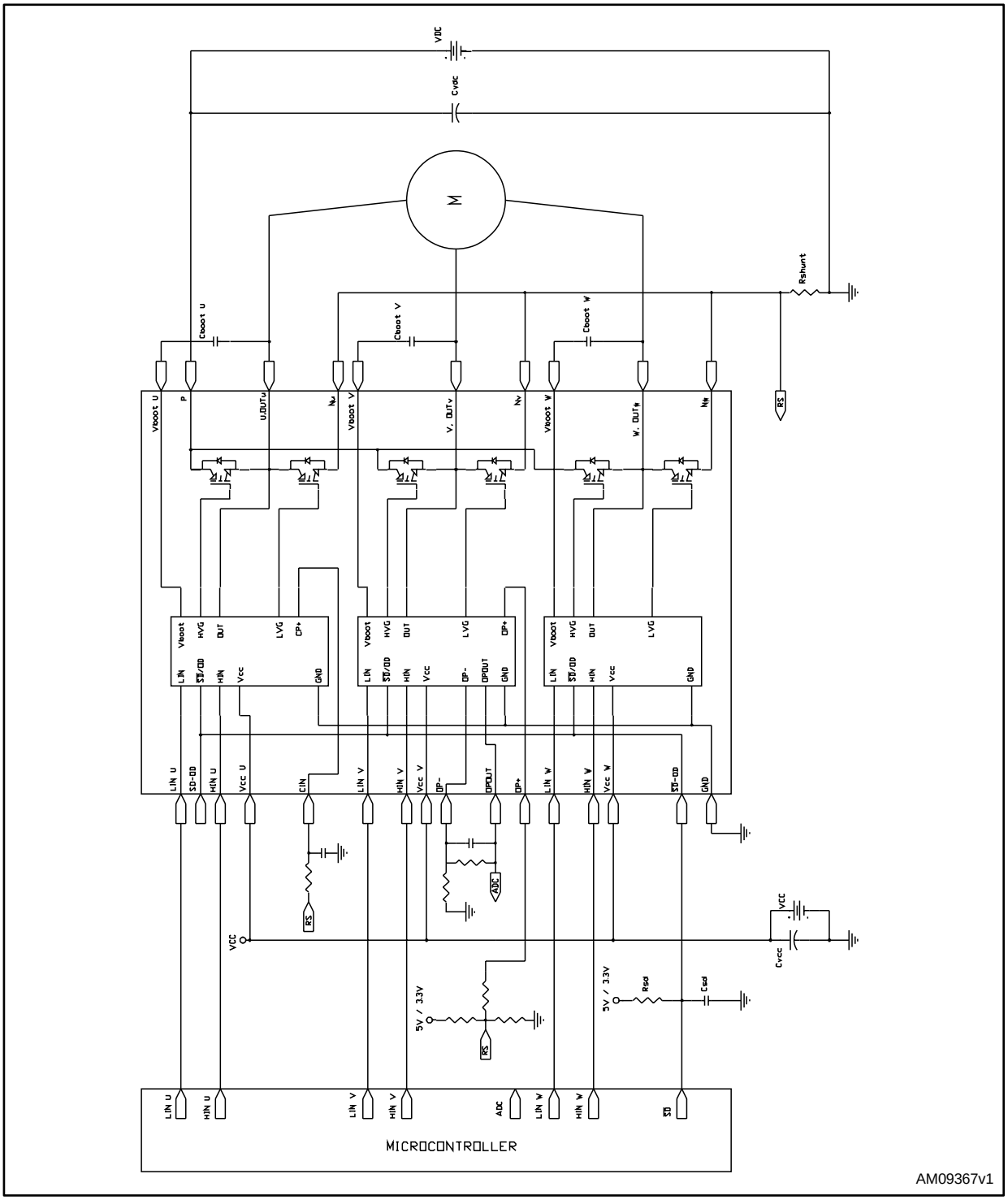
Please refer to *Table 13: "Sense comparator characteristics (VCC = 15 V unless otherwise specified)"* for internal propagation delay time details.

5 Application circuit example

Figure 7: Application circuit example



Application designers are free to use a different scheme according to the specifications of the device.

5.1 Guidelines

- Input signal HIN is active high logic. A pull-down resistor of 85 kΩ (typ.) is built-in for each high-side input. If an external RC filter is used for noise immunity, attention should be given to the variation of the input signal level.
- Input signal $\overline{\text{LIN}}$ is active low logic. A 720 kΩ (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low-side input.
- To avoid input signal oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.
- Each capacitor should be located as close as possible to pins of IPM.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitors mounted close to the module pins improve the performance.
- The $\overline{\text{SD}}$ /OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see *Section 4: "Smart shutdown function"* for detailed info).
  These guidelines ensure the specifications of the device for application designs. For further details, please refer to the relevant application note AN4043.

Table 15: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply voltage	Applied among P-Nu, Nv, Nw		300	500	V
V_{CC}	Control supply voltage	Applied to V_{CC}-GND	13.5	15	18	V
V_{BS}	High-side bias voltage	Applied to V_{BOOTi}-OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to avoid arm-short	For each input signal	1.5			µs
f_{PWM}	PWM input signal	-40 °C < T_c < 100 °C -40 °C < T_j < 125 °C			25	kHz
T_C	Case operation temperature				100	°C

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 NDIP-26L type C package information

Figure 8: NDIP-26L type C package outline

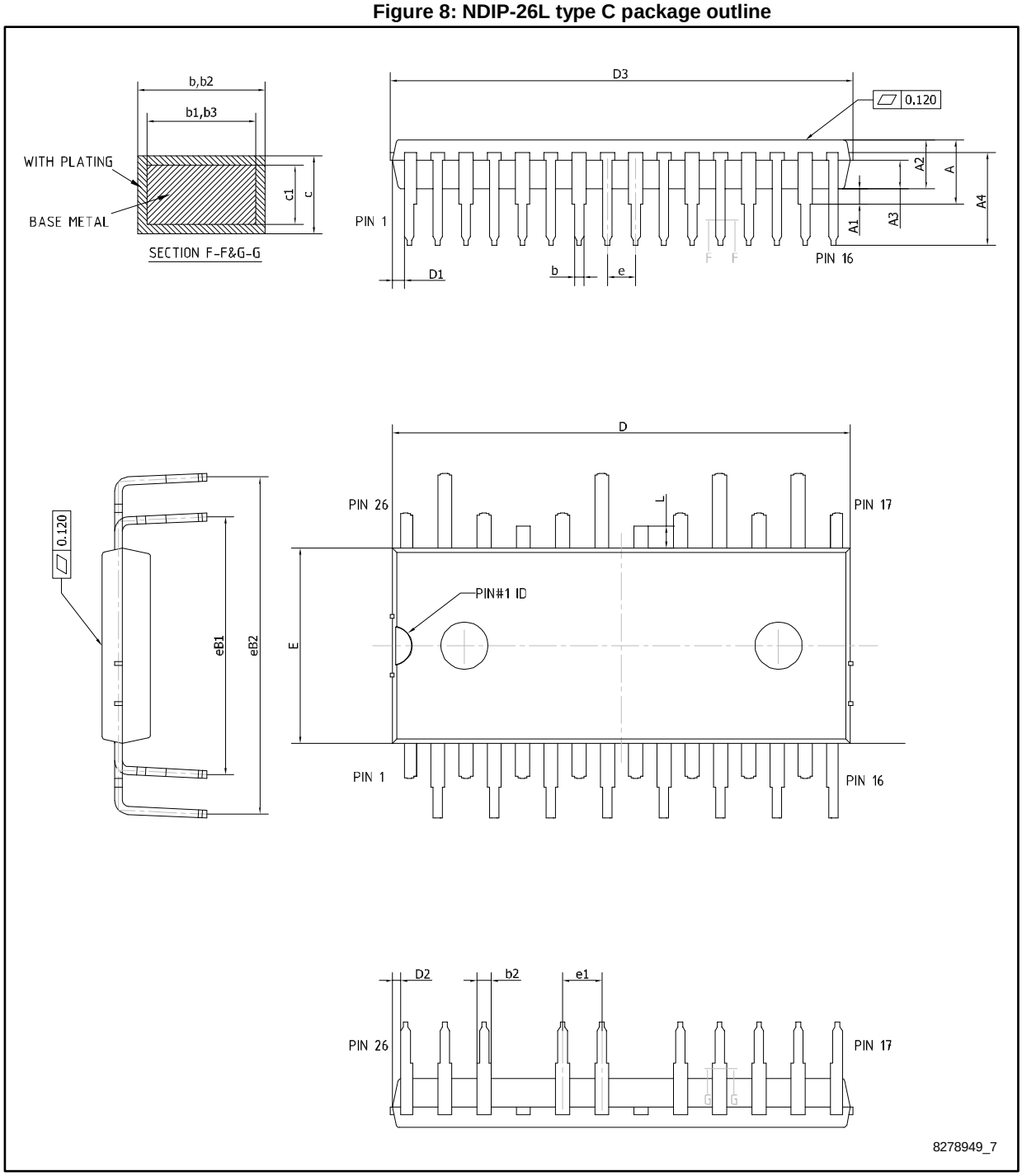


Table 16: NDIP-26L type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.40
A1	0.80	1.00	1.20
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
A4	5.70	5.90	6.10
b	0.53		0.72
b1	0.52	0.60	0.68
b2	0.83		1.02
b3	0.82	0.90	0.98
c	0.46		0.59
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.50	0.77	1.00
D2	0.35	0.53	0.70
D3			29.55
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

6.2 NDIP-26L packing information

Figure 9: NDIP-26L tube (dimensions are in mm)

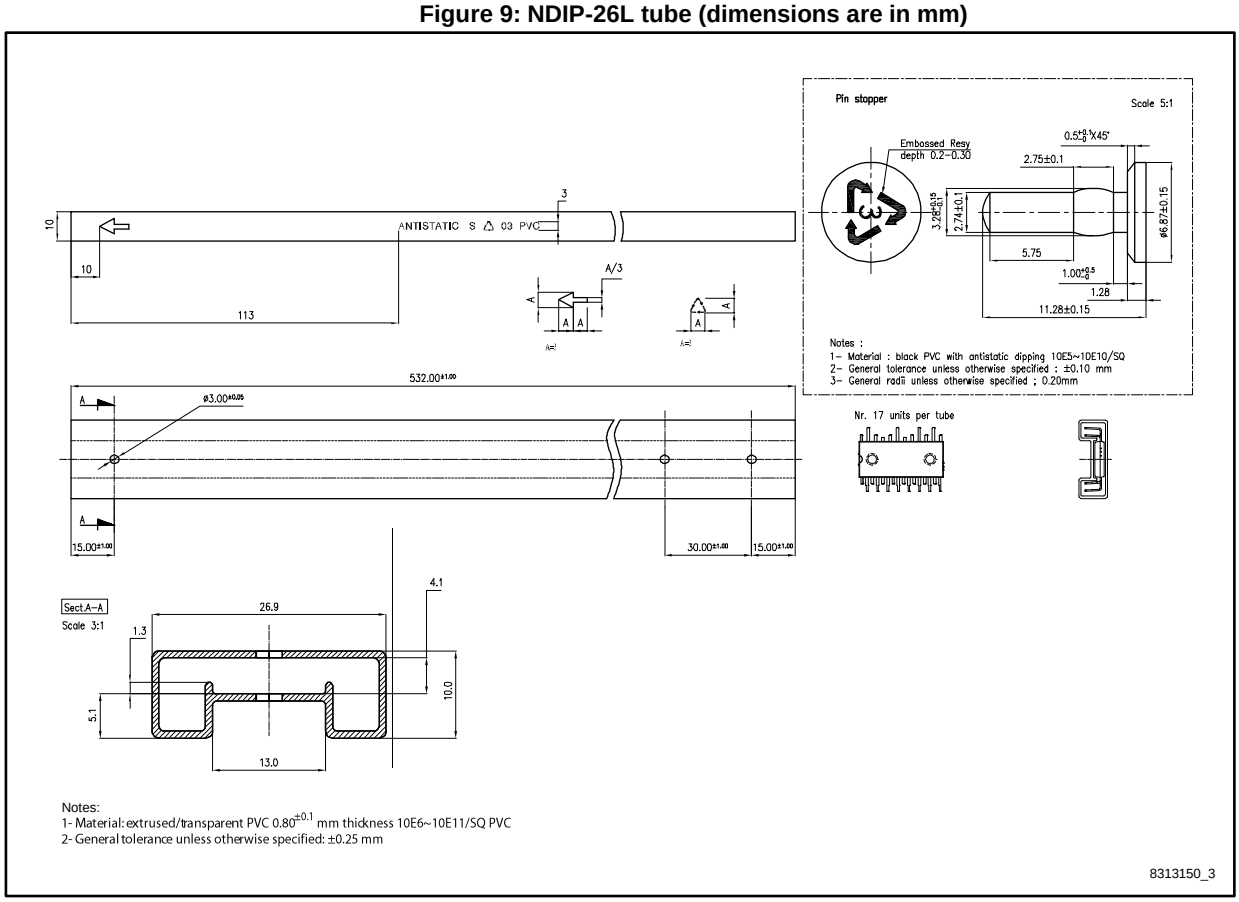


Table 17: Shipping details

Parameter	Value
Base quantity	17 pieces
Bulk quantity	476 pieces

7 Revision history

Table 18: Document revision history

Date	Revision	Changes
23-Jun-2011	1	Initial release.
23-Dec-2011	2	Document status promoted from preliminary data to datasheet. Added *Figure 9 on page 20.*
03-Jul-2012	3	Modified: Min. and Max. value *Table 4 on page 6*. Added: *Table 14 on page 17*.
14-Mar-2014	4	Updated *Figure 3: Switching time test circuit, Figure 6: Smart shutdown timing waveforms.* Updated *Table 9: Bootstrapped voltage (VCC = 15 V unless otherwise specified), Table 10: Logic inputs (VCC = 15 V unless otherwise specified)*. Updated *Section 6: Package mechanical data.*
28-Aug-2014	5	Updated unit in *Table 9: Bootstrapped voltage (VCC = 15 V unless otherwise specified)*
12-Nov-2014	6	Updated unit for Slew rate parameter in *Table 11.: OPAMP characteristics (VCC = 15 V unless otherwise specified)* Updated *6: Package mechanical data*.
16-Mar-2017	7	Updated *Section 6.1: "NDIP-26L type C package information"* and *Section 6.2: "NDIP-26L packing information"*. Minor text changes.

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