DEMO CIRCUIT 1348A
QUICK START GUIDE

LT3587EUD
High Voltage Monolithic Inverter and Dual Boost

DESCRIPTION

Demonstration Circuit 1348 is a single chip solution for applications requiring two positive and one negative high voltage supplies. The input may be a USB input or a Li-Ion battery equivalent power source.

The LT3587EUD is available in a 20-lead (3mm × 3mm) QFN surface mount package with exposed ground pad.

Design files for this circuit board are available. Call the LTC factory.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN	Bus Input Voltage Range		2.5		6.0	V
VOUT1	Output Voltage Range	IOUT1 0mA to 50mA	14.25		15.75	V
VOUT2	Output Voltage Range	IOUT2 0mA to 100mA	-7.5		-8.5	V
VOUT3	Output Voltage Voltage	IOUT3 0mA to ILIM3	23.5		26.0	V
ILIM	VOUT3 Current Limit	R_{ILIM} equals 8.04kΩ	18		22	mA

OPERATING PRINCIPLES

All three channels of the LT3587 use a constant frequency, current mode control scheme to provide voltage and/or current regulation at the output. Operation can be best understood by referring to the Block Diagram in Figure 1 of the LT3587 Data Sheet.

If EN/SS1 is pulled higher than 200mV, the bandgap reference, the start-up bias and the oscillator are turned on. At the start of each oscillator cycle, the SR latch X1 is set, which turns on the power switch Q1. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When this voltage exceeds the level at the negative input of A3, the SR latch X1 is reset, turning off the power switch Q1. The level at the negative input of A3 is set by the error amplifier A1, which is simply an amplified version of the difference between the reference of 1.24V and the feedback voltage. In this manner, the error amplifier sets the correct peak current level to keep the output voltage in regulation. If the error amplifier output increases, more current is delivered to the output: if decreased, less current is delivered.

The second channel is an inverting converter. This channel is also enabled through the EN/SS1 pin. The basic operation of this second channel is the same as the positive channel. The SR latch X2 is also set at the start of each oscillator cycle. The power switch Q2 is turned on at the same time as

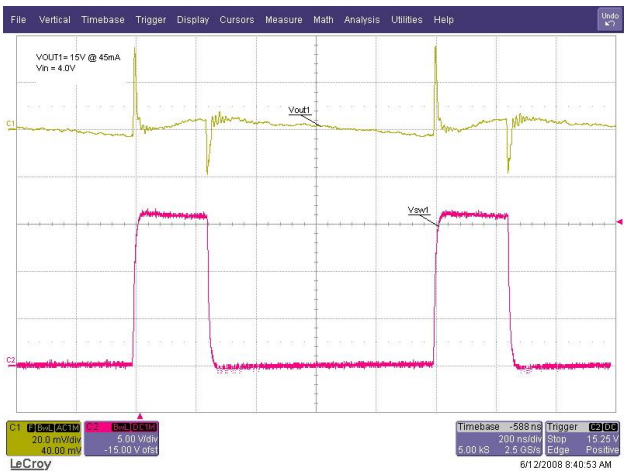
Q1. Q2 turns off based on its own feedback loop, which consists of error amplifier A2 and PWM comparator A4. The reference voltage of this negative channel is ground.

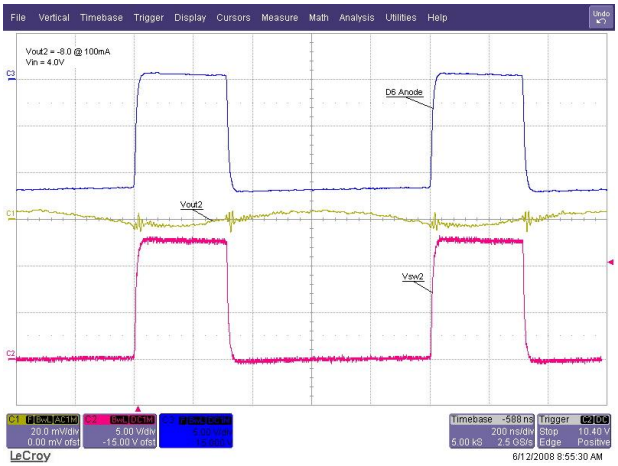
Similar to the first channel, the third channel is also a positive boost regulator. If EN/SS3 is pulled higher than 300mV, the bandgap reference, the start-up bias and the oscillators are also turned on. The SR latch X3 is set at the start of each oscillator cycle which turns on the power switch Q3. Q3 turns off based on its own feedback loop, which consists of error amplifier A5 and PWM comparator A6. The level at the negative input of A6 is set by the error ampliFer A5, and is an amplified version of the difference between the reference voltage of 0.8V and the maximum of the two feedback voltages at VFB3 and IFB3. A separate comparator (not shown) sets the maximum current limit on Q3.

The IFB3 pin is pulled up internally with a current that is (1/200) times the load current out of the VOUT3 pin. Therefore, an external resistor connected from this pin to ground generates a feedback voltage proportional to the VOUT3 output load current at the IFB3 pin. When the voltage at VFB3 is higher than the voltage at IFB3, the third channel regulates to the feedback voltage at VFB3, which in normal applications is a divided down voltage from VOUT3. In this state, the third channel behaves as a boost voltage regulator. On the other hand if the voltage at IFB3 is higher, the third channel regulates to the feedback voltage at IFB3, which therefore regulates the VOUT3 output load current to a particular value. In this state, the third channel behaves as a boost current regulator.

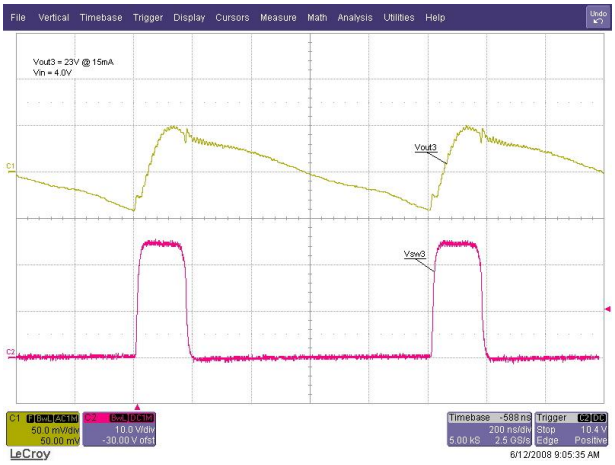
PMOS M1 is used as an output disconnect pass transistor for the first channel. M1 disconnects the load (VOUT1) from the input as long as the voltage between CAP1 and VIN is less than 2.5V (typ) and the voltage between CAP1 and VOUT1 is less than 10V (typ). Similarly, PMOS M3 is used as an output disconnect pass transistor for the third channel. M3 disconnects the load (VOUT3) from the input when the third channel is in shutdown (EN/SS3 voltage is lower than 200mV) and the voltage between CAP3 and VOUT3 is less than 10V (typ).

VOUT1 Output Ripple and Vsw1 Node





VOUT2 Output Ripple, Vsw2 and D6 Anode Nodes



VOUT3 Output Ripple and Vsw3 Node

QUICK START PROCEDURE

Using short twisted pair leads for any power connections, with all loads and power supplies off, refer to Figure 1 for the proper measurement and equipment setup.

Follow the procedure below:

1. Jumper, PS and LOAD Settings to start:
   JP1 = VIN
   JP2 (EN/SS1) = 0
   JP3 (EN/SS3) = 0
   JP4 (PULL UP) = VIN
   JP5 (FLT#) = 1
   JP6 = VS
   JP7 (IREG) = ON
   JP8 = PWM
   PS1 = OFF
   LOAD1 = OFF
   LOAD2 = OFF
   LOAD3 = OFF
2. Turn on PS1 and slowly increase voltage to 2.5V while monitoring the input current. If the current remains less than 50mA, increase PS1 to 4.0V and proceed to step 3.
3. Set JP2 (EN/SS1) to 1 and set LOAD1 to 5mA and LOAD2 to 10mA. Verify voltage on VOUT1 and VOUT2 are within the ranges of the Performance Summary.
4. Set LOAD1 to 50mA and LOAD2 to 100mA. Verify the voltages on VOUT1 and VOUT2 are within the ranges of the Performance Summary. Set LOAD1 to 5mA and LOAD2 to 10mA.
5. Set JP2 (EN/SS1) to 0, set JP3 (EN/SS3) to 1 and set LOAD3 to 2mA. Verify the voltage on VOUT3 is within the range of the Performance Summary.
6. Set LOAD3 to 15mA and verify the voltage on VOUT3 is within the range of the Performance Summary.
7. Increase LOAD3 until VOUT3 drops below 23.0V and verify IOUT3 is within the range of ILIM of the Performance Summary.
8. Set LOAD3 to 2mA. Connect a jumper from the VIN turret to the PWM turret and verify that the six LED's are on.
9. Remove the jumper from the VIN turret to the PWM turret, set JP8 to ON and verify that the six LED's are on. Turn PS1 off.
10. Connect a jumper from the VIN turret to the BAT turret. Set JP1 to BAT, turn PS1 on and verify that the six LED's are on.
11. Set JP5 (FLT#) to 0 and then return JP5 (FLT#) to 1, verify that the FLT# LED is on and that the six LED's are off.
12. Turn off PS1. Remove the jumper from VIN turret to BAT turret, Set JP1 to VIN and JP8 to PWM.
13. Set JP2 (EN/SS1) and JP3 (EN/SS3) to 0. Turn on PS1 and set to 4.0V. Verify VOUT1, VOUT2 and VOUT3 are off.
14. Set JP2 (EN/SS1) and JP3 (EN/SS3) to 1. Verify VOUT1, VOUT2 and VOUT3.
15. Turn off PS1.

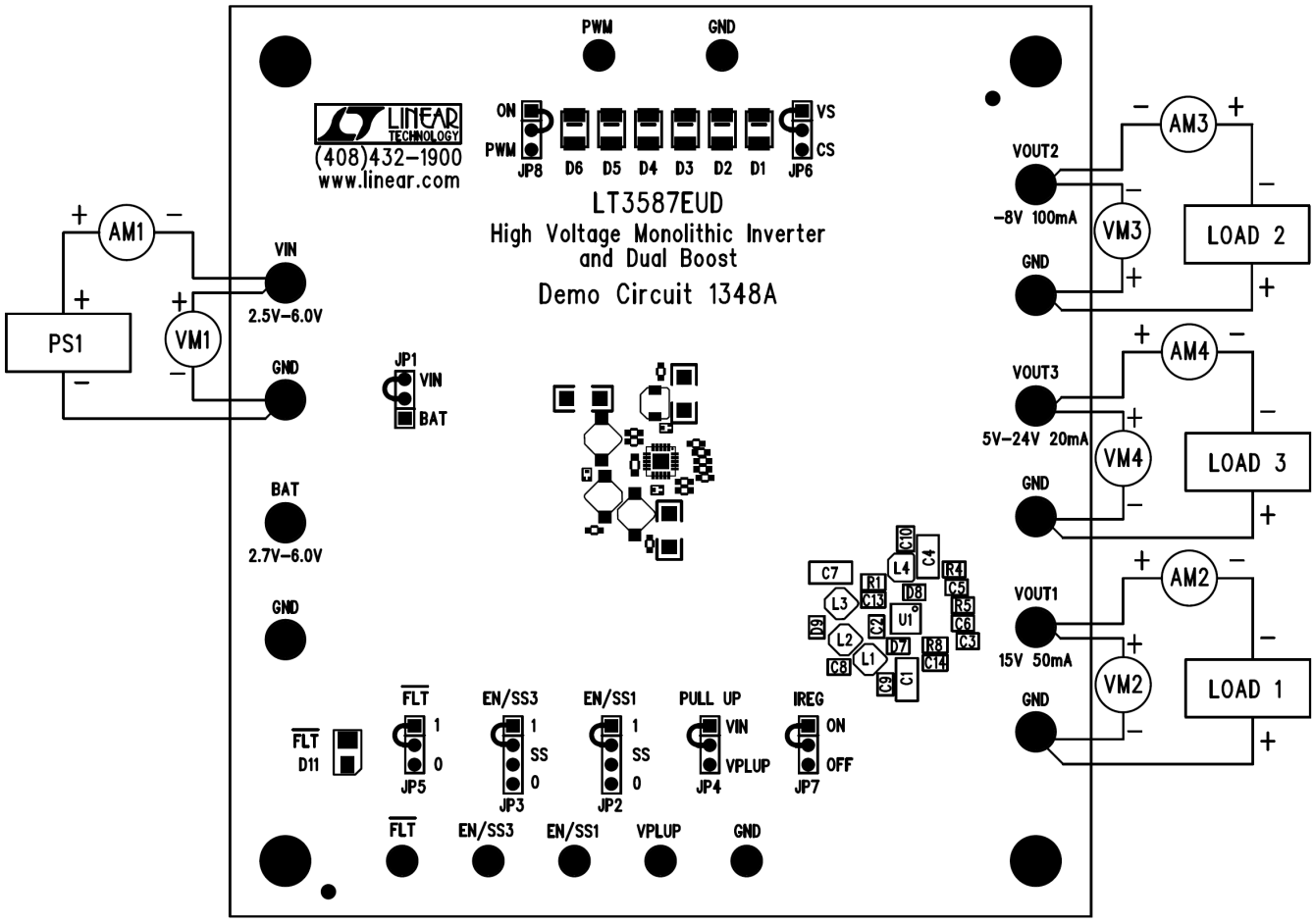


Figure 1. Proper Measurement Equipment Setup

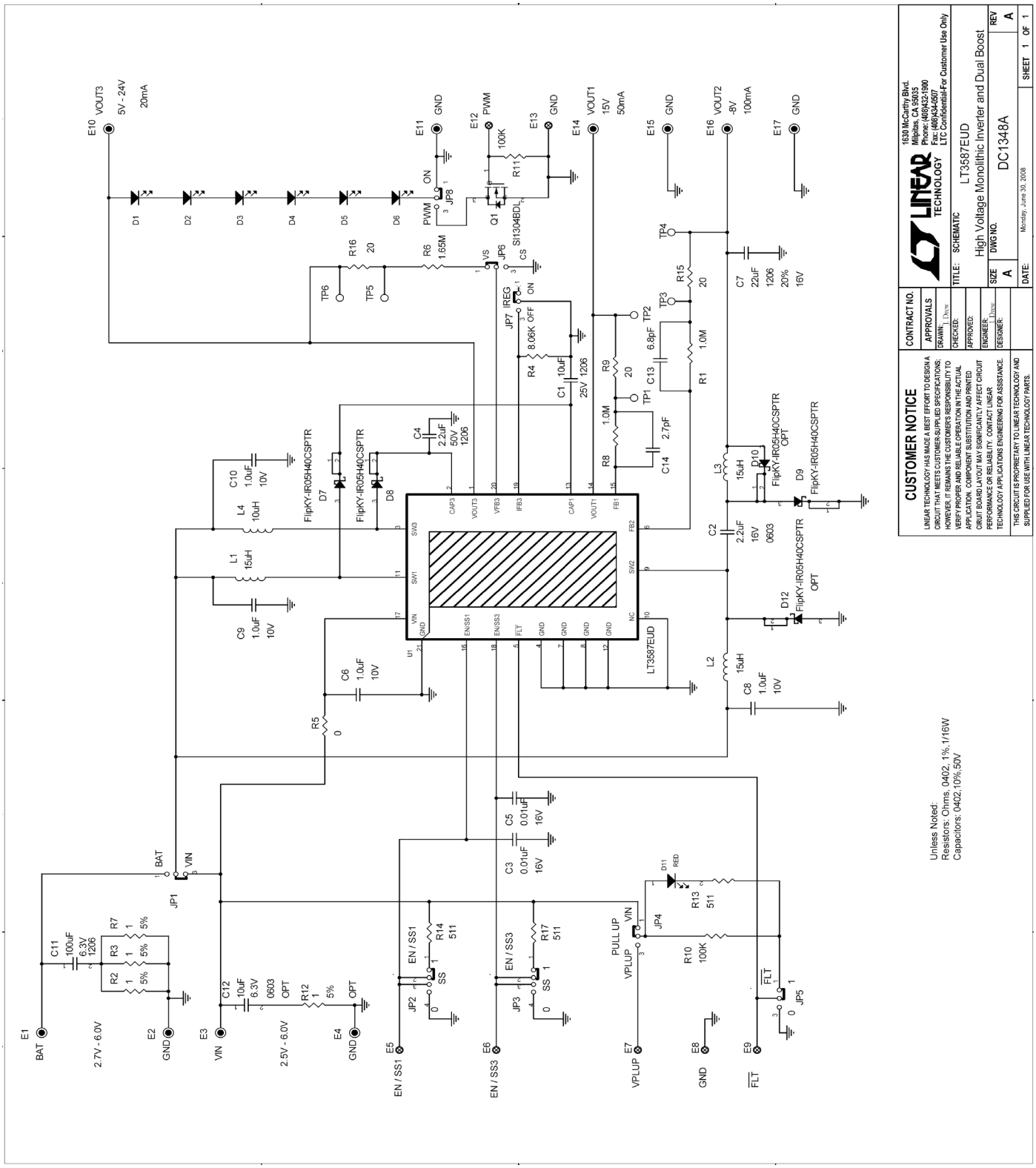


Figure 2: Schematic diagram

	Qty	Reference	Part Description	Manufacture / Part #
				NUMBER OF BOARDS =
REQUIRED CIRCUIT COMPONENTS:				
1	1	C1	CAP, CHIP, X5R, 10µF, ±10%, 25V, 1206	TAIYO YUDEN, TMK316BJ106KL-T
2	1	C2	CAP, CHIP, X5R, 2.2µF, ±10%, 16V, 0603	MURATA, GRM188R61C225KE15D
3	2	C3,C5	CAP, CHIP, X5R, 0.01µF, ±10%, 16V, 0402	MURATA, GRM155R71C103KA01D
4	1	C4	CAP, CHIP, X5R, 2.2µF, ±10%, 50V, 1206	MURATA, GCM31CR71H225KA55L
5	1	C7	CAP, CHIP, X5R, 22µF, ±20%, 16V, 1206	TAIYO YUDEN, EMK316BJ226ML-T
6	4	C6,C8,C9,C10	CAP, CHIP, X5R, 1.0µF, ±10%, 10V, 0402	MURATA, GRM155R61A105KE15D
7	1	C13	CAP, CHIP, COG, 6.8pF,10%, 50V, 0402	AVX, 04025A6R8KAT2A
8	1	C14	CAP, CHIP, COG, 2.7pF 10%, 50V, 0402	AVX, 04025A2R7KAT2A
9	6	D1,D2,D3,D4,D5,D6	DIODE, LED, WHITE	NICHIA, NSSW100
10	3	L1,L2,L3	IND, SMT, 15µH, 0.5A, ±20%,	SUMIDA, CDRH2D18/HP-150N
11	1	L4	IND, SMT,10µH, 0.7A, 20%	TOKO, 1071AS-100M
12	2	R1,R8	RES, CHIP, 1MΩ, 200ppm, 1/20W, 1%, 0402	VISHAY, CRCW04021M00FKED
13	1	R4	RES, CHIP, 8.06kΩ, 200ppm, 1/20W, 1%, 0402	VISHAY, CRCW04028K06FKED
14	1	R5	RES, CHIP, 0Ω, 1/20W, 0402	VISHAY, CRCW04020000Z0ED
15	1	R6	RES, CHIP, 1.65MΩ, 200ppm, 1/20W, 1%, 0402	VISHAY, CRCW04021M65FKED
16	1	U1	IC, SMT, HV Monolithic Inverter and Dual Boost	LTC, LT3587EUD
ADDITIONAL DEMO BOARD CIRCUIT COMPONENTS:				
1	3	D7,D8,D9	DIODE, SCHOTTKY 40V 0.5A	VISHAY, IR05H40CSPTRPBF
2	1	D11	LED, RED	PANASONIC, LN1251-C-TR
3	4	R2,R3,R7,R12	RES, CHIP, 1.0Ω, 200ppm, 1/16W, 5%, 0402	VISHAY, CRCW04021R00JNED
4	3	R9,R15,R16	RES, CHIP, 20.0Ω, 200ppm, 1/16W, 5%, 0402	VISHAY, CRCW040220R0JNED
5	2	R10,R11	RES, CHIP, 100kΩ, 200ppm, 1/20W, 1%, 0402	VISHAY, CRCW0402100KFNED
6	3	R13,R14,R17	RES, CHIP, 511Ω, 200ppm, 1/20W, 1%, 0402	VISHAY, CRCW04025116FKED
7	1	Q1	MOSFET NCHAN, 30V	VISHAY SILICONIX, SI1304BDL-T1-E3
HARDWARE FOR DEMO BOARD ONLY:				
1	10	E1,E2,E3,E4,E10,E11,E14, E15,E16,E17	Turret, 0.09"	MIL-MAX, 2501-2
2	7	E5,E6,E7,E8,E9,E12 E13	Turret, 0.061"	MIL-MAX, 2308-2
3	6	JP1,JP4,JP5,JP6,JP7, JP8	3 Pin Jumper, 2mm	SAMTEC, TMM-103-02-L-S
4	2	JP2,JP3	4 Pin Jumper, 2mm	SAMTEC, TMM-104-02-L-S
5	8	JP1,JP2,JP3,JP4,JP5,JP6, JP7,JP8	SHUNT 2mm	SAMTEC, 2SN-BK-G

Bill of Materials