24AA515/24LC515/24FC515

512K I²C™ CMOS Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
24AA515	1.8-5.5V	400 kHz†	I
24LC515	2.5-5.5V	400 kHz	I
24FC515	2.5-5.5V	1 MHz	I

†100 kHz for VCC < 2.5V.

Features:

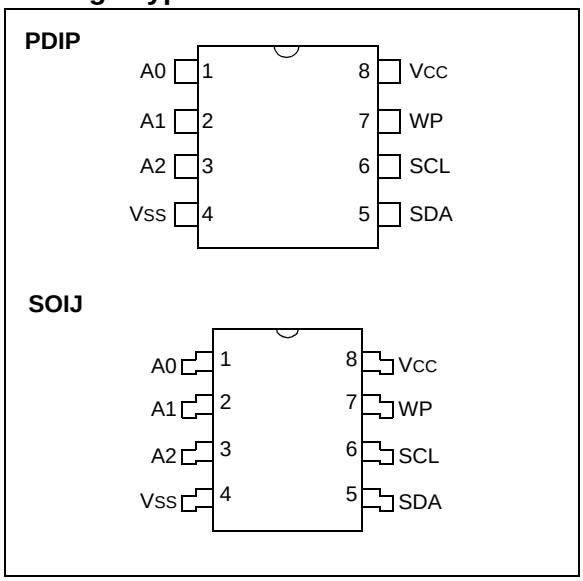
- Single Supply with Operation Down to 1.7V for 24AAXX Devices, 2.5V for 24LCXX Devices
- Low-Power CMOS Technology:
  - Active current 500 uA, typical
  - Standby current 100 nA, typical
- 2-Wire Serial Interface, I²C™ Compatible
- Cascadable up to Four Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Page Write Time 5 ms max.
- Self-Timed Erase/Write Cycle
- 64-Byte Page Write Buffer
- Hardware Write Protect
- ESD Protection >4000V
- More than 1 Million Erase/Write Cycles
- Data Retention >200 years
- Factory Programming Available
- Packages Include 8-lead PDIP, SOIJ
- Pb-Free and RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E):-40°C to +125°C

Description:

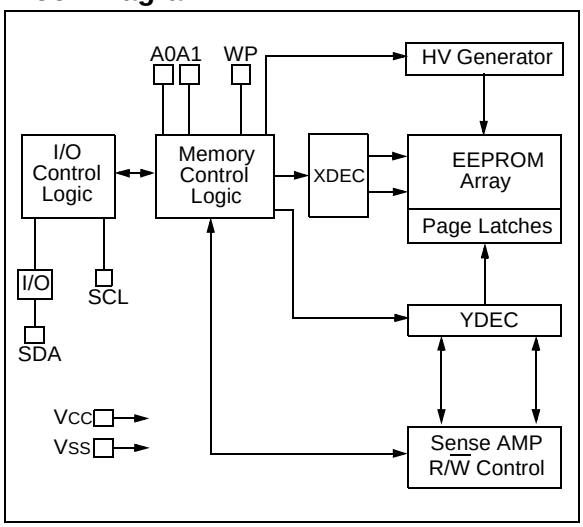
The Microchip Technology Inc. 24AA515/24LC515/24FC515 (24XX515*) is a 64K x 8 (512K bit) Serial Electrically Erasable PROM, capable of operation across a broad voltage range (1.7V to 5.5V). It has been developed for advanced, low-power applications such as personal communications or data acquisition. This device has both byte write and page write capability of up to 64 bytes of data. This device is capable of both random and sequential reads.

Reads may be sequential within address boundaries 0000h to 7FFFh and 8000h to FFFFh. Functional address lines allow up to four devices on the same data bus. This allows for up to 2 Mbits total system EEPROM memory. This device is available in the standard 8-pin plastic DIP and SOIJ packages.

Package Type



Block Diagram



*24XX515 is used in this document as a generic part number for the 24AA515/24LC515/24FC515 devices.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
		A0, A1, SCL, SDA and WP pins:				
D1	VIH	High-level input voltage	0.7 VCC	—	V	
D2	VIL	Low-level input voltage	—	0.3 VCC 0.2 VCC	V V	VCC ≥ 2.5V VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC	—	V	VCC ≥ 2.5V **(Note)**
D4	VOL	Low-level output voltage	—	0.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
D5	ILI	Input leakage current	—	±1	µA	VIN = VSS or VCC, WP = VSS VIN = VSS or VCC, WP = VCC
D6	ILO	Output leakage current	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V **(Note)** TA = 25°C, FCLK = 1 MHz
D8	ICC Read	Operating current	—	500	µA	VCC = 5.5V, SCL = 400 kHz
	ICC Write		—	3	mA	VCC = 5.5V
D9	Iccs	Standby current	—	5	µA	SCL = SDA = VCC = 5.5V A0, A1, WP = VSS, A2 = VCC

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): V_{CC} = +1.7V to 5.5V T_A = -40°C to +85°C			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— — —	100 400 1000	kHz	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
2	T_{HIGH}	Clock high time	4000 600 500	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
3	T_{LOW}	Clock low time	4700 1300 500	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
4	T_R	SDA and SCL rise time **(Note 1)**	— — —	1000 300 300	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
5	T_F	SDA and SCL fall time **(Note 1)**	— —	300 100	ns	All except, 24FC515 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
6	$T_{HD:STA}$	Start condition hold time	4000 600 250	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
7	$T_{SU:STA}$	Start condition setup time	4700 600 250	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
8	$T_{HD:DAT}$	Data input hold time	0	—	ns	**(Note 2)**
9	$T_{SU:DAT}$	Data input setup time	250 100 100	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
10	$T_{SU:STO}$	Stop condition setup time	4000 600 250	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
11	$T_{SU:WP}$	WP setup time	4000 600 600	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
12	$T_{HD:WP}$	WP hold time	4700 1300 1300	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
13	T_{AA}	Output valid from clock **(Note 2)**	— — —	3500 900 400	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
14	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	4700 1300 500	— — —	ns	1.7V ≤ Vcc ≤ 2.5V 2.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc ≤ 5.5V (24FC515 only)
15	T_{OF}	Output fall time from V_{IH} minimum to V_{IL} maximum C_B ≤ 100 pF	10 + 0.1C_B	250 250	ns	All except, 24FC515 **(Note 1)** 24FC515 **(Note 1)**
16	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except, 24FC515 **(Notes 1 and 3)**
17	T_{WC}	Write cycle time (byte or page)	—	5	ms	
18		Endurance	1 M	—	cycles	25°C **(Note 4)**

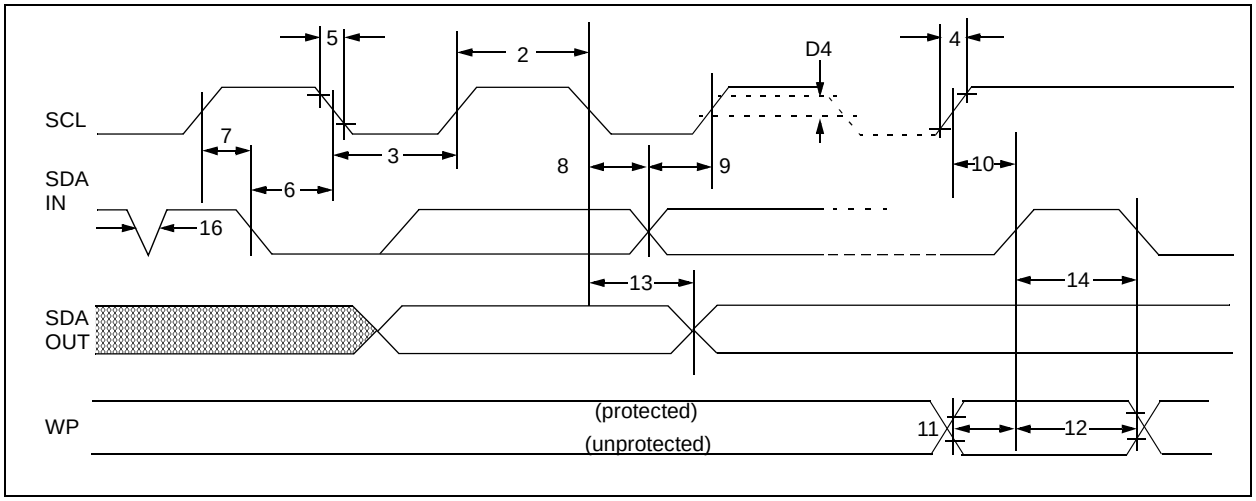
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIJ	Function
A0	1	1	User Configurable Chip Select
A1	2	2	User Configurable Chip Select
A2	3	3	Non-Configurable Chip Select. This pin must be hard wired to logical 1 state (VCC). Device will not operate with this pin left floating or held to logical 0 (VSS).
VSS	4	4	Ground
SDA	5	5	Serial Data
SCL	6	6	Serial Clock
WP	7	7	Write-Protect Input
VCC	8	8	+1.7 to 5.5V (24AA515) +2.5 to 5.5V (24LC515) +2.5 to 5.5V (24FC515)

2.1 A0, A1 Chip Address Inputs

The A0, A1 inputs are used by the 24XX515 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to four devices may be connected to the same bus by using different Chip Select bit combinations. In most applications, the chip address inputs A0 and A1 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

2.2 A2 Chip Address Input

The A2 input is non-configurable Chip Select. This pin must be tied to VCC in order for this device to operate.

2.3 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.4 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

2.5 Write-Protect (WP)

This pin must be connected to either VSS or VCC. If tied to VSS, write operations are enabled. If tied to VCC, write operations are inhibited but read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24XX515 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus must be controlled by a master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions while the 24XX515 works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX515 does not generate any Acknowledge bits if an internal programming cycle is in progress, however, the control byte that is being polled must match the control byte used to initiate the write cycle.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX515) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

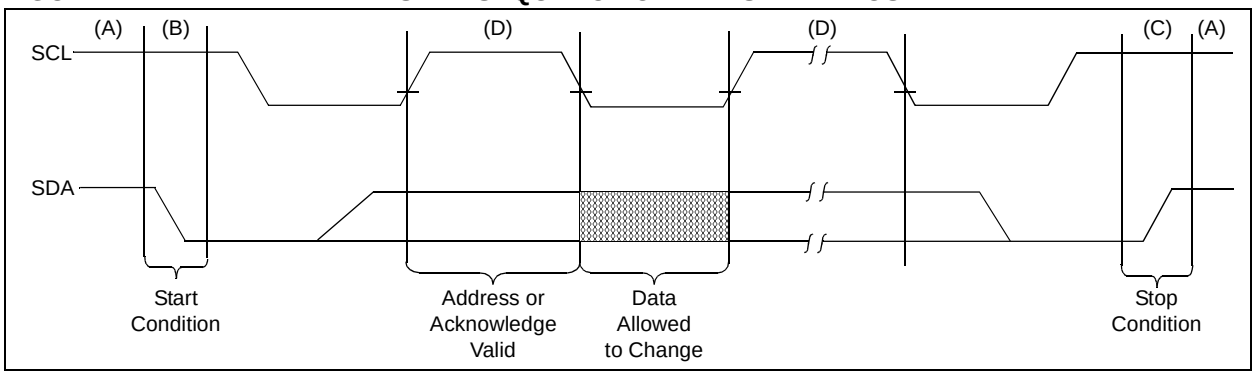
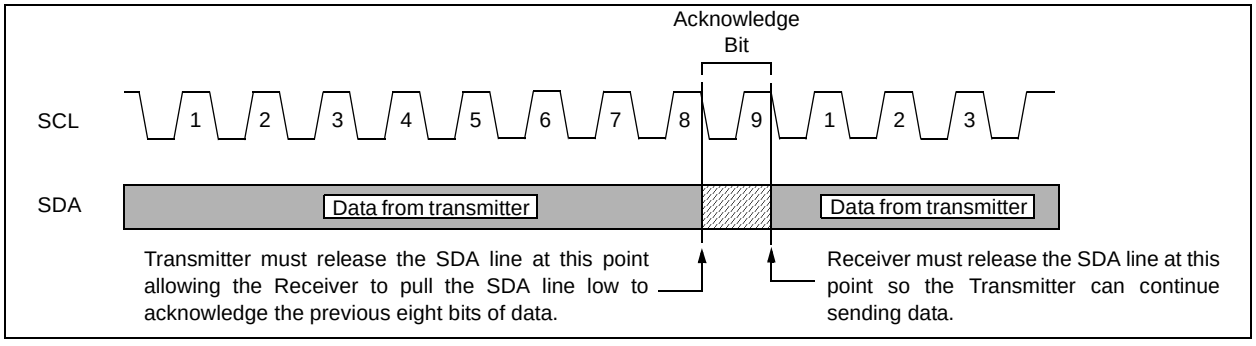


FIGURE 4-2: ACKNOWLEDGE TIMING



5.0 DEVICE ADDRESSING

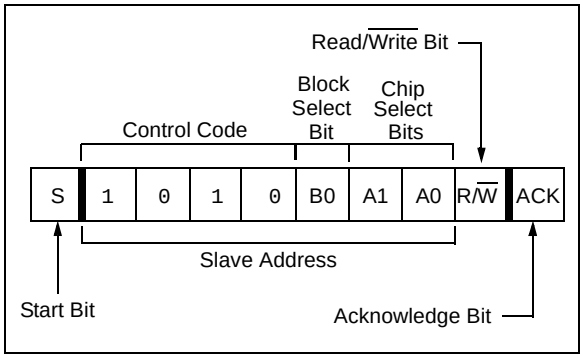
A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a 4-bit control code; for the 24XX515, this is set as '1010' binary for read and write operations. The next bit of the control byte is the block select bit (B0). This bit acts as the A15 address bit for accessing the entire array. The next two bits of the control byte are the Chip Select bits (A1, A0). The Chip Select bits allow the use of up to four 24XX515 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A1 and A0 pins for the device to respond. These bits are in effect the two Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected, and when set to a '0', a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A14…A0 are used, the upper address bit is a "don't care." The upper address bits are transferred first, followed by the Less Significant bits.

Following the Start condition, the 24XX515 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a '1010' code and appropriate device select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX515 will select a read or write operation.

This device has an internal addressing boundary limitation that is divided into two segments of 256K bits. Block select bit 'B0' is used in place of address bit location 'A15' to control access to each segment.

FIGURE 5-1: CONTROL BYTE FORMAT



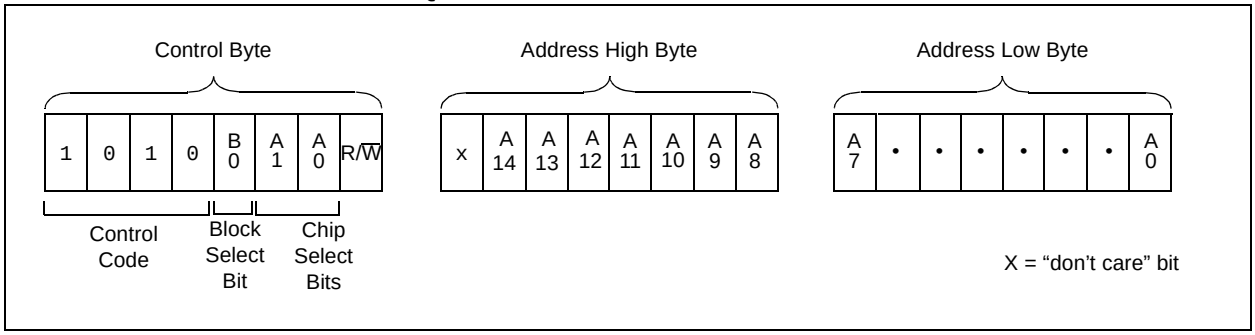
5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A1, A0 can be used to expand the contiguous address space for up to 2 Mbit by adding up to four 24XX515's on the same bus. In this case, software can use A0 of the control byte as address bit A16 and A1 as address bit A17. It is not possible to sequentially read across device boundaries.

Each device has internal addressing boundary limitations. This divides each part into two segments of 256K bits. The block select bit 'B0' controls access to each "half" rather than address bit location A15.

Sequential read operations are limited to 256K blocks. To read through four devices on the same bus, eight random Read commands must be given.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the master, the control code (four bits), the block select (one bit) the Chip Select (two bits), and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the high-order byte of the word address and will be written into the Address Pointer of the 24XX515. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX515, the master device will transmit the data word to be written into the addressed memory location. The 24XX515 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and during this time, the 24XX515 will not generate Acknowledge signals as long as the control byte being polled matches the control byte that was used to initiate the write (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

6.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24XX515 in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to 63 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a Stop condition. After receipt of each word, the six lower Address Pointer bits are internally incremented by one. If the master should transmit more than 64 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (0000-FFFF) when the pin is tied to VCC. If tied to VSS the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 1-1) Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 6-1: BYTE WRITE

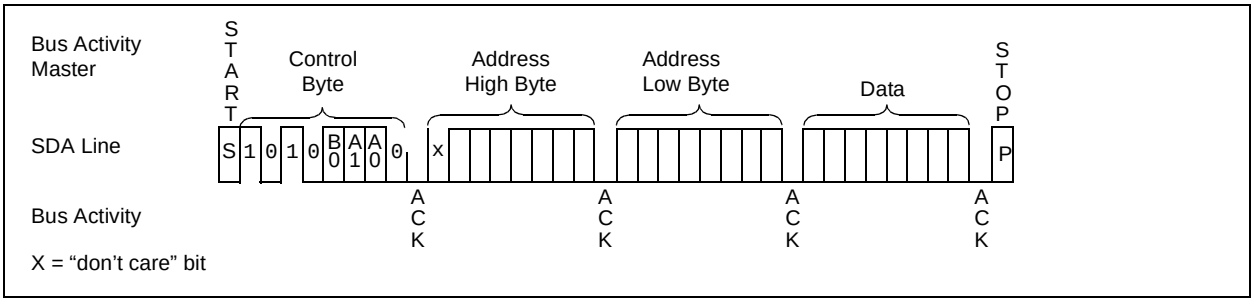
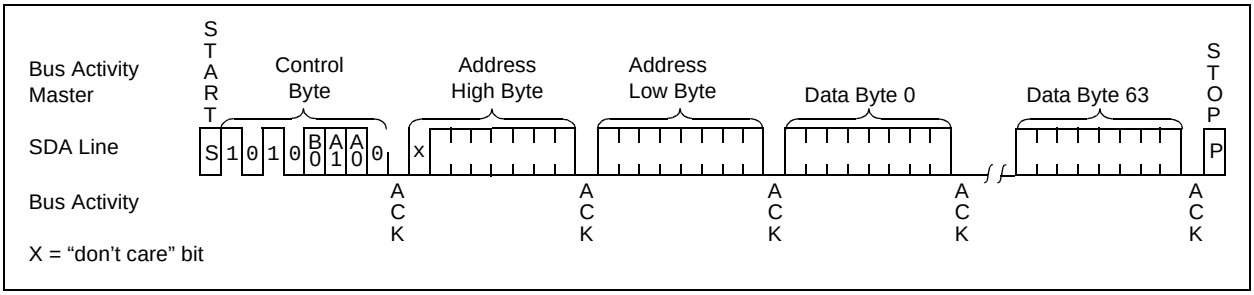


FIGURE 6-2: PAGE WRITE

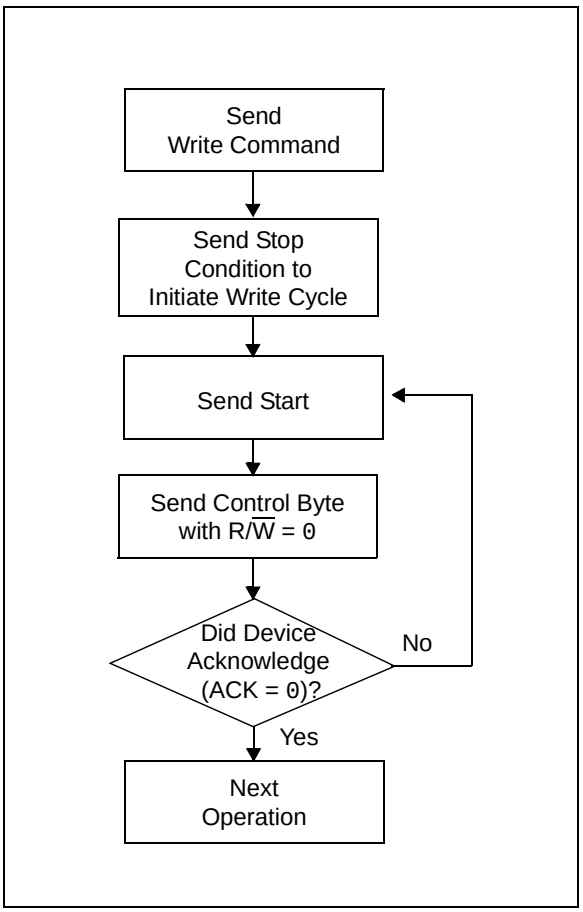


7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete. (This feature can be used to maximize bus throughput.) Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

Note:	Care must be taken when polling the 24LC515. The control byte that was used to initiate the write needs to match the control byte used for polling.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

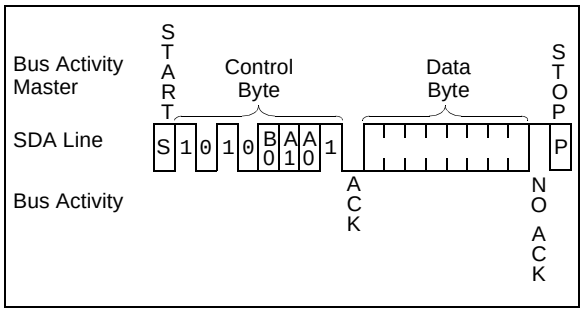
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX515 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the 24XX515 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XX515 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24XX515 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The 24XX515 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition which causes the 24XX515 to discontinue transmission (Figure 8-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX515 transmits the first data byte, the master issues an acknowledge as opposed to the Stop condition used in a random read. This acknowledge directs the 24XX515 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the master, the master will NOT generate an acknowledge, but will generate a Stop condition. To provide sequential reads, the 24XX515 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows half the memory contents to be serially read during one operation. Sequential read address boundaries are 0000h to 7FFFh and 8000h to FFFFh. The internal Address Pointer will automatically roll over from address 7FFF to address 0000 if the master acknowledges the byte received from the array address 7FFF. The internal address counter will automatically roll over from address FFFFh to address 8000h if the master acknowledges the byte received from the array address FFFFh.

FIGURE 8-2: RANDOM READ

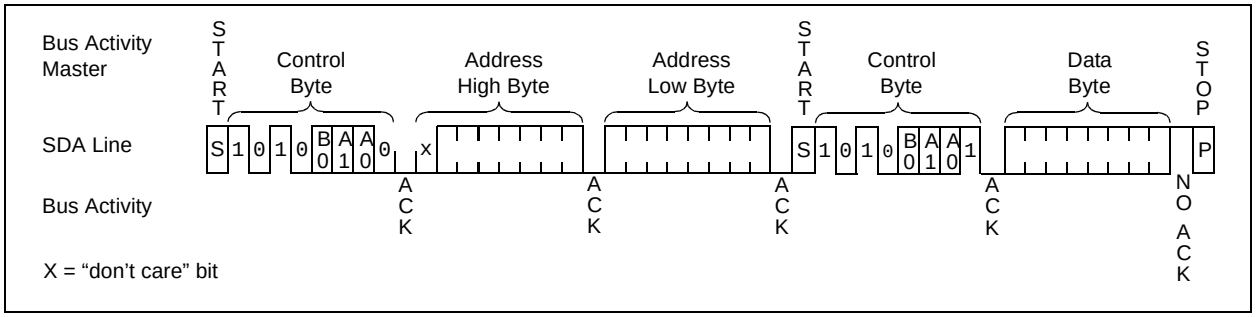
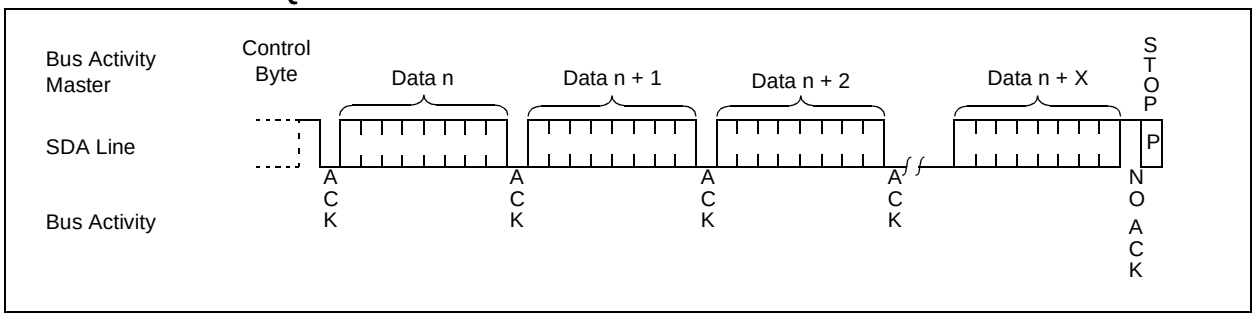


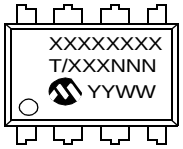
FIGURE 8-3: SEQUENTIAL READ



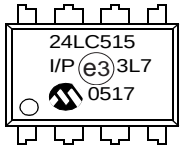
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

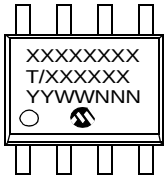
8-Lead PDIP (300 mil)



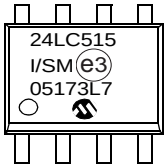
Example:



8-Lead SOIJ (5.28 mm)



Example:



Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)

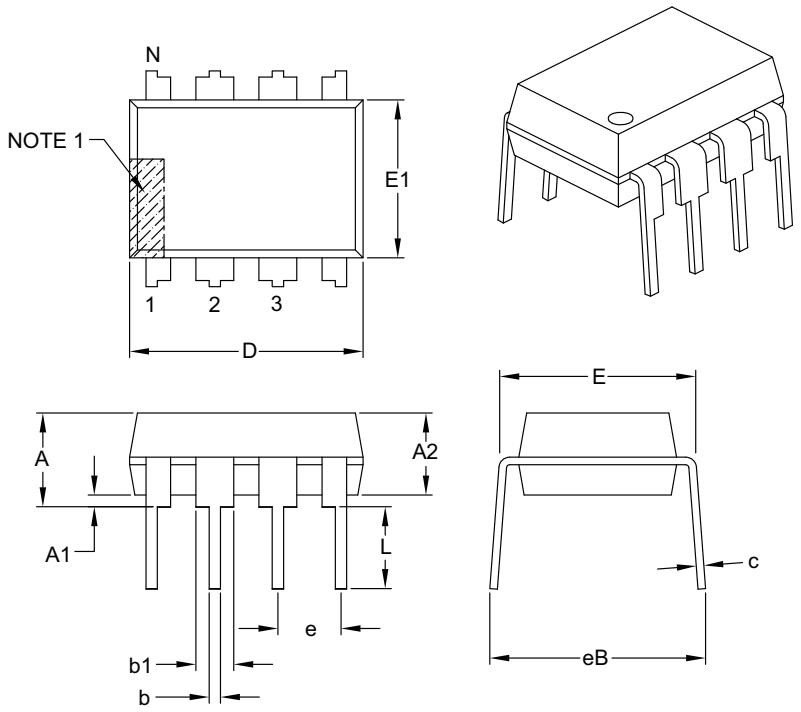
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

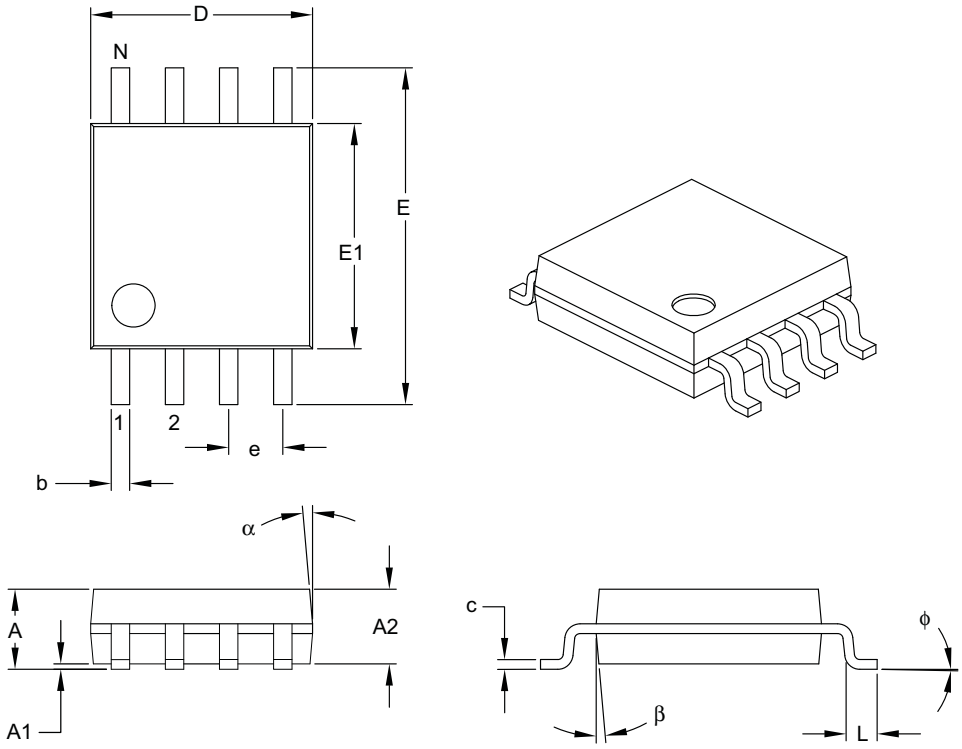
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SM) – Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	–	2.03
Molded Package Thickness	A2	1.75	–	1.98
Standoff §	A1	0.05	–	0.25
Overall Width	E	7.62	–	8.26
Molded Package Width	E1	5.11	–	5.38
Overall Length	D	5.13	–	5.33
Foot Length	L	0.51	–	0.76
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.15	–	0.25
Lead Width	b	0.36	–	0.51
Mold Draft Angle Top	α	–	–	15°
Mold Draft Angle Bottom	β	–	–	15°

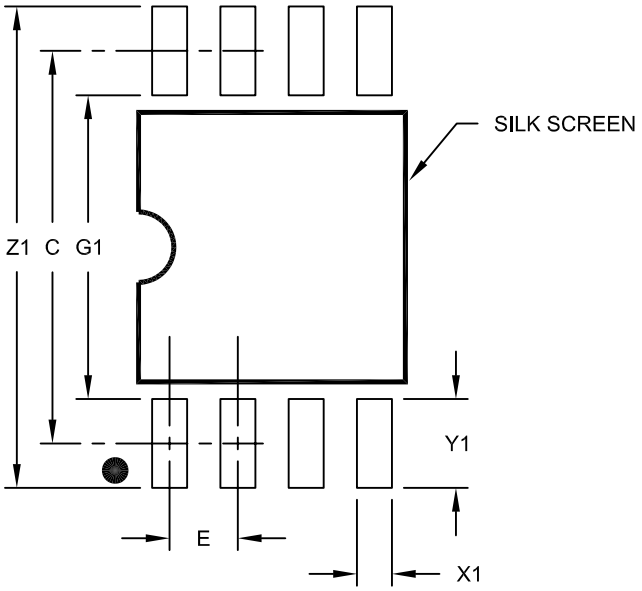
Notes:

1. SOIJ, JEITA/EIAJ Standard, formerly called SOIC.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

Microchip Technology Drawing C04-056B

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Overall Width	Z1			9.00
Contact Pad Spacing	C1		7.30	
Contact Pad Width (X28)	X1			0.65
Contact Pad Length (X28)	Y1			1.70
Distance Between Pads	G1	5.60		
Distance Between Pads	G	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056B

APPENDIX A: REVISION HISTORY

Revision C

Corrections to Section 1.0, Electrical Characteristics.

Revision D

Removed Preliminary status.
Revised conditions, Table 1-2, Param. 18.

Revision E

Revised Tables 1-1 and 2-1. Add Pb-free marking.

Revision F

Section 1.0 Electrical Characteristics: revised Ambient Temperature; Revised Section 2.1 and Section 2.5

Revision G (07/2008)

Revised Features section; Revised 1.8V voltage to 1.7V; Replaced Package Drawings; Revised Product ID System.

NOTES:

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5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	24AA515:	=	512K Bit 1.8V I^2C CMOS Serial EEPROM
	24AA515T:	=	512K Bit 1.8V I^2C CMOS Serial EEPROM (Tape and Reel)
	24LC515:	=	512K Bit 2.5V I^2C CMOS Serial EEPROM
	24LC515T:	=	512K Bit 2.5V I^2C CMOS Serial EEPROM (Tape and Reel)
	24FC515:	=	512K Bit 2.5V I^2C CMOS Serial EEPROM
	24FC515T:	=	512K Bit 2.5V I^2C CMOS Serial EEPROM (Tape and Reel)
Temperature Range:	I	=	-40°C to+85°C
Package:	P	=	Plastic DIP (300 mil Body), 8-lead
	SM	=	Plastic SOIJ (5.28 mm Body), 8-lead

Examples:

a) 24AA515T-I/SM: Tape and Reel, Industrial Temperature, SOIJ package.

b) 24LC515-I/P: Industrial Temperature, PDIP package.

c) 24LC515-I/SM: Industrial Temperature, SOIJ package.

d) 24LC515T-I/SM: Tape and Reel, Industrial Temperature, SOIJ package.

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