PI4IOE5V9570

4-bit general purpose outputs for 1MHz I²C bus

Features

- Operation power supply voltage from 2.3V to 5.5V
- 4-bit I²C-bus GPO
- 1 MHz I²C-bus interface with 30 mA SDA sink capability for 4000pF
- Latched outputs with 25mA capability for directly driving LEDs
- Software Reset; Power-on reset
- Low standby current
- ESD protection (4KV HBM and 1KV CDM)
- Offered in two different packages:UQFN 1.6x1.6-8,MSOP-8

Description

The PI4IOE5V9570 is a CMOS device that provides 4bits of General Purpose parallel Output (GPO) expansion in low voltage processor and handheld battery powered mobile applications. It operates at 1 MHz I²C-bus speeds while maintaining backward compatibility to Fast-mode (400 kHz) and Standard-mode (100 kHz).

The PI4IOE5V9570 is a streamlined GPO that consists of 4-bit push-pull outputs that offer low current consumption, small packaging options The PI4IOE5V9570 output expander provides a simple solution when additional outputs are needed while keeping interconnections and floor space to a minimum, for example, in battery powered mobile applications where PCBs are crowded for interfacing to sensors, push buttons, etc.

The PI4IOE5V9570 contains an internal Power-On Reset (POR) and a Software Reset feature that initializes the device to its default state.

Pin Configuration

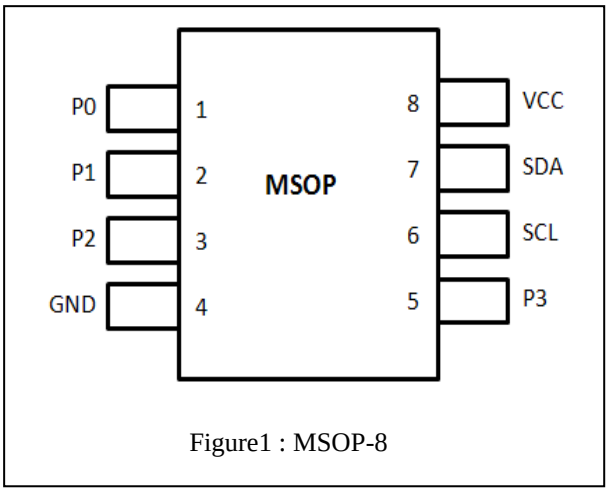


Figure1 : MSOP-8

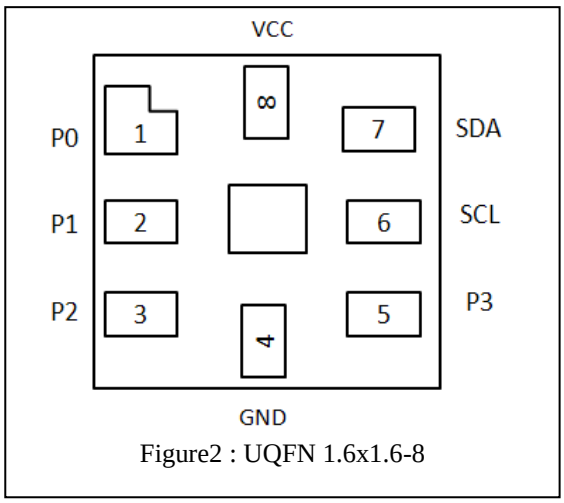


Figure2 : UQFN 1.6x1.6-8

Pin Description

Table 1. Pin configuration
* I = Input; O = Output; P = Power; G = Ground

TDFN 1.6*1.6	TSSOP	Name	Type	Description
1	1	P0	I/O	Input/ output 0
2	2	P1	I/O	Input/ output 1
3	3	P2	I/O	Input/ output 2
4	4	GND	G	Supply Ground
5	5	P3	I/O	Input/ output 3
6	6	SCL	I	Serial clock line
7	7	SDA	I/O	Serial data line
8	8	VCC	P	Power supply

Maximum Ratings

Power supply.....-0.5V to +6.0V
Voltage on an I/O pin.....GND-0.5V to +6.0V
Input current.....±20mA
Output current on an I/O pin.....±50mA
Supply current.....85mA
Ground supply current.....100mA
Total power dissipation.....200mW
Operation temperature.....-40~85℃
Storage temperature.....-65~150℃
Maximum Junction temperature ,T j(max).....125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC =2.3 V to 5.5V; GND = 0 V; Tamb= -40 ℃ to +85 ℃; unless otherwise specified.

Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3	-	5.5	V
I_{DD}	Supply current	Operating mode; no load; VI = VCC or GND; fSCL = 1 MHz;	-	200	500	μA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; V_I = VCC; f_{SCL}= 0 kHz; I/O = inputs	-	4.5	10	uA
V_{POR}	Power-on reset voltage[1]	Standby mode; no load; VI = VCC or GND; fSCL = 0 kHz	-	1.16	1.41	V
Input SCL, input/output SDA						
V_{IL}	Low level input voltage		-0.5		$0.3V_{CC}$	V
V_{IH}	High level input voltage		$0.7V_{CC}$		5.5	V
I_{OL}	Low level output current	V_{OL} = 0.4 V; V_{CC} = 2.3 V	20	35	-	mA
		V_{OL} = 0.4 V; V_{CC} = 3.0 V	25	44		
		V_{OL} = 0.4 V; V_{CC} = 4.5 V	30	57		
I_L	Leakage current	V_I=VCC=GND	-1	-	1	μA
C_i	Input capacitance	V_I =GND	-	5	10	pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
VIL	LOW-level input voltage		-0.5		0.81	V
VIH	HIGH-level input voltage		1.8		5.5	V
I_{OL}	Low level output current	VCC = 2.3 V; V_{OL} = 0.5 V[2]	12	26		mA
		VCC =3.0V; V_{OL} = 0.5 V[2]	17	33		mA
		VCC =4.5V; V_{OL} = 0.5 V[2]	25	40		mA
I_{OL}(tot)	total LOW-level output current	VOL=0.5V;VCC=4.5V			200	mA
I_{OH}	HIGH-level output current	VOH = GND	-30	-359	-480	uA
Itrt(pu)	transient boosted pull-up current	VOH= GND	-0.5	-1.0		mA
C_i	Input capacitance		-	2.1	10	pF
C_o	Output capacitance		-	2.1	10	pF

Note:
[1]: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.
[2]: Each I/O must be externally limited to a maximum of 25 mA and the total package limited to 100 mA due to internal busing limits.
[3]: The value is not tested, but verified on sampling basis.

Dymaic Characteristics

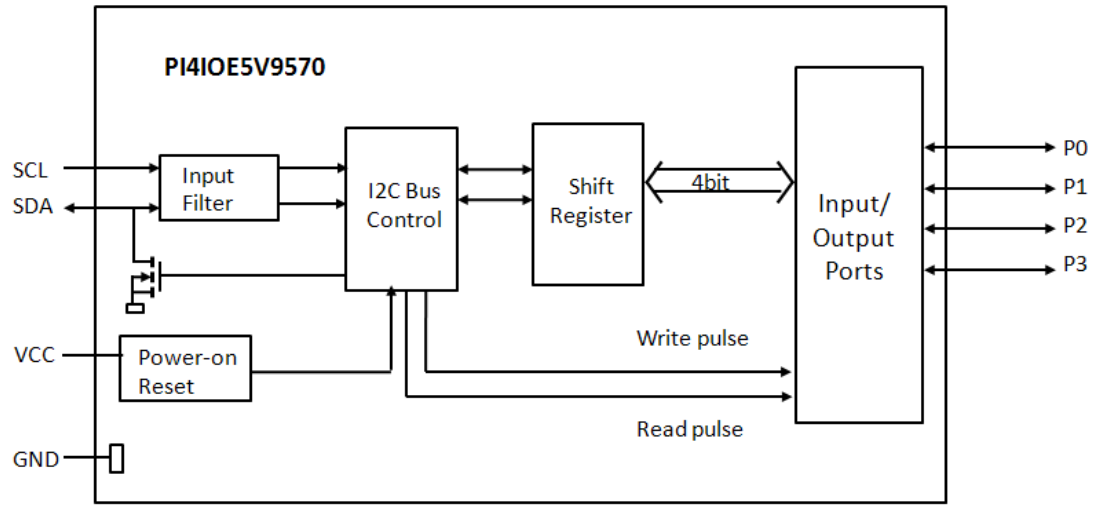
Table 3: Dynamic characteristics

Symbol	Parameter	Test Conditions	Standard mode I^2C		Fast mode I^2C		1 MHz I2C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5		µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26		µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26		µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26		µs
$t_{VD;ACK}$[1]	data valid acknowledge time		-	3.45	-	0.9		0.45	µs
$t_{HD;DAT}$	data hold time		0			0			ns
$t_{VD;DAT}$[2]	data valid time			3.45	-	0.9		0.45	us
$t_{SU;DAT}$	data set-up time		250	-	100	-	50		ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5		µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26		µs
t_f	fall time of both SDA and SCL signals		-	300	-	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	-	300	-	120	ns
t_{SP}[3]	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	-	50	ns
Port timing									
$t_{v(Q)}$	Data output valid time			200		200		200	ns

Note:
[1] tVD;ACK = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
[2] tVD;DAT = minimum time for SDA data out to be valid following SCL LOW.
[3] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

PI4IOE5V9570 Block Diagram

Fig 3: Block diagram of PI4IOE5V9570



Details Description

a. Device Address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	0	1	0	0	1	0	0	R/W

b. Software Reset Call

General Call address: allows resetting the device through the I²C-bus upon reception of the right I²C-bus sequence.

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
General Call Address	0	0	0	0	0	0	0	0

c. Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I²C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.

a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

b. If more than 1 byte of data is sent, the device does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 4.

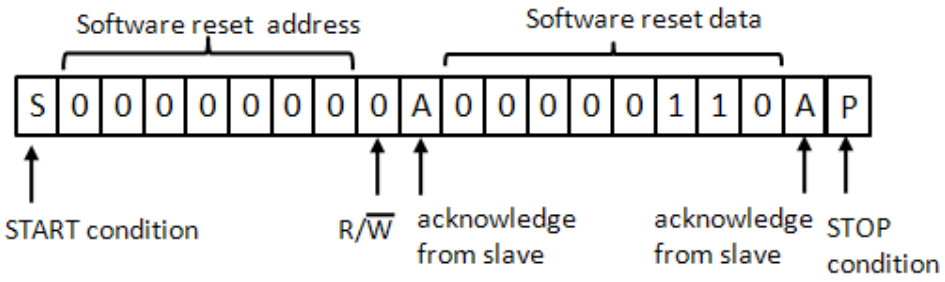


Figure 4: Software reset

d. Quasi-bidirectional I/O architecture

The device ports are entirely independent and are output ports. The state of the ports at the pin is transferred from the ports to the microcontroller in the Read mode (see Figure 7). Output data is transmitted to the ports in the Write mode (see Figure 6).At power-on all ports are HIGH. The state of the Output Port register determines if either Q1 or Q2 is on, driving the line either HIGH or LOW. A bit set to 1 in the data byte drives the line HIGH at the corresponding port. A bit set to 0 in the data byte drives the line LOW at the corresponding port.

If an external voltage is applied to an output, care should be exercised because of the low-impedance path that exists between the pin and either VCC or GND.

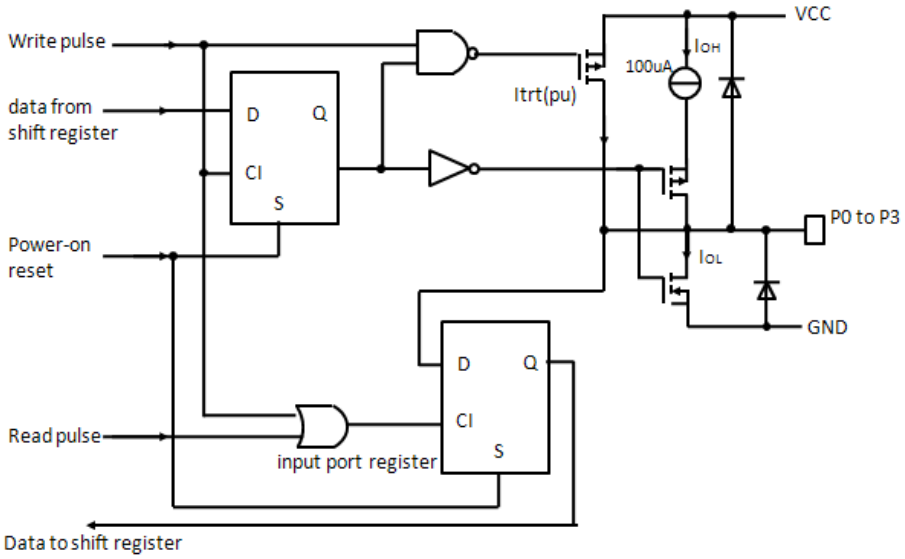


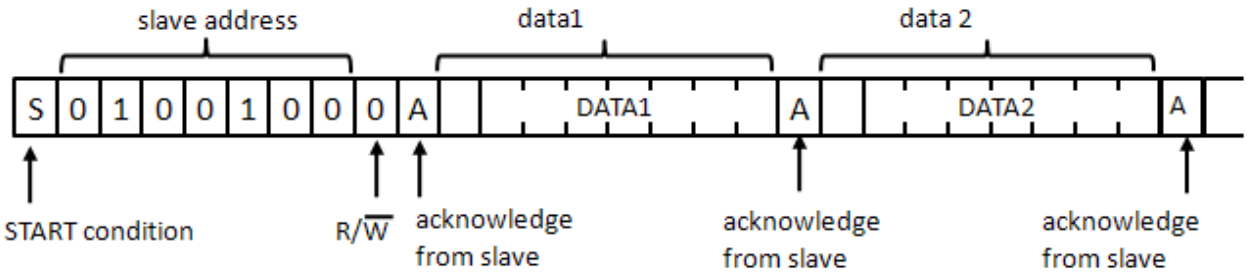
Figure 5:I/O architecture

e. Bus Transaction

Writing to the port (output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0, the Write mode is entered. The device acknowledges and the master sends the data byte for P7 to P0 and is acknowledged by the device. Writes to P7 to P4 are ignored in the PI4IOE5V9570 as only P3 through P0 are available. The 4-bit data is presented on the port lines after it has been acknowledged by the device. The number of data bytes that can be sent successively is not limited. The previous data is overwritten every time a data byte has been sent.

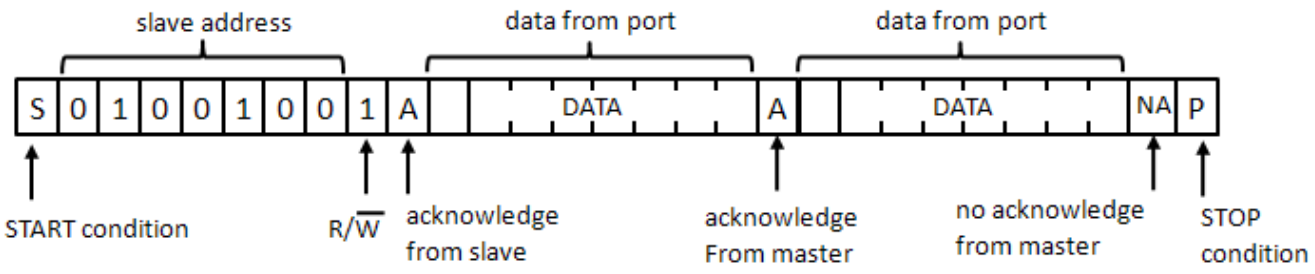
Figure 6: Write to configuration registers



Reading from a port (input mode)

All ports are outputs and cannot be used as inputs. When reading the device, the data returned is the port state at the pin. To read, the master (microcontroller) first addresses the slave device by setting the last bit of the byte containing the slave address to logic 1. The data byte that follows on the SDA is the value of the ports pins. There is no limit to the number of bytes read, and the state of the output port pins is updated at each acknowledge cycle. Logic 1 means that the port is HIGH. Logic 0 means that the port is LOW. When the PI4IOE5V9570 is read, P7 through P4 return logic '1'.

Figure 7: Read from registers



Note: Transfer can be stopped at any time by a STOP condition.

f. Power-on reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the device in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the device registers and I²C-bus/SMBus state machine initialize to their default states.

I/O expander applications

Bellow figure shows a 4-bit output expander application. The desired HIGH or LOW logic levels are controlled by the master with speeds of up to 1 MHz .This allows the host processor to control various functions quickly and with very low overhead. The port read function of the device enables the host processor to poll the status of the output port pins. This is useful for system recovery operations or debugging.

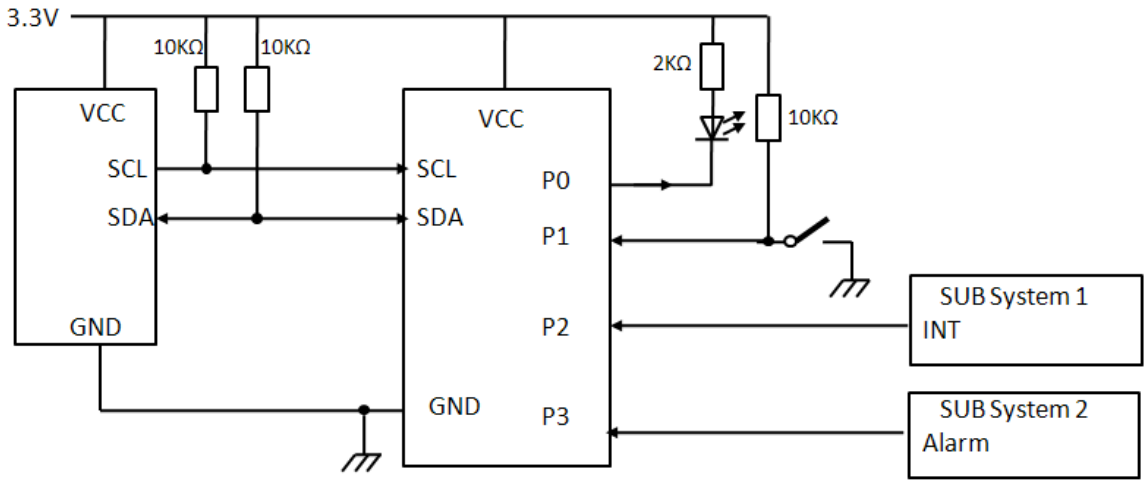
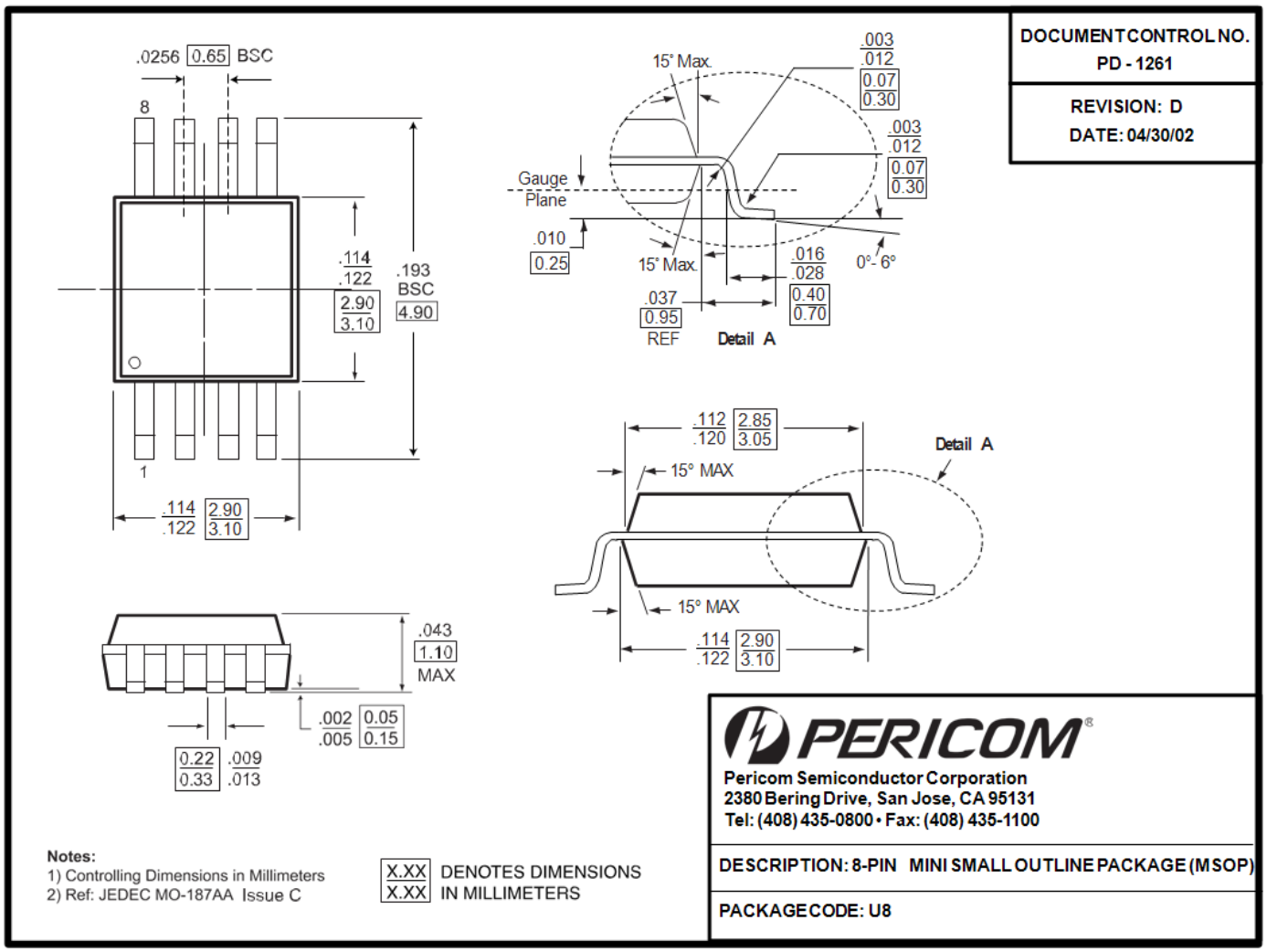


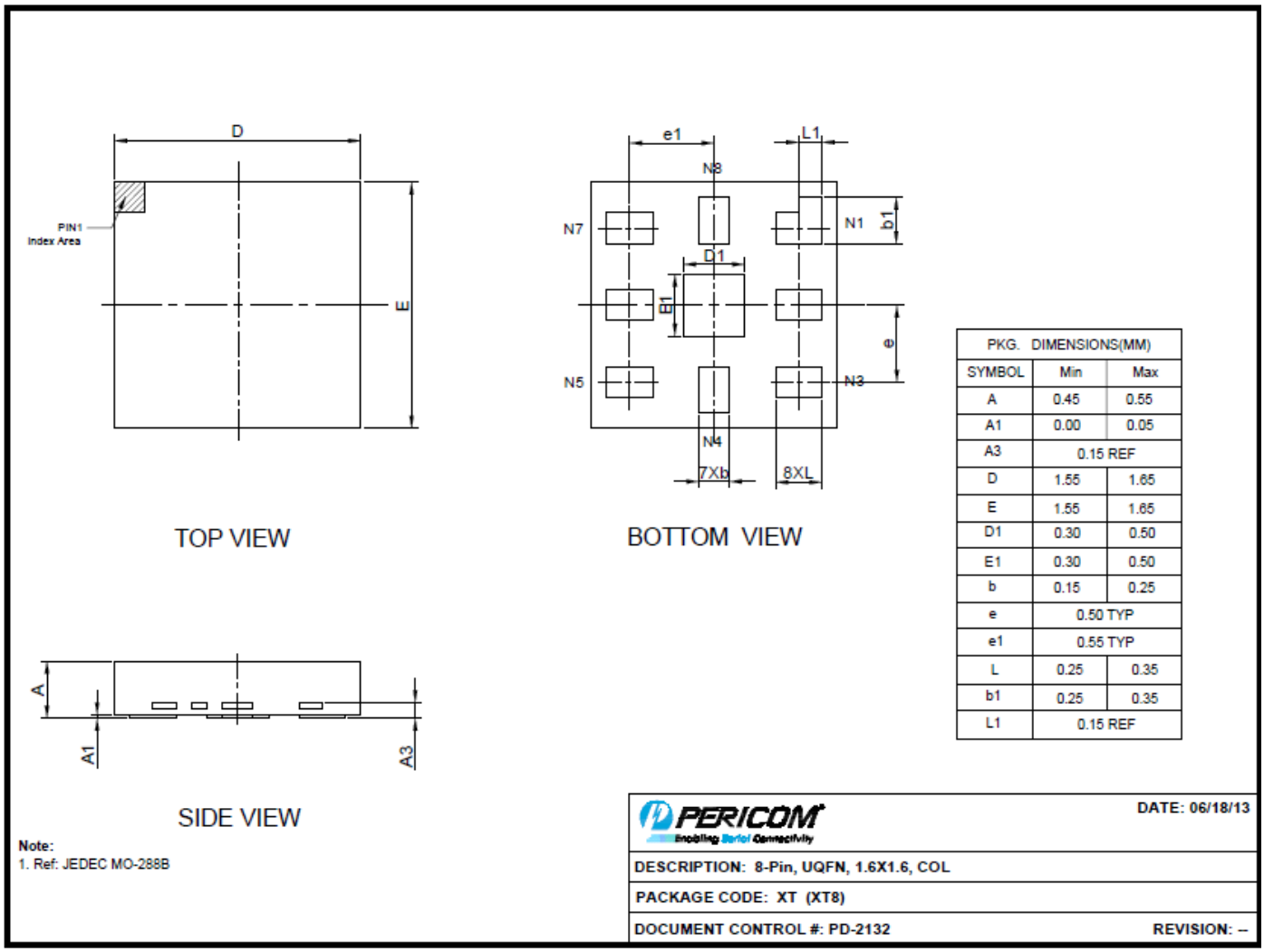
Figure 8: Application

Mechanical Information

MSOP-8(U)



UQFN-8(XT)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF	
D	1.55	1.65
E	1.55	1.65
D1	0.30	0.50
E1	0.30	0.50
b	0.15	0.25
e	0.50 TYP	
e1	0.55 TYP	
L	0.25	0.35
b1	0.25	0.35
L1	0.15 REF	

Ordering Information

Part No.	Package Code	Package
PI4IOEV9570UE	U	8-Pin, Mini Small Outline Package(MSOP)
PI4IOE5V9570UE	U	8-Pin, Mini Small Outline Package(MSOP), Tape & Reel
PI4IOE5V9570XTEX	XT	8-pin UQFN 1.6x1.6, Tape & Reel

Note:

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel