IGLOO2 Pin Descriptions

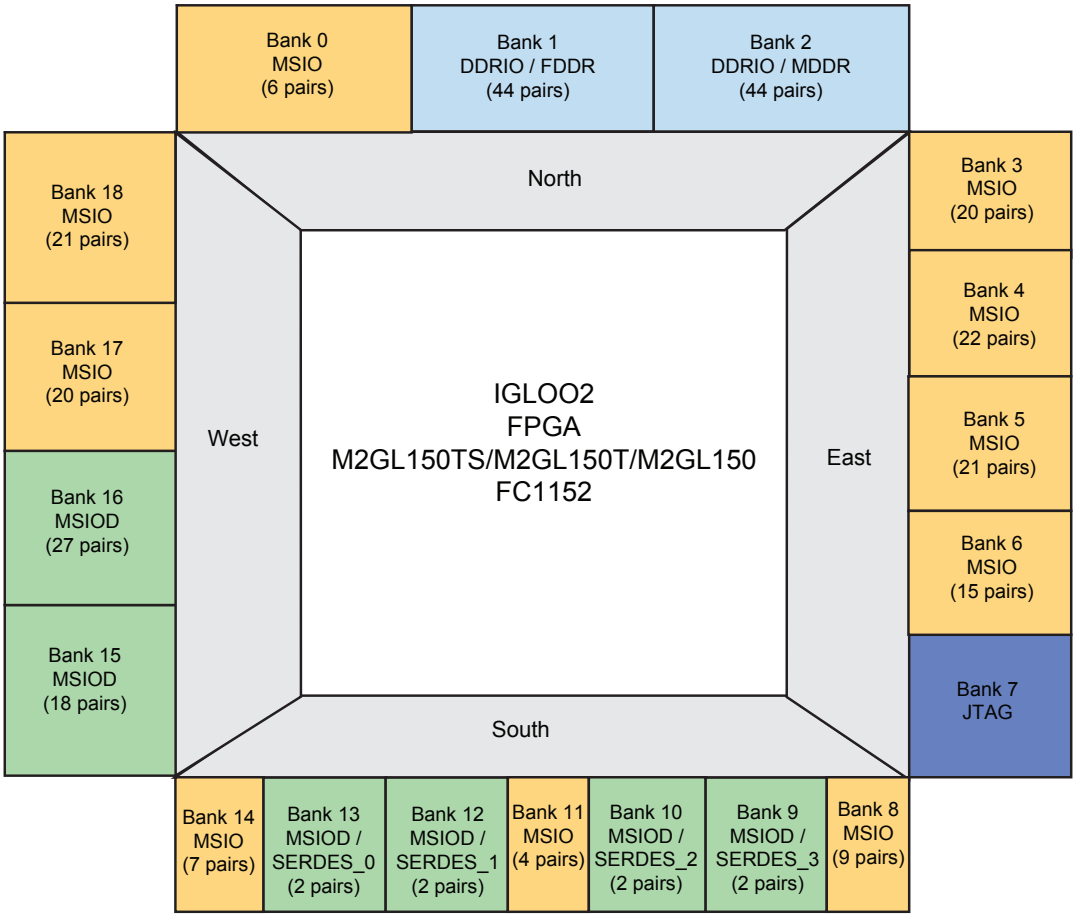
User I/Os

IGLOO®2 field programmable gate array (FPGA) devices feature a flexible I/O structure that supports a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The MSIO, MSIOD, and DDRIO can be configured as differential I/Os or two single-ended I/Os. These I/Os use one I/O slot to implement single-ended standards and two I/O slots for differential standards.

For functional block diagrams of MSIO, MSIOD, and DDRIO, refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.
For supported I/O standards, refer to the "Supported Voltage Standards" table in the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

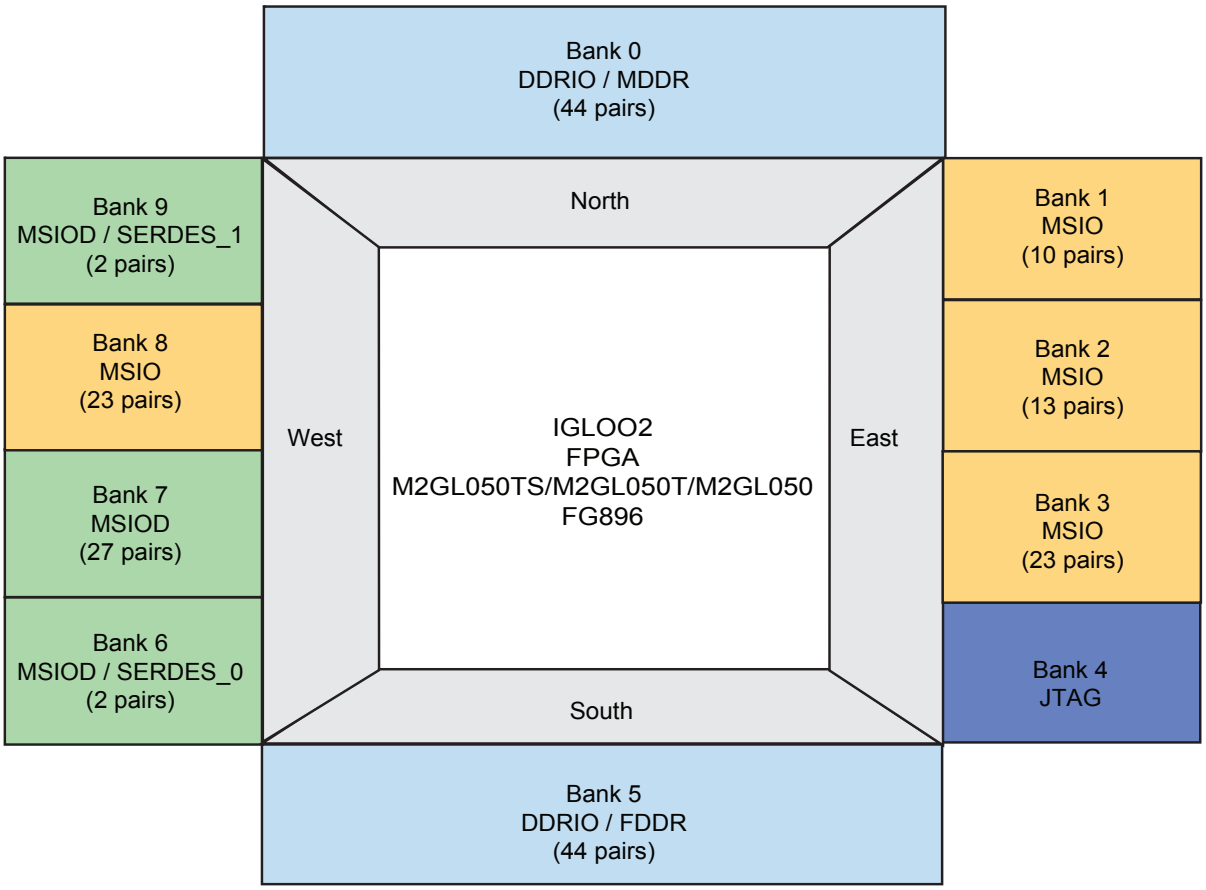
Bank Location Diagrams

I/Os are grouped on the basis of I/O voltage standard. The grouped I/Os of each voltage standard form an I/O bank. Each I/O bank has dedicated I/O supply and ground voltages. Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank.



Note: For M2GL150-FC1152 device, SERDES blocks are not available in bank 9, 10, 12, and 13.

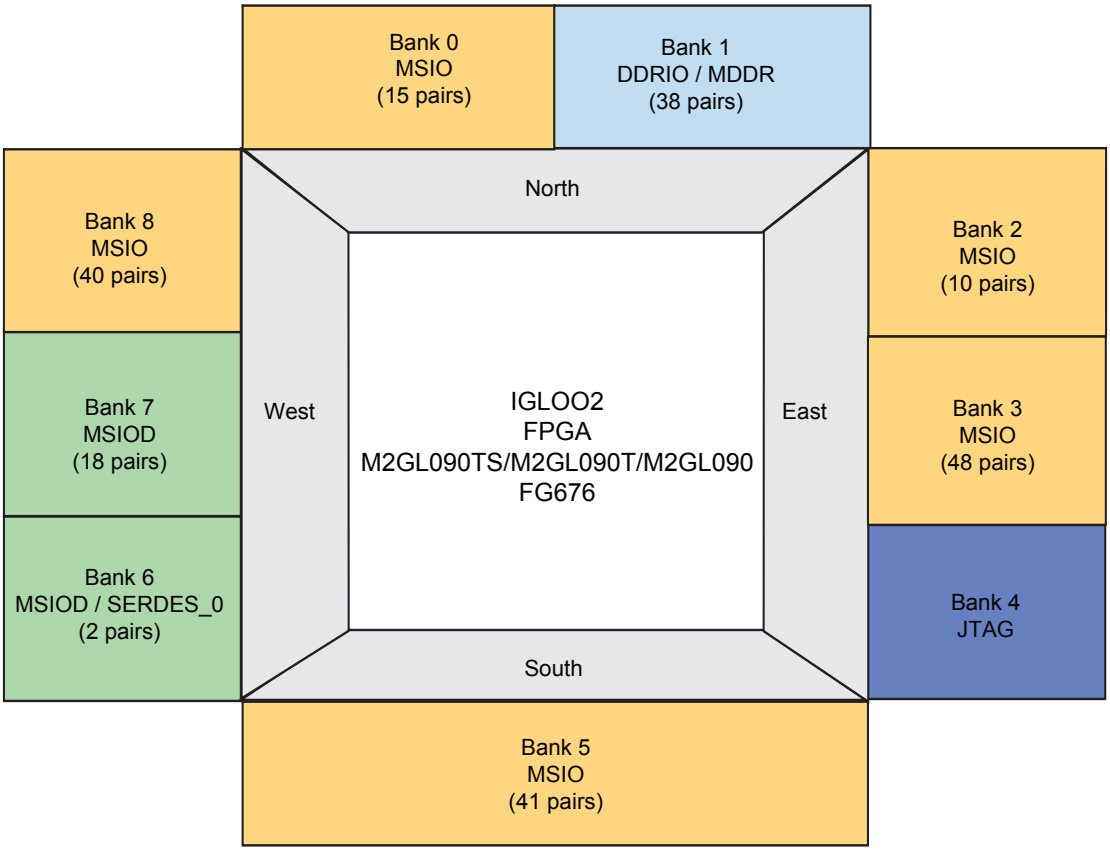
***Figure 1* • IGLOO2 M2GL150TS/M2GL150T/M2GL150-FC1152 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin H27, MSI46NB1, cannot be configured as differential. The function MSI46NB1 is an input only pin.*
2. *For M2GL050-FG896 device, SERDES blocks are not available in bank 6 and bank 9.*

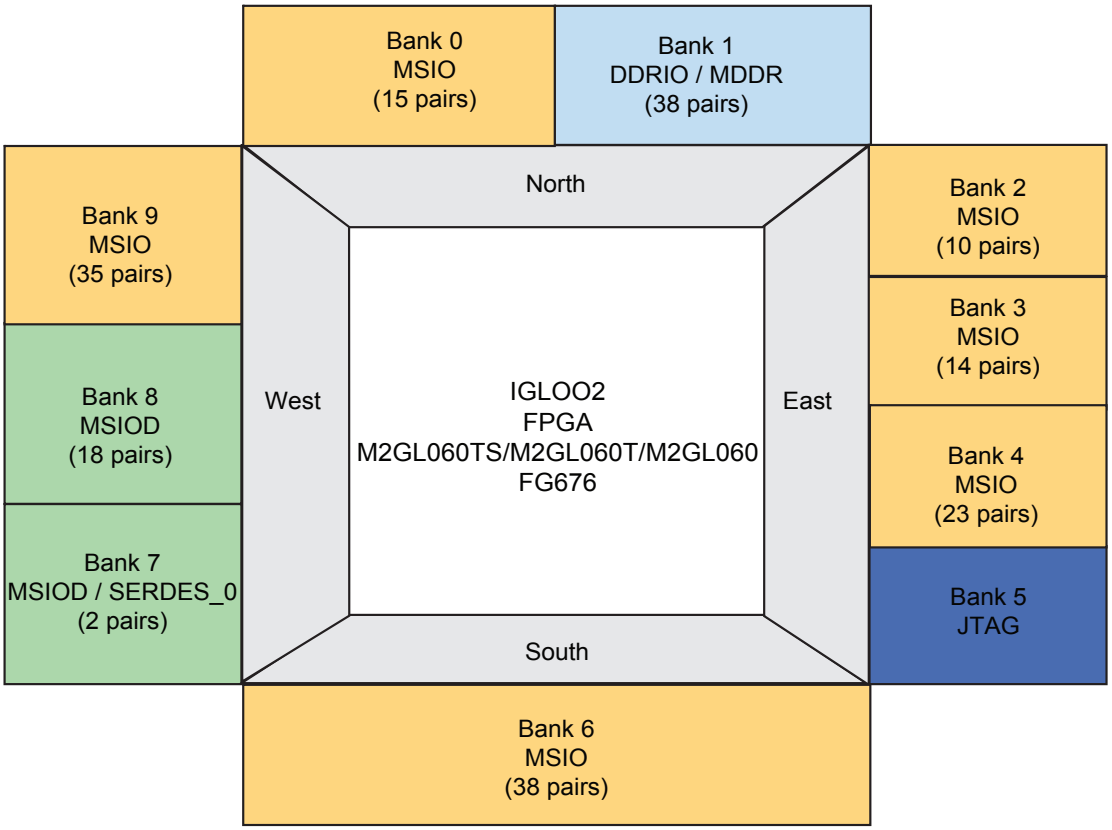
***Figure 2* • IGLOO2 M2GL050TS/M2GL050T/M2GL050-FG896 I/O Bank Locations**



Notes:

1. *In bank 2, there are 21 single-ended user I/Os. Pin D23 and MSI59NB2 cannot be configured as differential. The function MSI59NB2 is an input only pin.*
2. *For M2GL090-FG676 device, the SERDES block is not available in bank 6.*

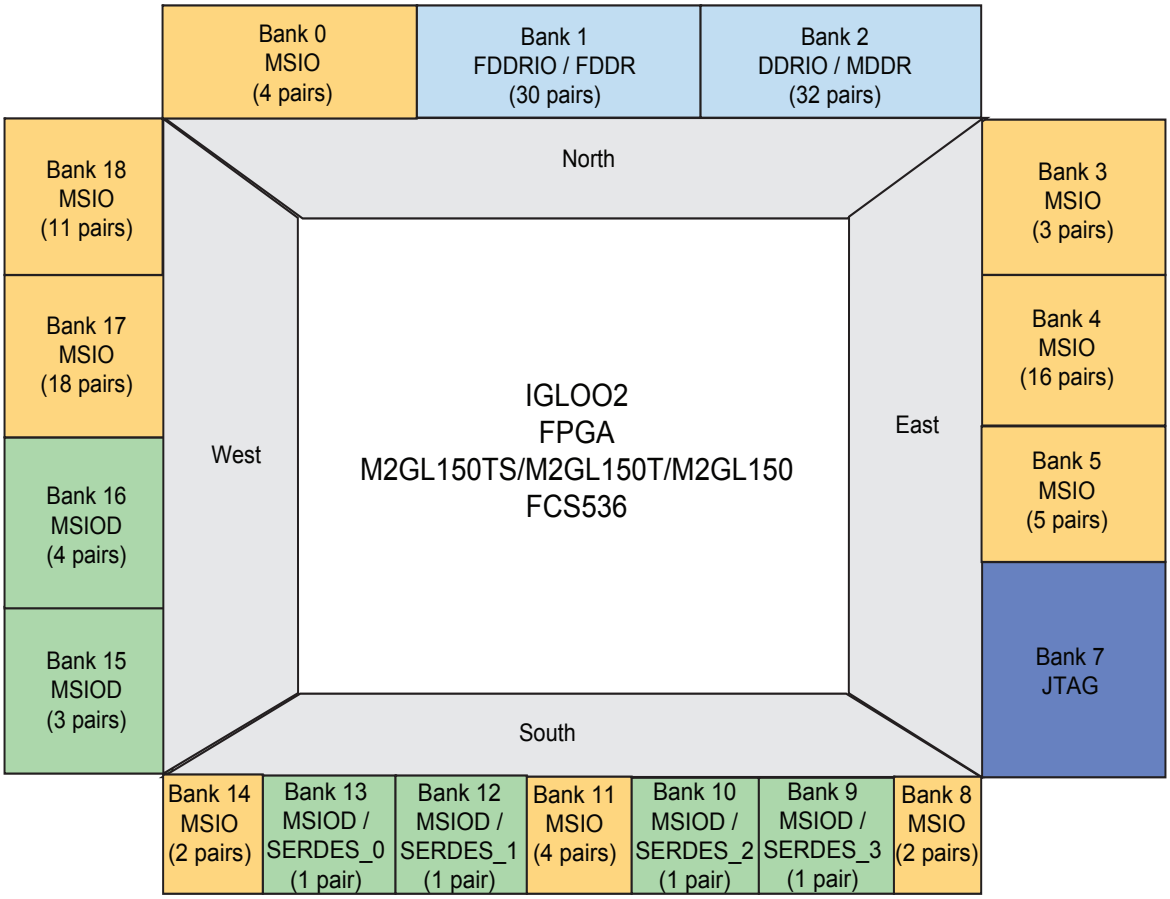
Figure 3 • **IGLOO2 M2GL090TS/M2GL090T/M2GL090-FG676 I/O Bank Locations**



Notes:

1. *For M2GL060-FG676 device, SERDES block is not available in bank 7.*

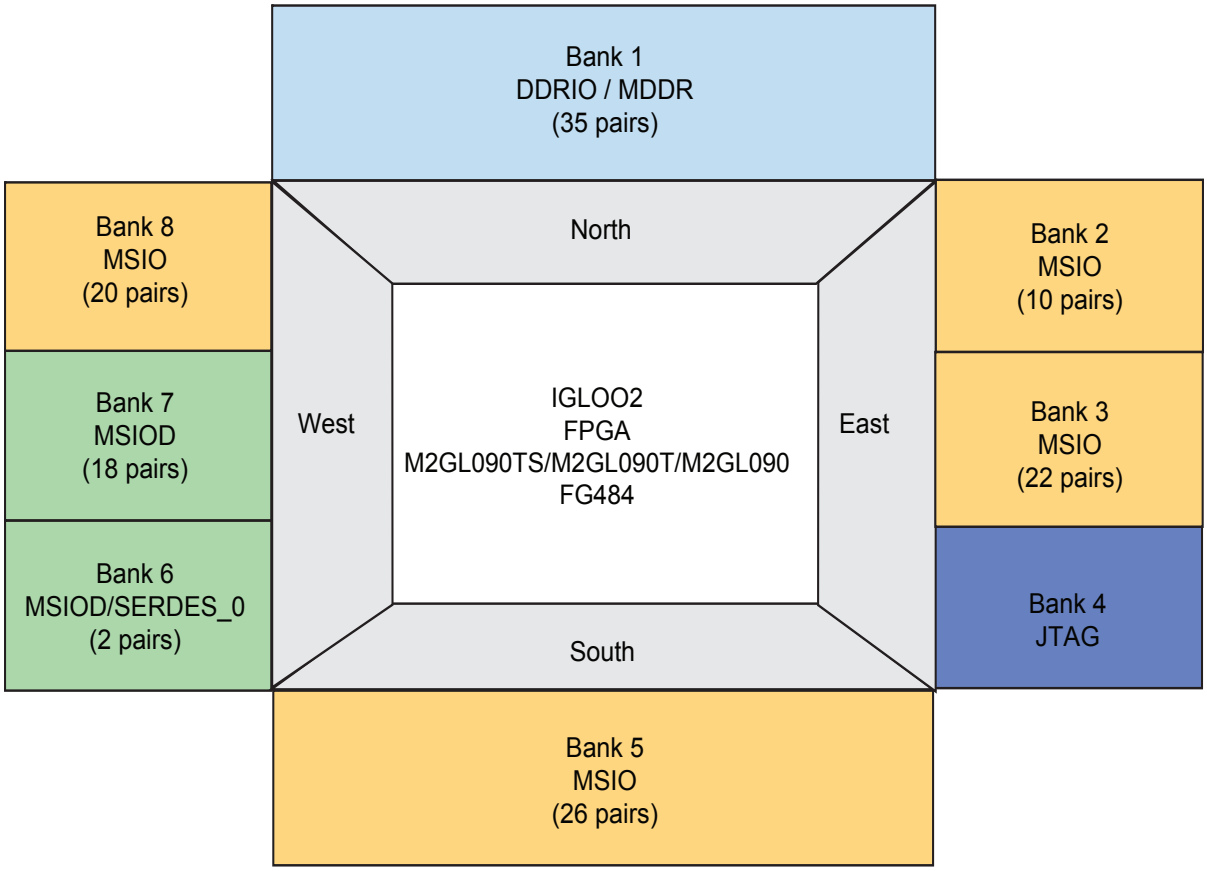
Figure 4 • **IGLOO2 M2GL060TS/ M2GL060T/M2GL060-FG676 I/O Bank Locations**



Notes:

1. *For M2GL150-FCS536 device, SERDES interface is not available in bank 9, 10,12, and 13.*

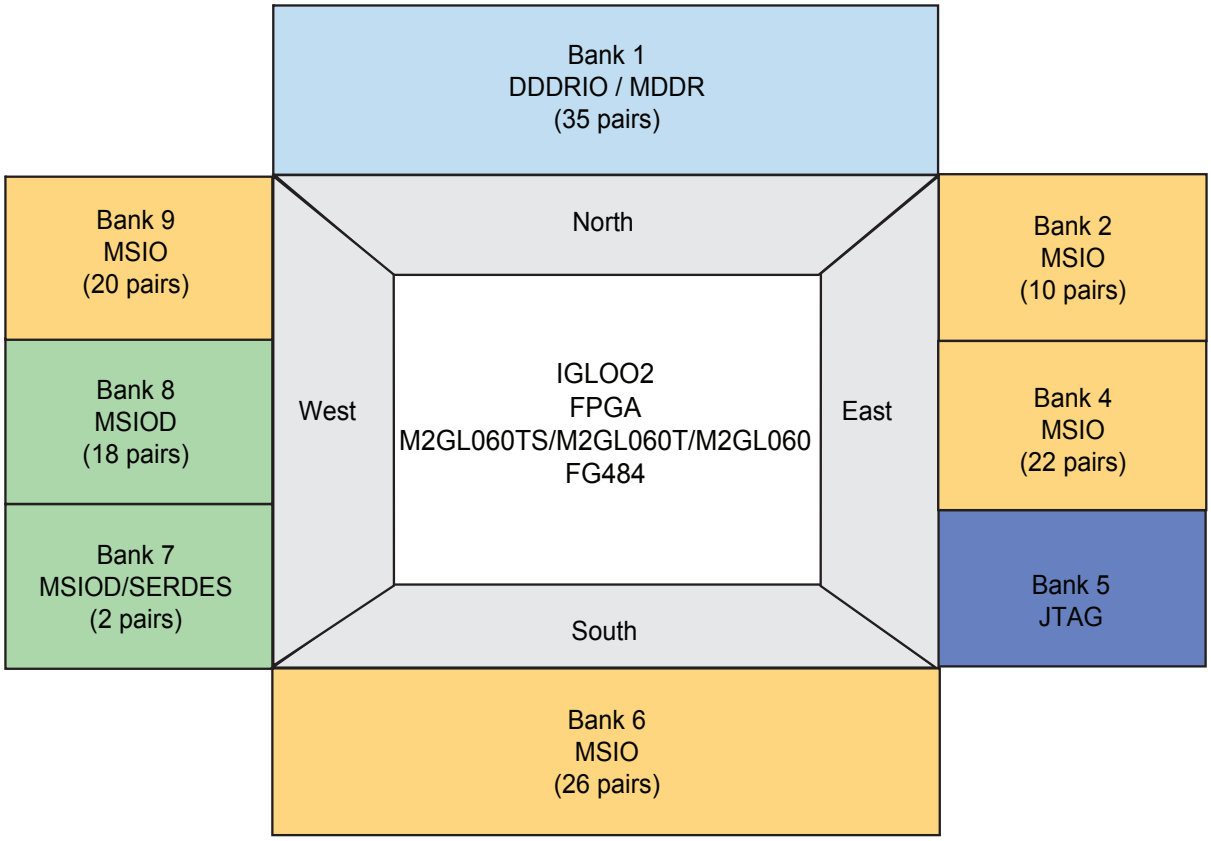
Figure 5 • **IGLOO2 M2GL150TS/M2GL150T/M2GL150-FCS536 I/O Bank Locations**



Notes:

1. *In bank 2, there are 21 single-ended user I/Os. Pin D21, MSI59NB2, cannot be configured as differential. The function MSI59NB2 is an input only pin.*
2. *For M2GL090-FG484 device, SERDES block is not available in bank 6.*

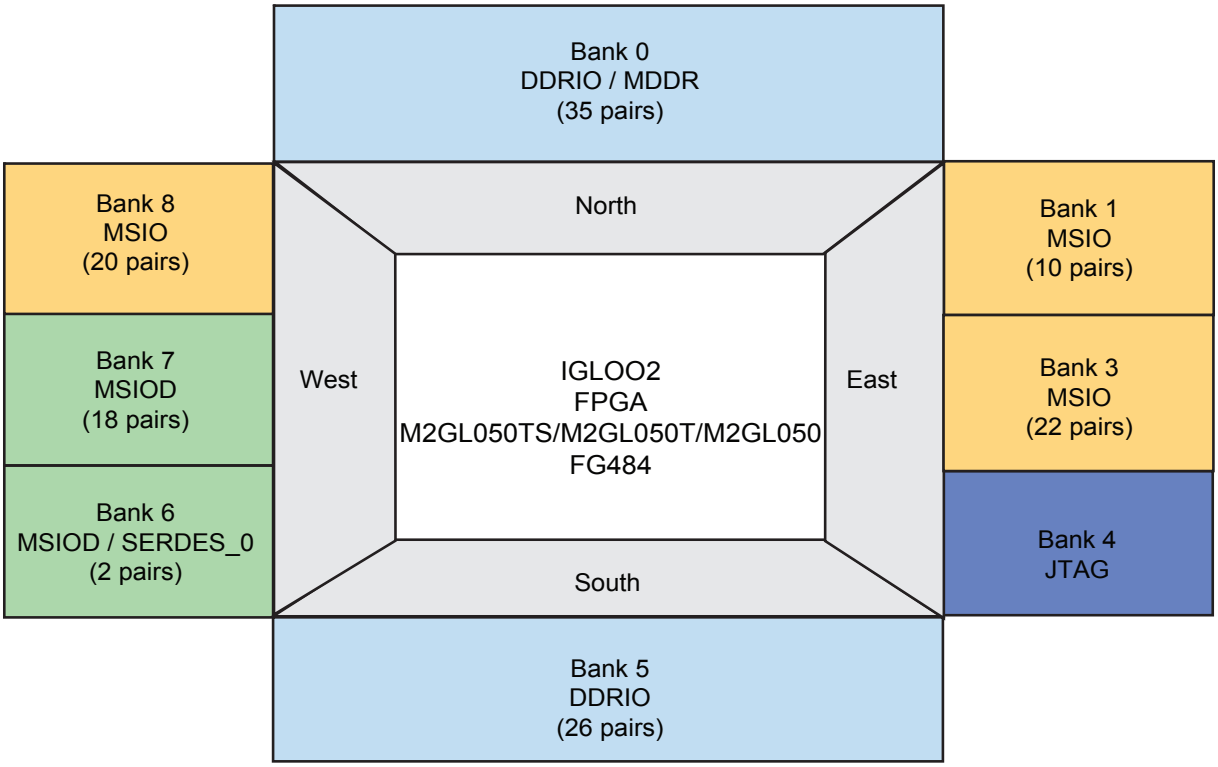
***Figure 6* • IGLOO2 M2GL090TS/M2GL090T/M2GL090-FG484 I/O Bank Locations**



Notes:

1. *In bank 2, there are 21 single-ended user I/Os. Pin D21, MSI47NB2, cannot be configured as differential. The function MSI47NB2 is an input only pin.*
2. *For the M2GL060S-FG484 and M2GL060-FG484 devices, SERDES block is not available in bank 7.*

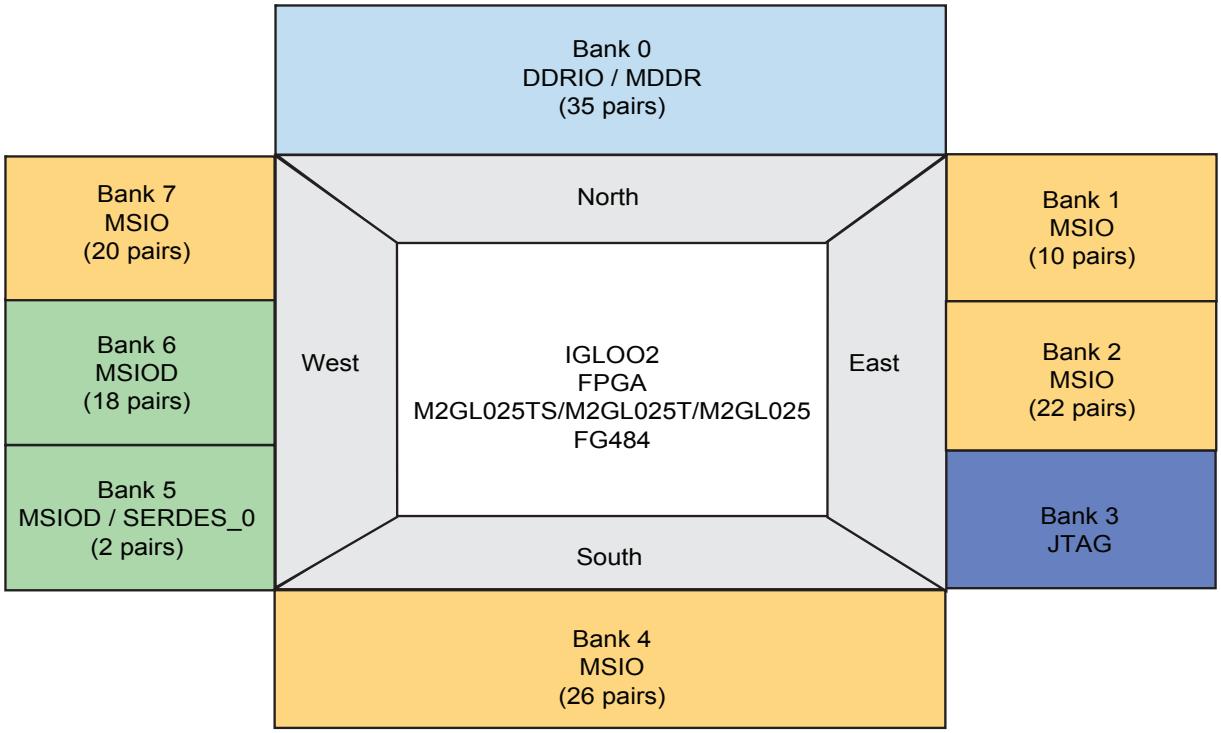
Figure 7 • **IGLOO2 M2GL060TS/M2GL060T/M2GL060-FG484 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D21, MSI46NB1, cannot be configured as differential. The function MSI46NB1 is an input only pin.*
2. *For M2GL050-FG484 device, SERDES block is not available in bank 6.*

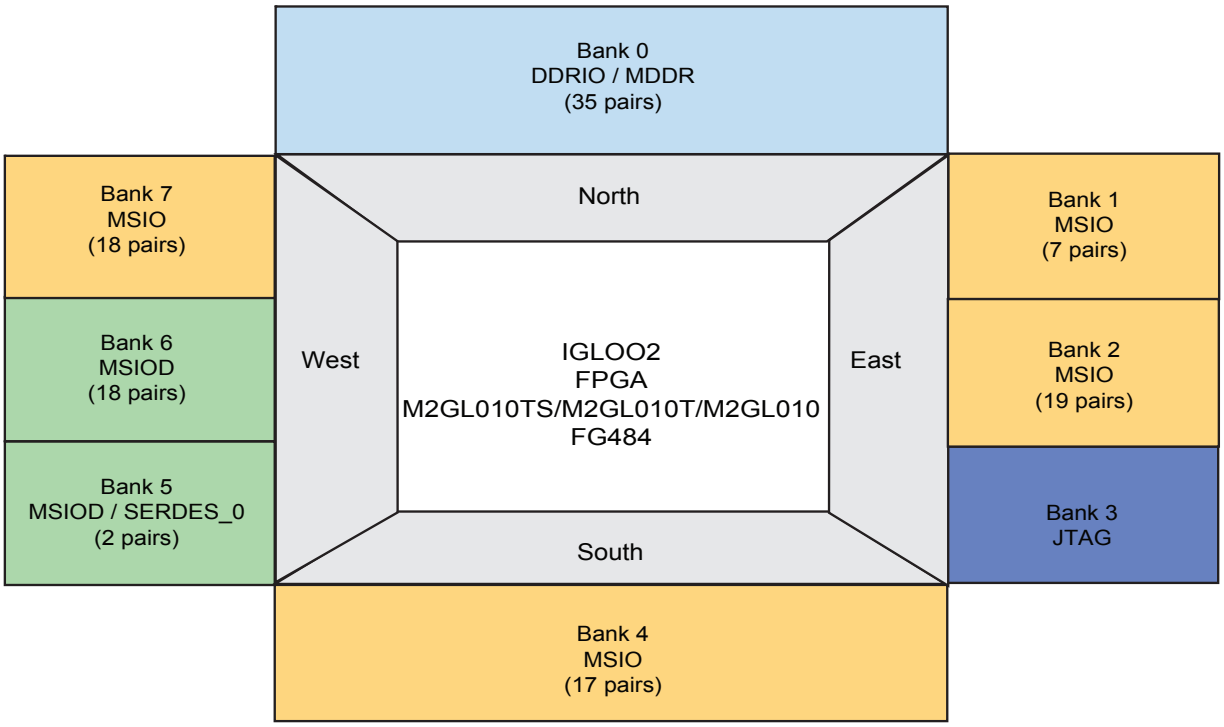
Figure 8 • **IGLOO2 M2GL050TS/M2GL050T/M2GL050-FG484 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D21, MSI32NB1, cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2GL025-FG484 device, SERDES block is not available in bank 5.*

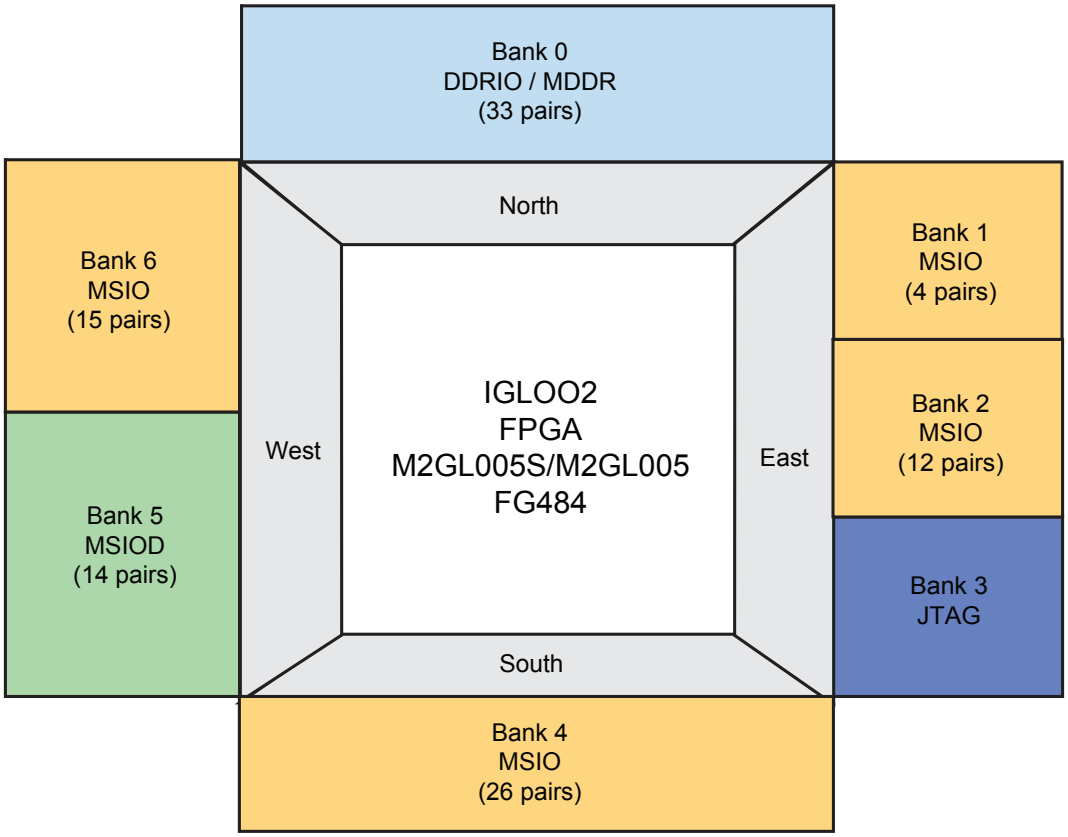
***Figure 9* • IGLOO2 M2GL025TS/M2GL025T/M2GL025-FG484 I/O Bank Locations**



Notes:

1. *In bank 1, there are 15 single-ended user I/Os. Pin D21, MSI26NB1, cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2GL010-FG484 device, SERDES block is not available in bank 5.*

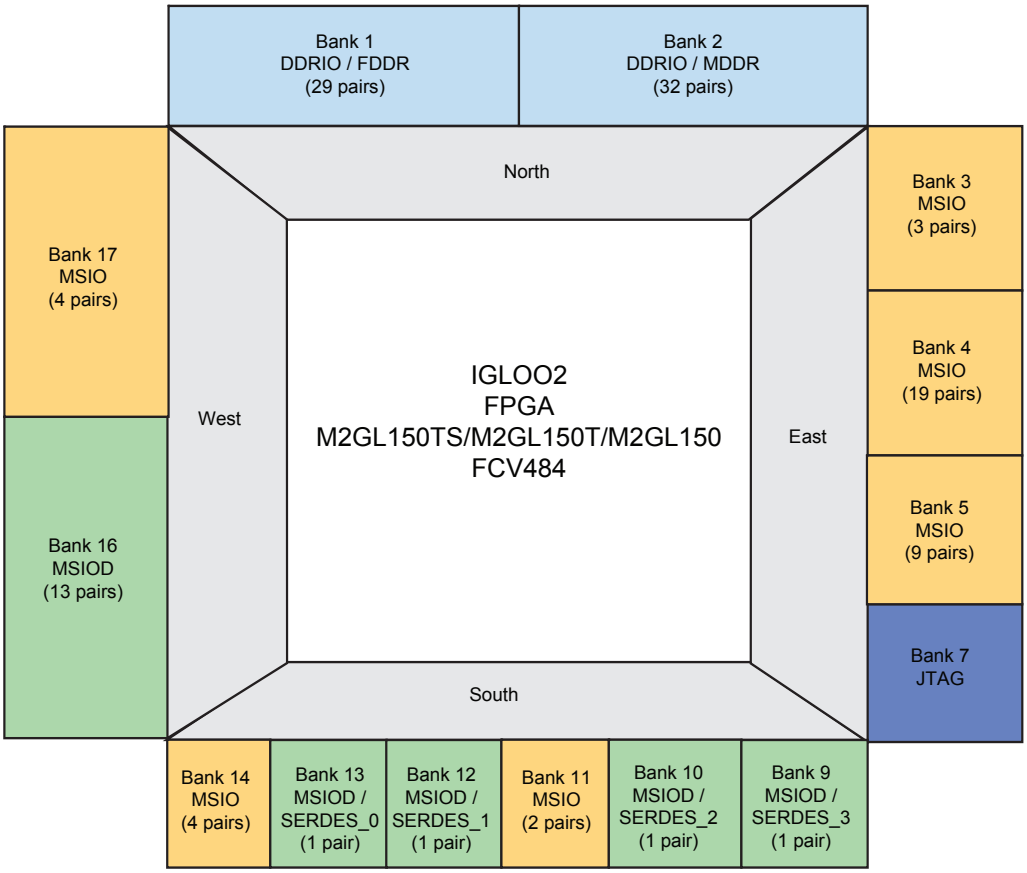
***Figure 10* • IGLOO2 M2GL010TS/M2GL010T/M2GL010-FG484 I/O Bank Locations**



Notes:

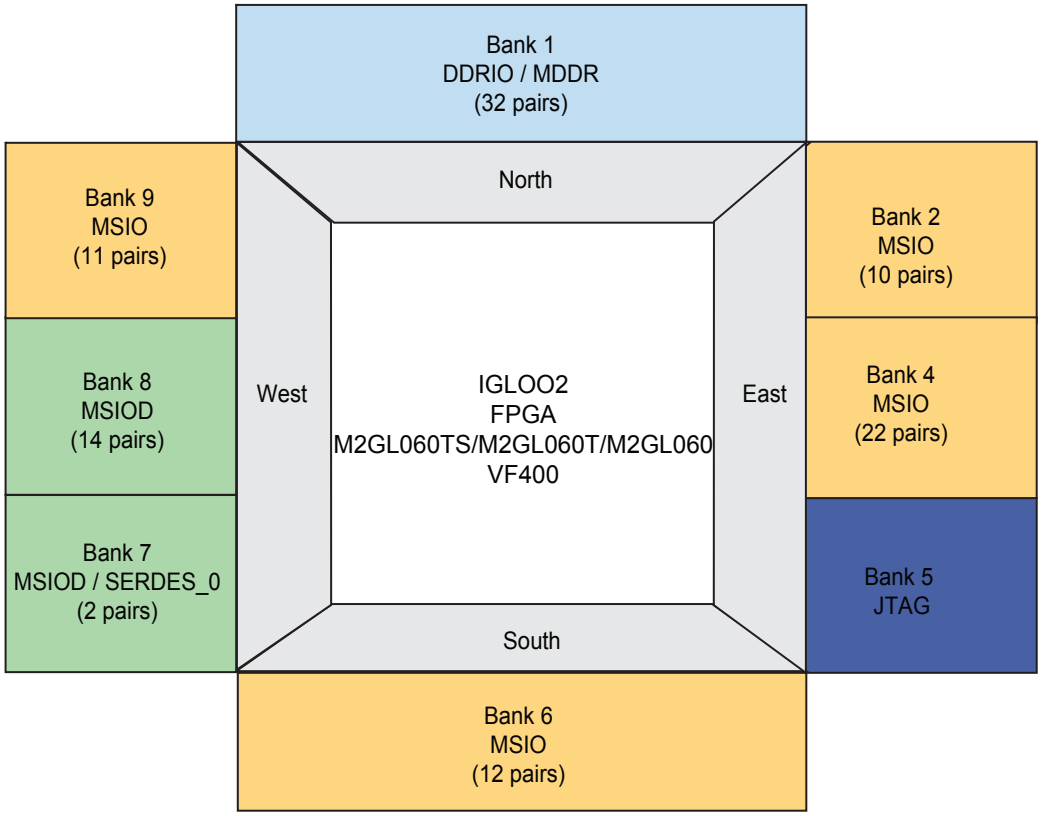
1. *In bank 1, there are 9 single-ended user I/Os. Pin D21 and MSI16NB1 cannot be configured as differential.*
2. *The function MSI16NB1 is an input only pin.*

Figure 11 • **IGLOO2 M2GL005S/M2GL005-FG484 I/O Bank Locations**



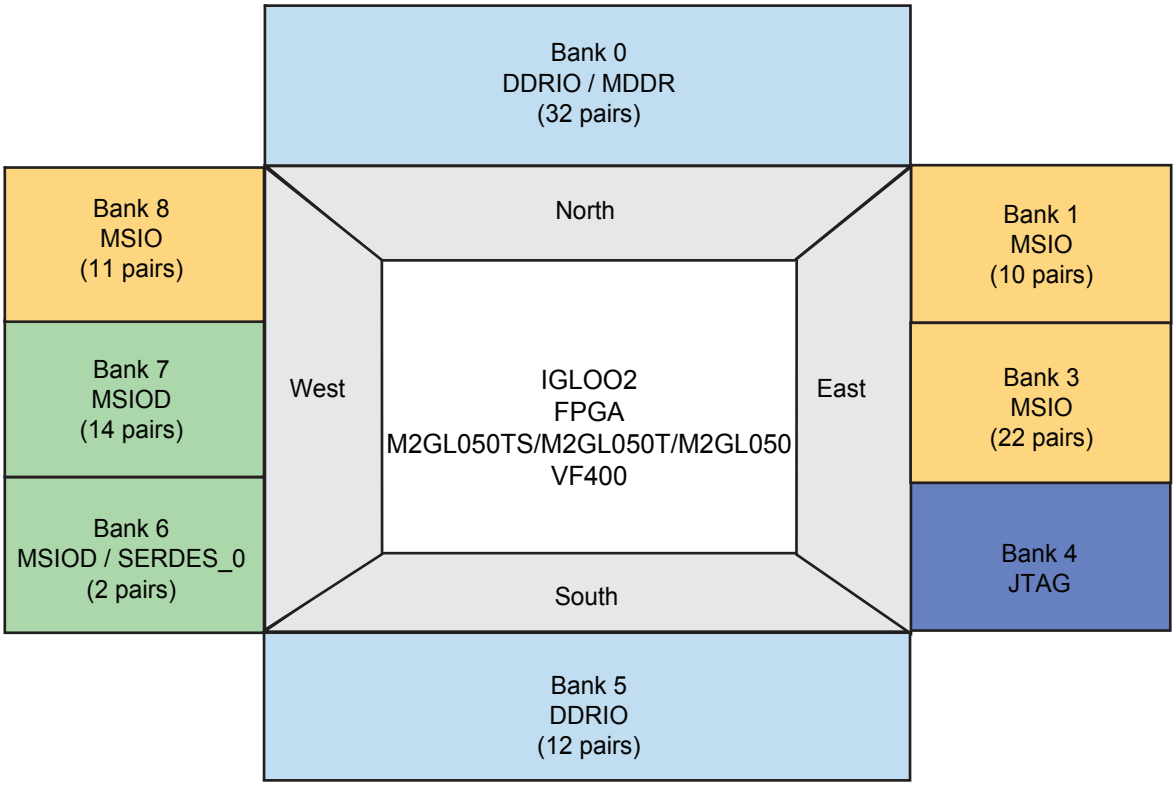
Note: For M2GL150-FCV484 device, SERDES block is not available in banks 9, 10, 12, and 13.

Figure 12 • **IGLOO2 M2GL150TS/M2GL150T/M2GL150-FCV484 I/O Bank Locations**



Note: For M2GL060-VF400 device, SERDES block is not available in bank 7.

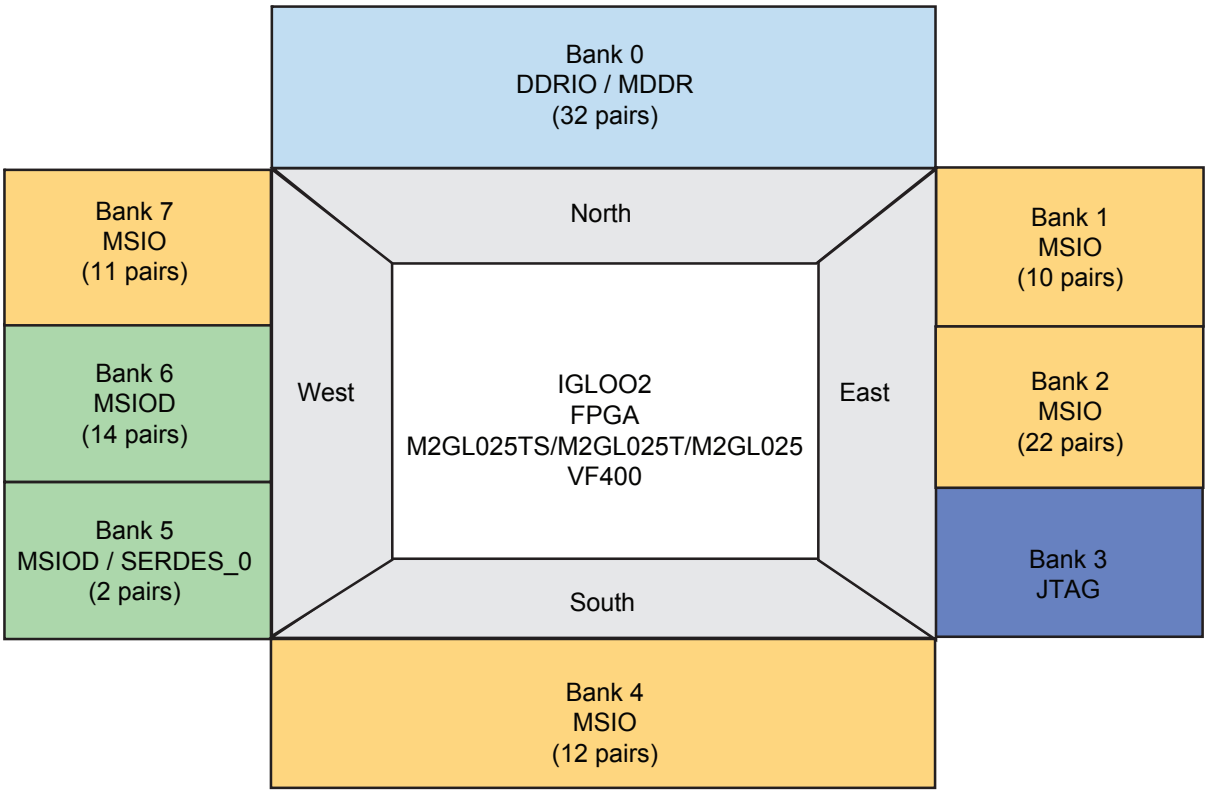
Figure 13 • **IGLOO2 M2GL060TS/M2GL060T/M2GL060-VF400 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D18, MSI46NB1, cannot be configured as differential. The function MSI46NB1 is an input only pin.*
2. *For M2GL050-VF400 device, SERDES block is not available in bank 6.*

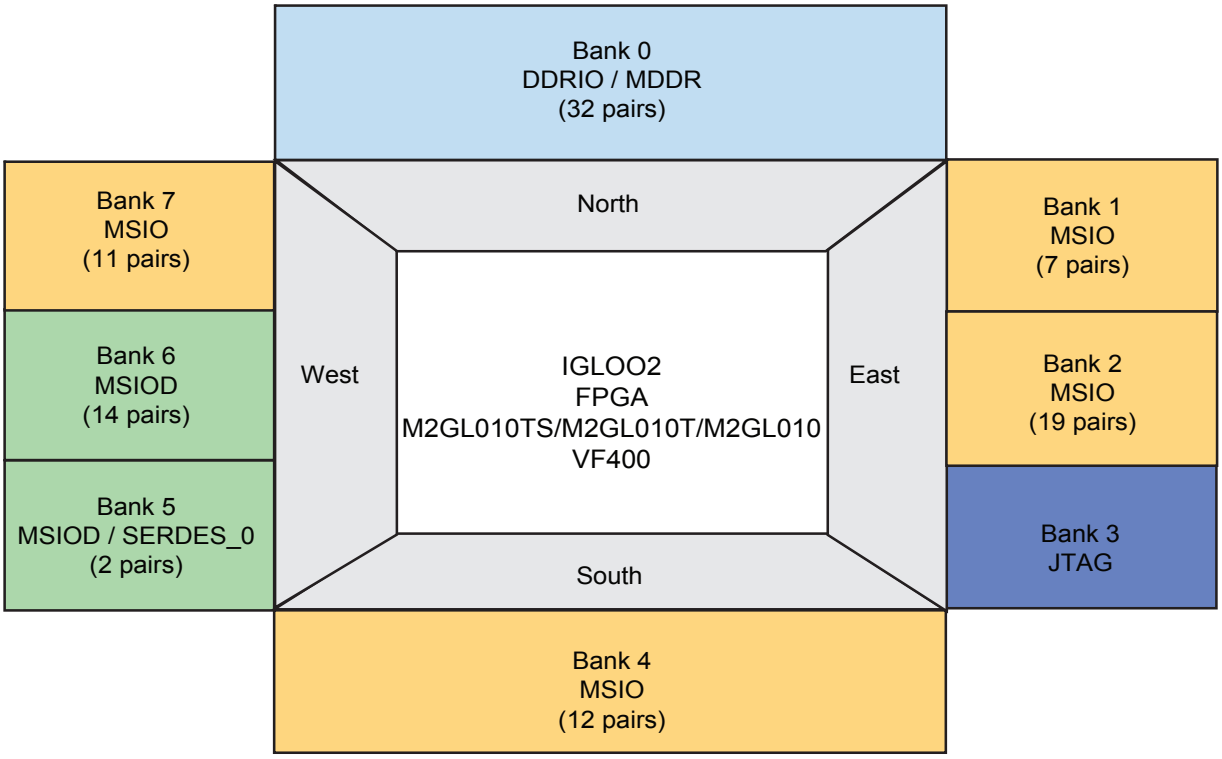
Figure 14 • **IGLOO2 M2GL050TS/M2GL050T/M2GL050-VF400 I/O Bank Locations**



Notes:

1. *In bank 1, there are 21 single-ended user I/Os. Pin D18, MSI32NB1, cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2GL025-VF400 device, SERDES block is not available in bank 5.*

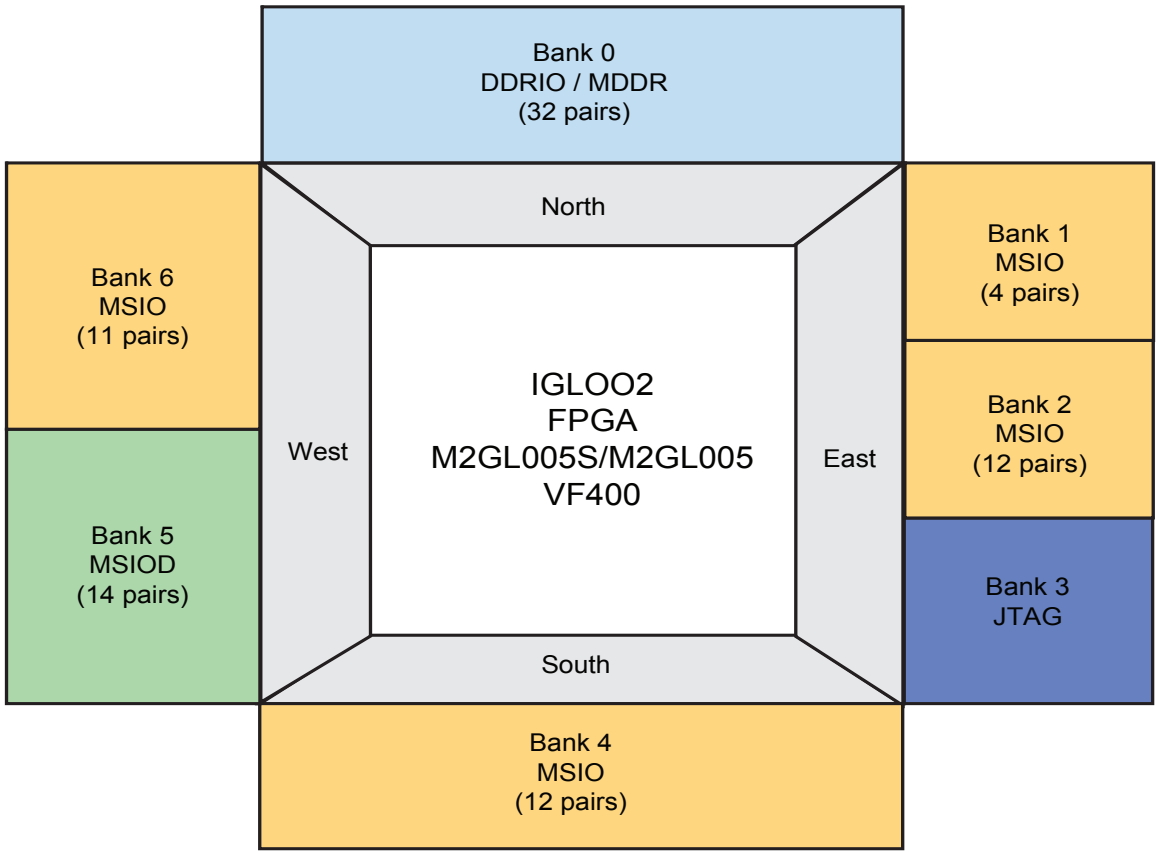
Figure 15 • **IGLOO2 M2GL025TS/M2GL025T/M2GL025-VF400 I/O Bank Locations**



Notes:

1. *In bank 1, there are 15 single-ended user I/Os. Pin- D18, MSI26NB1, cannot be configured as differential. The function MSI26NB1 is an input only pin.*
2. *For M2GL010-VF400 device, SERDES block is not available in bank 5.*

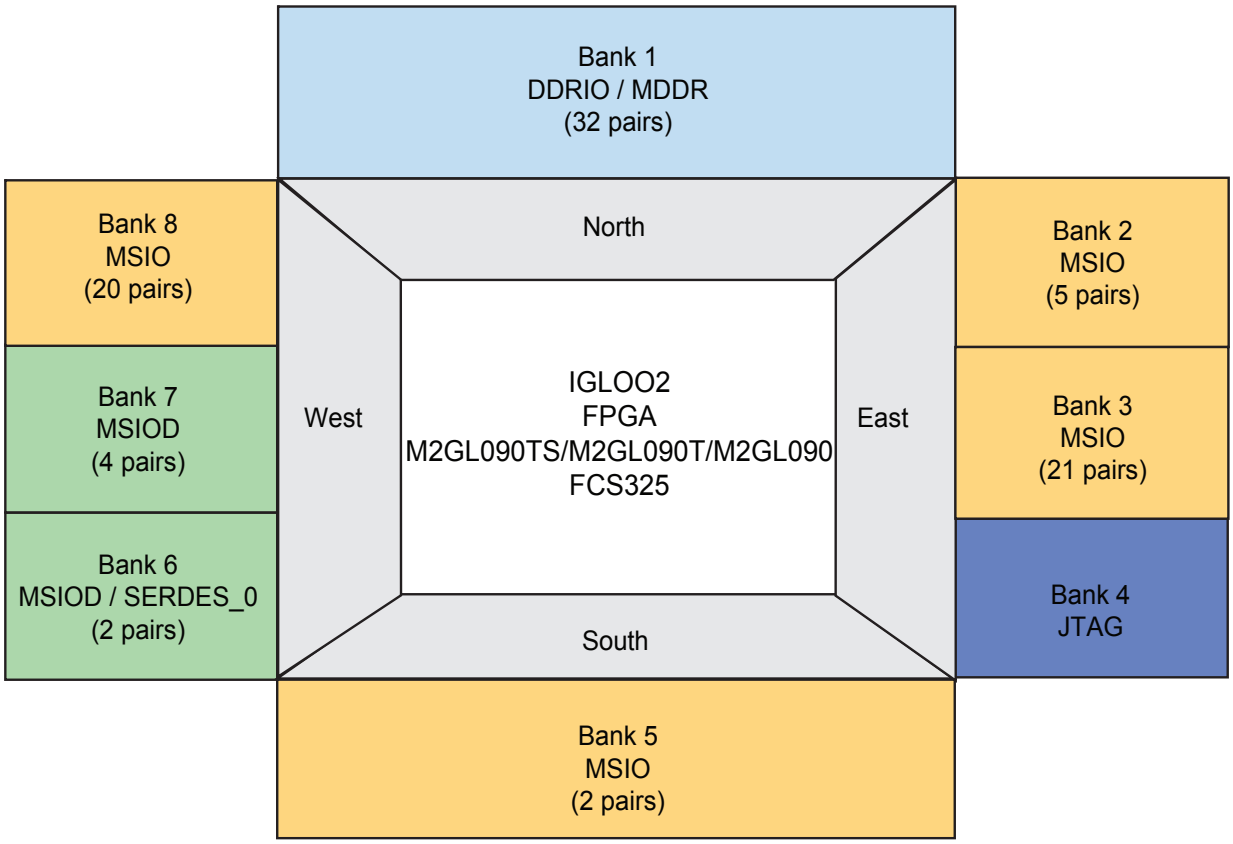
***Figure 16* • IGLOO2 M2GL010TS/M2GL010T/M2GL010-VF400 I/O Bank Locations**



Notes:

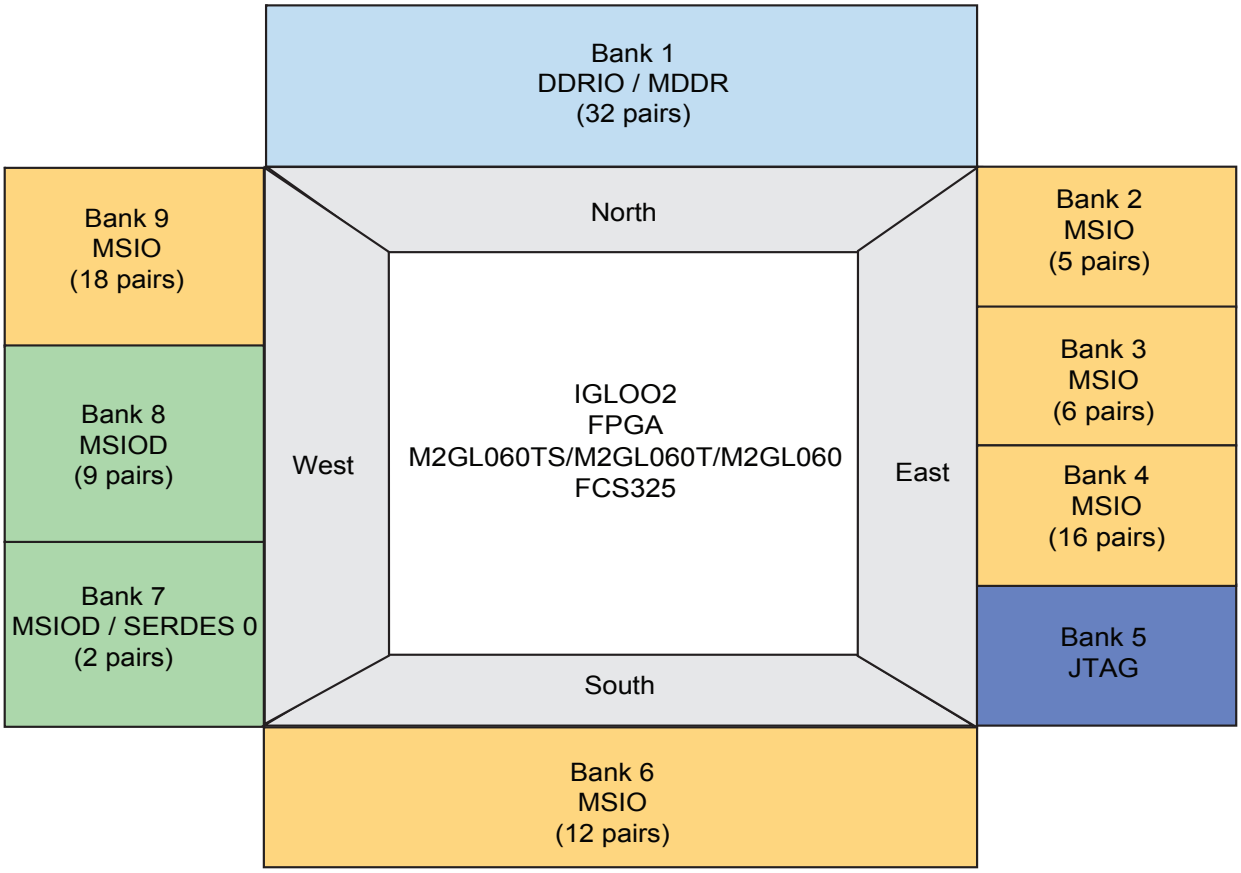
1. *In bank 1, there are 9 single-ended user I/Os. Pin D18, MSI16NB1 cannot be configured as differential.*
2. *The function MSI16NB1 is an input only pin.*

Figure 17 • **IGLOO2 M2GL005S/M2GL005-VF400 I/O Bank Locations**



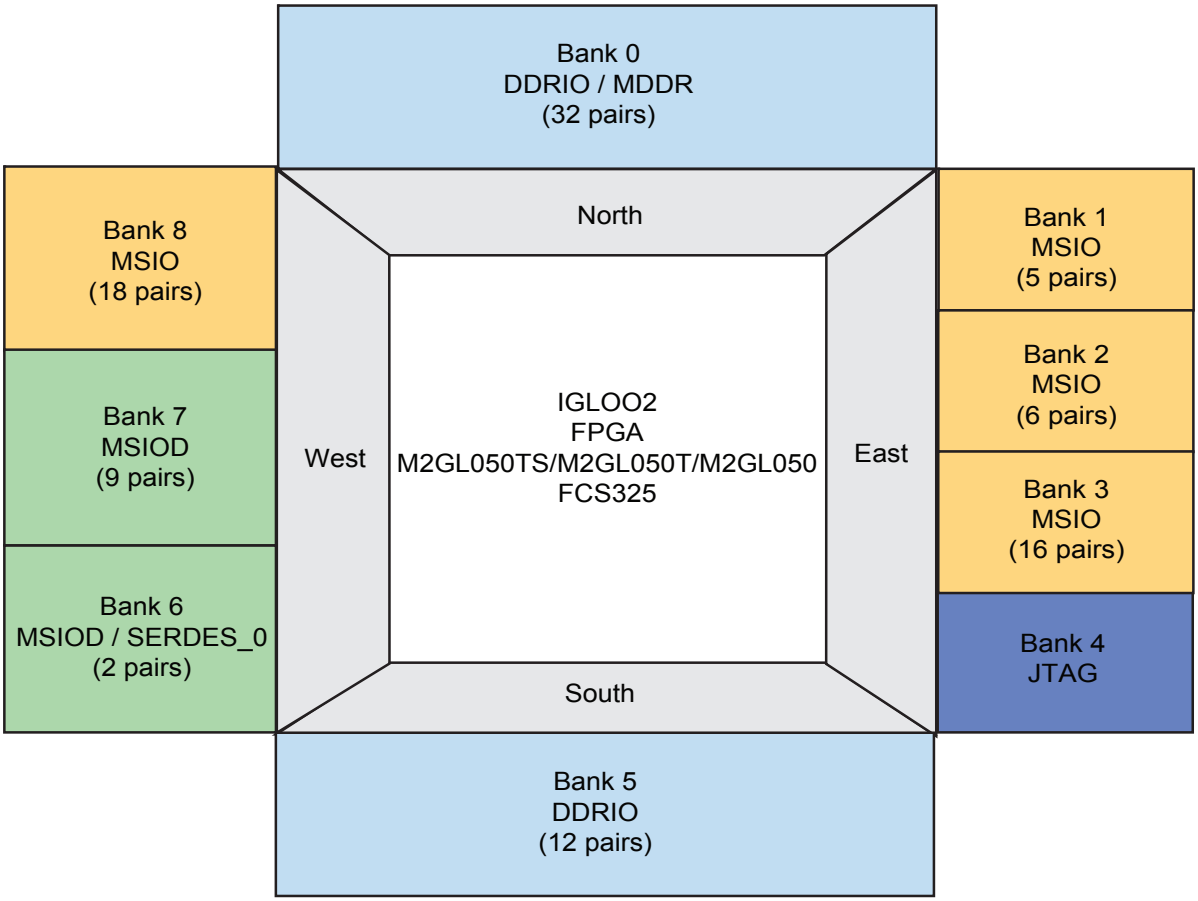
Note: For M2GL090-FCS325 device, SERDES block is not available in bank 6.

Figure 18 • **IGLOO2 M2GL090TS/M2GL090T/M2GL090-FCS325 I/O Bank Locations**



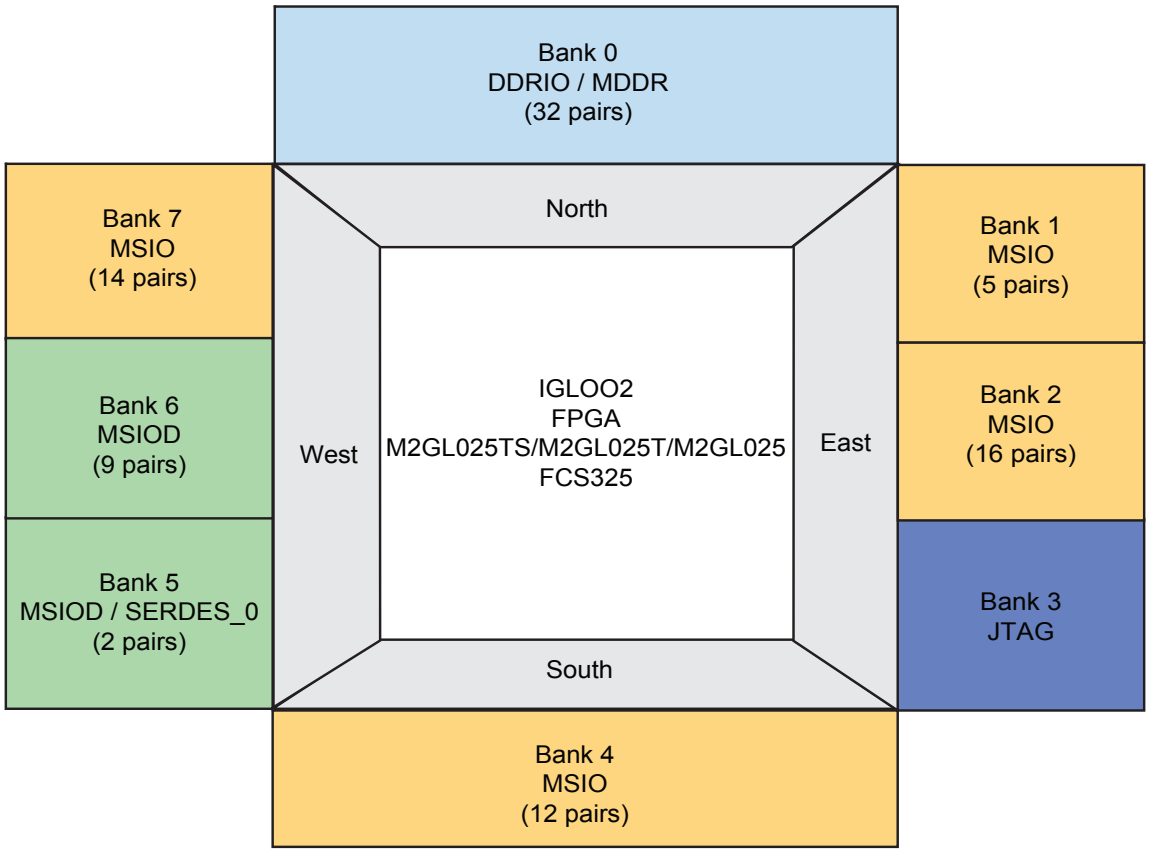
Note: For M2GL060-FCS325 device, SERDES block is not available in bank 7.

Figure 19 • **IGLOO2 M2GL060TS/M2GL060T/M2GL060-FCS325 I/O Bank Locations**



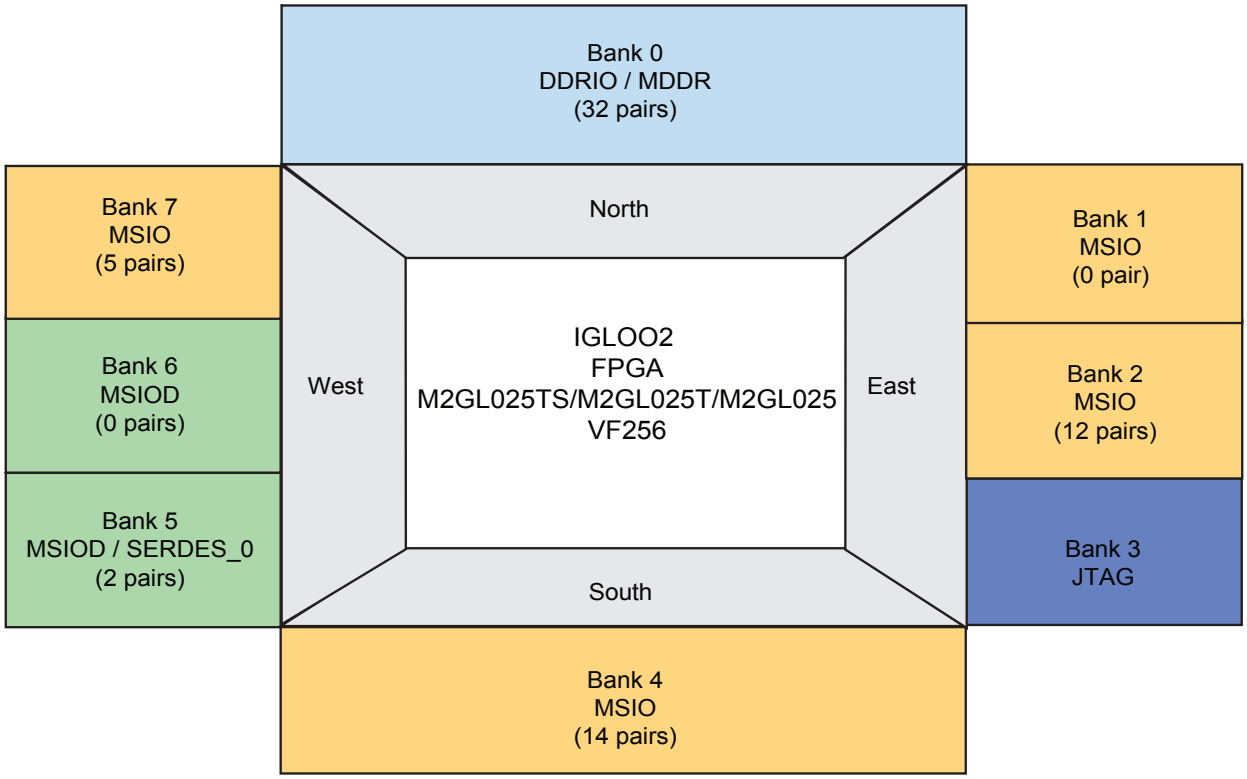
Note: For M2GL050-FCS325 device, SERDES block is not available in bank 6.

Figure 20 • **IGLOO2 M2GL050TS/M2GL050T/M2GL050-FCS325 I/O Bank Locations**



Note: For M2GL025-FCS325 device, SERDES block is not available in bank 5.

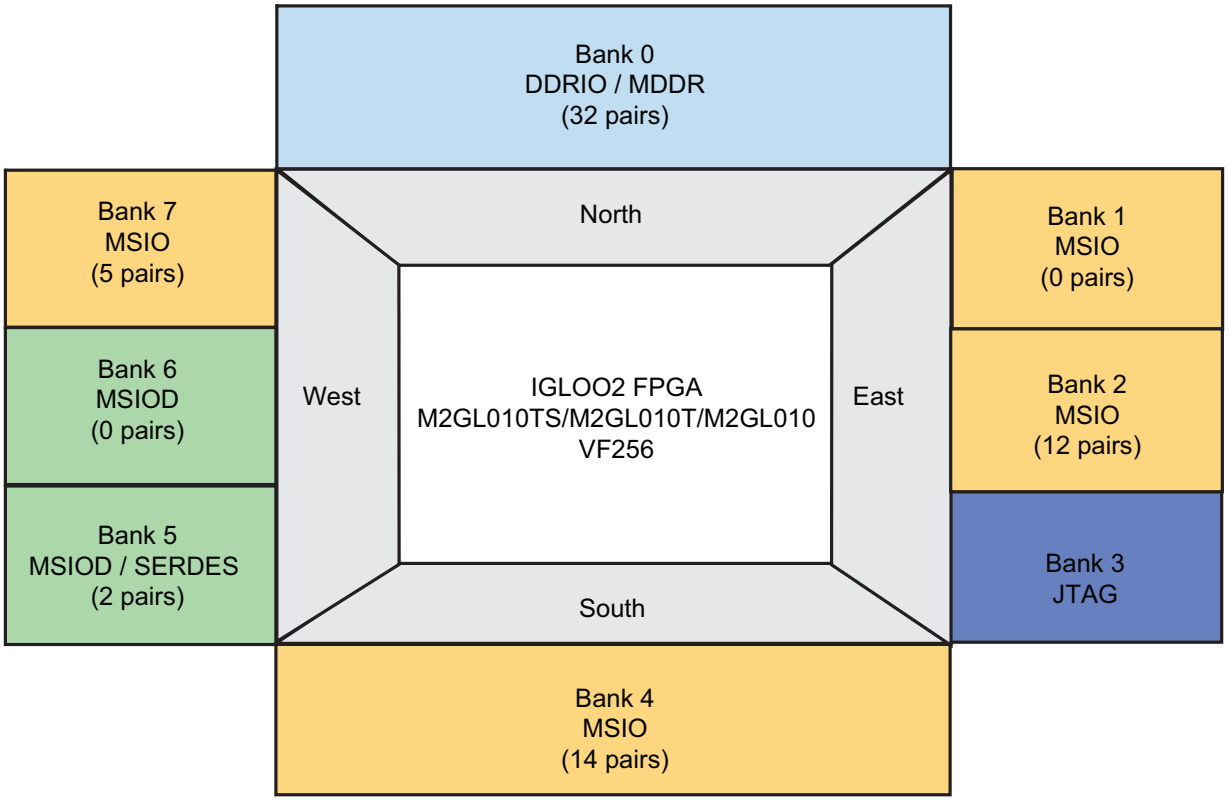
Figure 21 • **IGLOO2 M2GL025TS/M2GL025T/M2GL025-FCS325 I/O Bank Locations**



Notes:

1. *In bank 1, there are 4 single-ended user I/Os. Pin G12, MSIO32NB1 cannot be configured as differential. The function MSI32NB1 is an input only pin.*
2. *For M2GL025-VF256 device, SERDES block is not available in bank 5.*

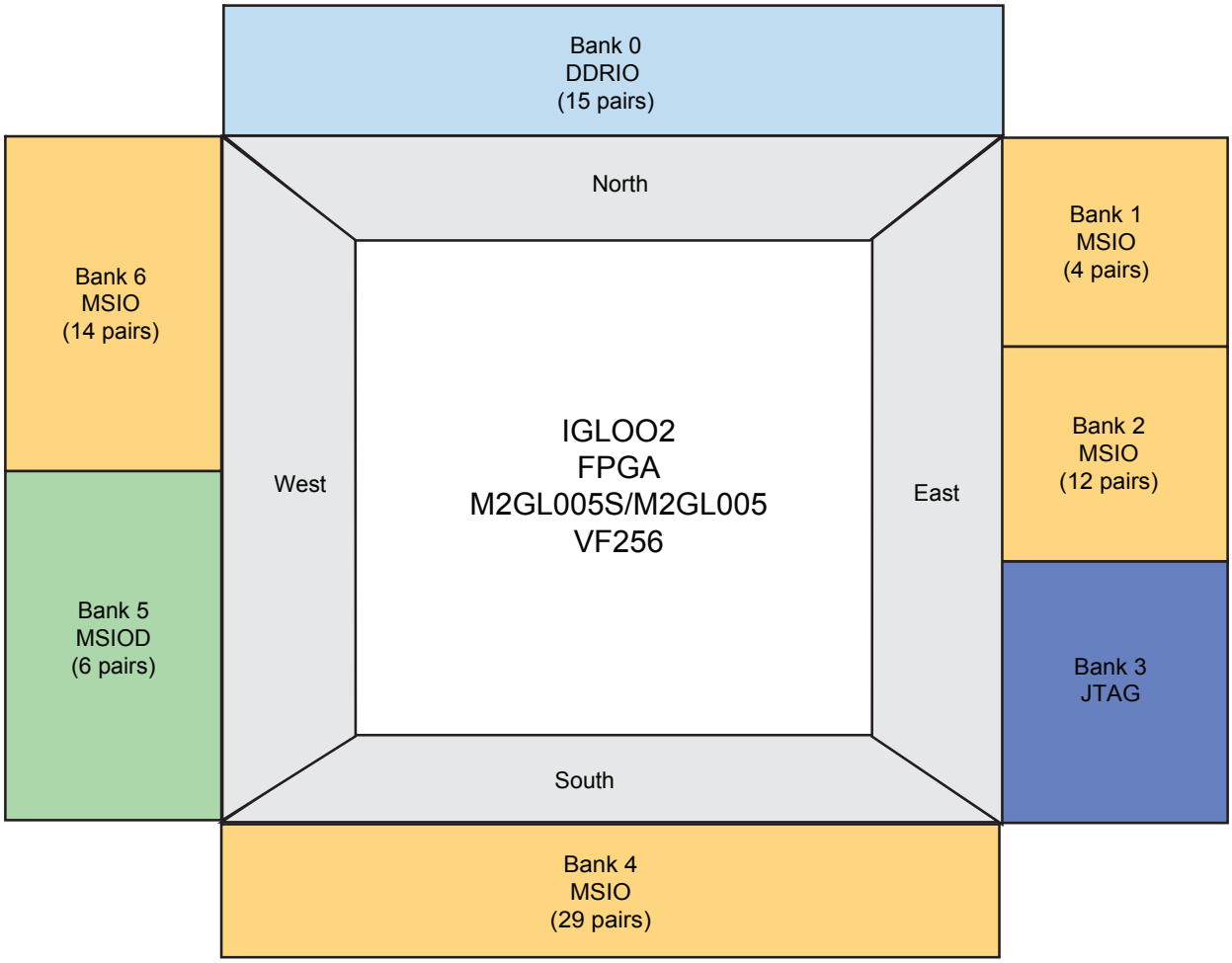
Figure 22 • **IGLOO2 M2GL025TS/M2GL025T/M2GL025-VF256 I/O Bank Locations**



Notes:

1. *In bank 1, there are 4 single-ended user I/Os. Pin G12, MSI26NB1 cannot be configured as differential. The function MSI26NB1 is an input only pin.*
2. *For M2GL010-VF256 device, SERDES block is not available in bank 5.*

Figure 23 • **IGLOO2 M2GL010TS/M2GL010T/M2GL010-VF256 I/O Bank Locations**



Note: In bank 1, there are 9 single-ended user I/Os. Pin D12, MSI16NB1 cannot be configured as differential. The function MSI16NB1 is an input only pin.

Figure 24 • **IGLOO2 M2GL005S/M2GL005-VF256 I/O Bank Locations**

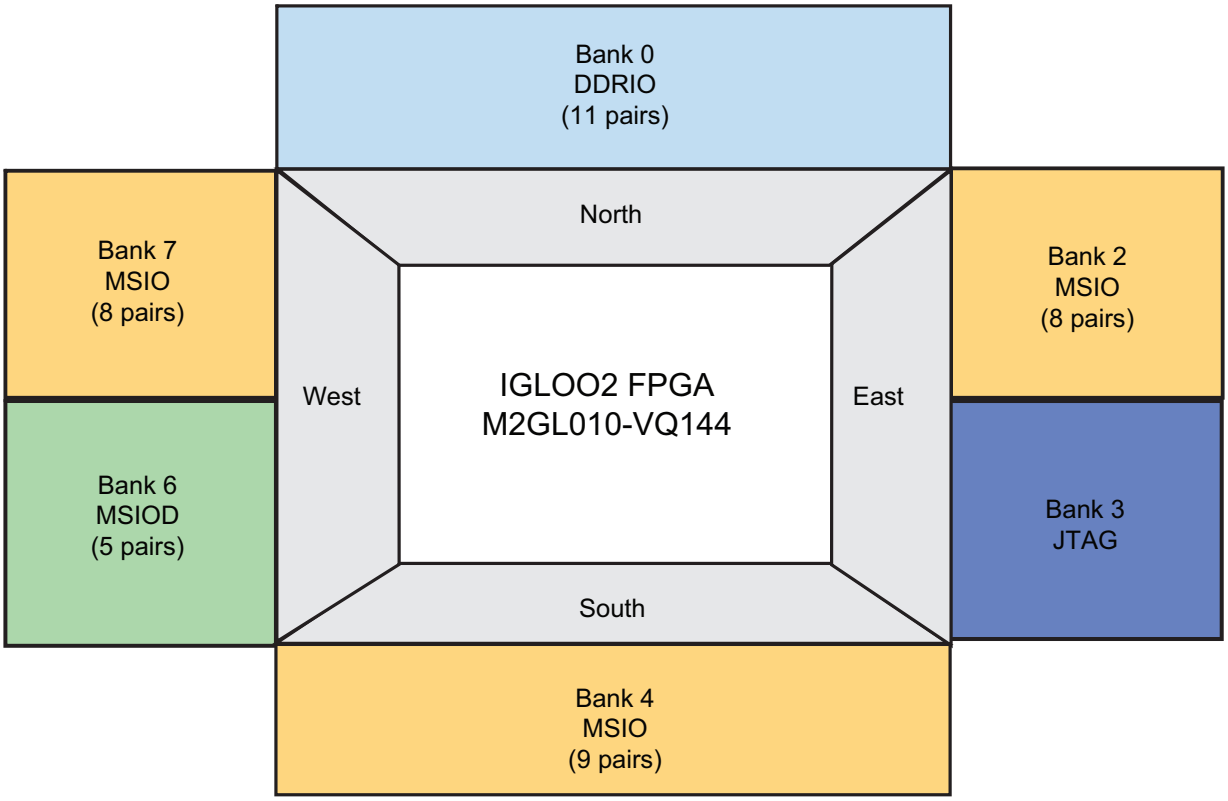


Figure 25 • **IGLOO2 M2GL010-TQ144 I/O Bank Locations**

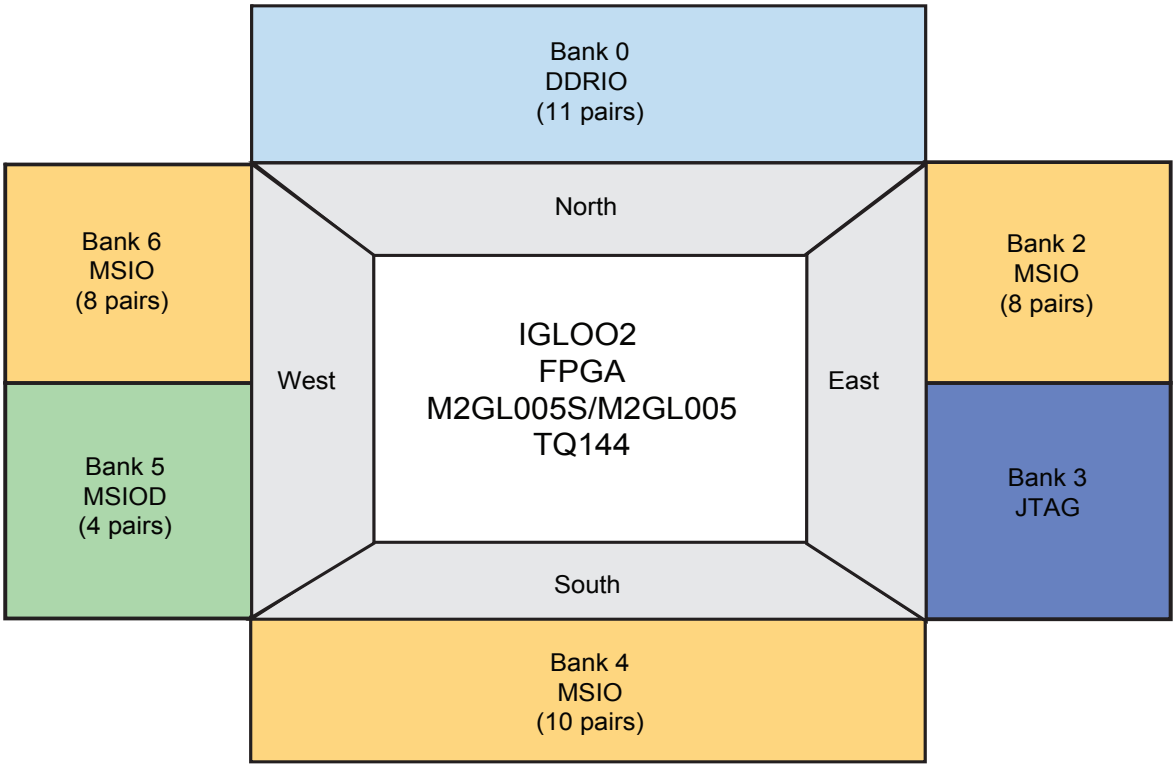


Figure 26 • **IGLOO2 M2GL005S/M2GL005-TQ144 I/O Bank Locations**

Table 1 • **Organization of I/O Banks in IGLOO2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484**

	FC1152	FG896	FG676		FCS536	FCV484	FG484					
Bank No.	**M2GL150TS M2GL150T M2GL150**	**M2GL050TS M2GL050T M2GL050**	**M2GL090TS M2GL090T M2GL090**	**M2GL060TS M2GL060T M2GL060**	**M2GL150TS M2GL150T M2GL150**	**M2GL150TS M2GL150T M2GL150**	**M2GL090TS M2GL090T M2GL090**	**M2GL060TS M2GL060T M2GL060**	**M2GL050TS M2GL050T M2GL050**	**M2GL025TS M2GL050T M2GL025**	**M2GL010TS M2GL010T M2GL010**	**M2GL005S**
Bank 0	MSIO: fabric	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	–	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 1	DDRIO: FDDR or fabric	MSIO: fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: FDDR or fabric	DDRIO: FDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 2	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric	–	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 3	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric		MSIO: fabric	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD
Bank 4	MSIO: fabric	JTAG/ SWD	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	JTAG/ SWD	MSIO: fabric	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 5	MSIO: fabric	DDRIO: FDDR or fabric	MSIO: fabric	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	JTAG/ SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric
Bank 6	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	–	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric
Bank 7	JTAG/ SWD	MSIOD: fabric	MSIOD: fabric	MSIOD: SERDES 0 or fabric	JTAG/ SWD	JTAG/ SWD	MSIOD: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	–
Bank 8	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	–	MSIO: fabric	MSIOD: fabric	MSIO: fabric	–	–	–
Bank 9	MSIOD: SERDES 3 or fabric	MSIOD: SERDES 1 or fabric	–	MSIO: fabric	MSIOD: SERDES 3 or fabric	MSIOD: SERDES 3 or fabric	–	MSIO: fabric	–	–	–	–
Bank 10	MSIOD: SERDES 2 or fabric	–	–	–	MSIOD: SERDES 2 or fabric	MSIOD: SERDES 2 or fabric	–	–	–	–	–	–

Table 1 • **Organization of I/O Banks in IGLOO2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 (continued)**

	FC1152	FG896	FG676		FCS536	FCV484	FG484					
Bank No.	**M2GL150TS M2GL150T M2GL150**	**M2GL050TS M2GL050T M2GL050**	**M2GL090TS M2GL090T M2GL090**	**M2GL060TS M2GL060T M2GL060**	**M2GL150TS M2GL150T M2GL150**	**M2GL150TS M2GL150T M2GL150**	**M2GL090TS M2GL090T M2GL090**	**M2GL060TS M2GL060T M2GL060**	**M2GL050TS M2GL050T M2GL050**	**M2GL025TS M2GL050T M2GL025**	**M2GL010TS M2GL010T M2GL010**	**M2GL005S**
Bank 11	MSIO: fabric	–	–	–	MSIO: fabric	MSIO: fabric	–	–	–	–	–	–
Bank 12	MSIOD: SERDES 1 or fabric	–	–	–	MSIOD: SERDES 1 or fabric	MSIOD: SERDES 1 or fabric	–	–	–	–	–	–
Bank 13	MSIOD: SERDES 0 or fabric	–	–	–	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	–	–	–	–	–	–
Bank 14	MSIO: fabric	–	–	–	MSIO: fabric	MSIO: fabric	–	–	–	–	–	–
Bank 15	MSIOD: fabric	–	–	–	MSIOD: fabric	–	–	–	–	–	–	–
Bank 16	MSIOD: fabric	–	–	–	MSIOD: fabric	MSIOD: fabric	–	–	–	–	–	–
Bank 17	MSIO: fabric	–	–	–	MSIO: fabric	MSIO: fabric	–	–	–	–	–	–
Bank 18	MSIO: fabric	–	–	–	MSIO: fabric	–	–	–	–	–	–	–

Note: Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 2 • **Organization of I/O Banks in IGLOO2 Devices - VF400, FCS325, VF256, and TQ144**

	VF400					FCS325				VF256			TQ144	
Bank No.	**M2GL060TS M2GL060T M2GL060**	**M2GL050TS M2GL050T M2GL050**	**M2GL025TS M2GL025T M2GL025**	**M2GL010TS M2GL010T M2GL010**	**M2GL005S**	**M2GL090TS M2GL090T M2GL090**	**M2GL060TS M2GL060T M2GL060**	**M2GL050TS M2GL050T M2GL050**	**M2GL025TS M2GL025T M2GL025**	**M2GL025TS M2GL025T M2GL025**	**M2GL010TS M2GL010T M2GL010**	**M2GL005S**	**M2GL010**	**M2GL005S**
Bank 0	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	–	–	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	DDRIO: fabric	DDRIO: fabric	DDRIO: fabric
Bank 1	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	–
Bank 2	MSIO: fabric	–	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 3		MSIO: fabric	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD	JTAG/ SWD
Bank 4	MSIO: fabric	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	JTAG/ SWD	MSIO: fabric	JTAG/ SWD	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric
Bank 5	JTAG/ SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	JTAG/ SWD	DDRIO: FDDR or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	–	MSIOD: fabric
Bank 6	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: SERDES 0 or fabric	MSIO: fabric	MSIOD: fabric	MSIOD: fabric	MSIO: fabric	MSIOD: fabric	MSIO: fabric
Bank 7	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	–	MSIOD: fabric	MSIOD: SERDES 0 or fabric	MSIOD: fabric	MSIO: fabric	MSIO: fabric	MSIO: fabric	–	MSIO: fabric	–
Bank 8	MSIOD: fabric	MSIO: fabric	–	–	–	MSIO: fabric	MSIOD: fabric	MSIO: fabric	–	–	–	–	–	–
Bank 9	MSIO: fabric	–	–	–	–	–	MSIO: fabric	–	–	–	–	–	–	–

Note: Banks that are shaded should always be powered with the appropriate VDDI bank supplies.

Table 3 • **User I/O Types**

Name	Type	Description
MSIOxyBz	In/out	MSIOs provide programmable drive strength, weak pull-up, and weak-pull-down. In single-ended mode, the I/O pair operates as two separate I/Os named P and N. IGLOO2 I/O ports also support ESD protection. MSIO I/O cells operate at up to 3.3 V and are capable of high-speed LVDS2V5 and LVDS3V3 operation.
MSIODxyBz	In/out	MSIOD is very similar to MSIO, but drops 3.3 V and hot-plug support and adds pre-emphasis, in order to achieve higher speeds. MSIODs provide programmable drive strength, weak pull-up, and weak pull-down. MSIOD I/O cells operate at up to 2.5 V and are capable of high-speed LVDS2V5 operation. Some of these pins are also multiplexed with the SERDES interface. IGLOO2 I/O ports support ESD protection.
DDRIOxyBz	In/out	The double data input output (DDRIO) is a multi-standard I/O optimized for LPDDR/DDR2/DDR3 performance. In IGLOO2 devices there are two DDR subsystems: the fabric DDR and High Performance Memory Subsystem (HPMS) DDR controllers. All DDRIOs can be configured as differential I/Os or two single-ended I/Os. If you select MDDR/FDDR, Libero® System-on-Chip (SoC) automatically connects MDDR/FDDR signals to the DDRIOs. DDRIOs can be connected to the respective DDR subsystem PHYs or can be used as user I/Os. Depending on the memory configuration, only the required DDRIOs are used by Libero SoC. The unused DDRIOs are available to connect to the fabric.
Note: For more information on I/O status of MSIO, MSIOD and DDRIO pins during power up/down and default conditions, refer to *AC396: SmartFusion2 and IGLOO2 in Hot Swapping and Cold Sparing Application Note*.		

All user IOs have internal clamp diode control circuitry. A pull-up clamp diode must not be present in the I/O circuitry if the hot-swap feature is used. The 3.3 V PCI standard requires a pull-up clamp diode on the I/O, so it cannot be selected if hot-swap capability is required.

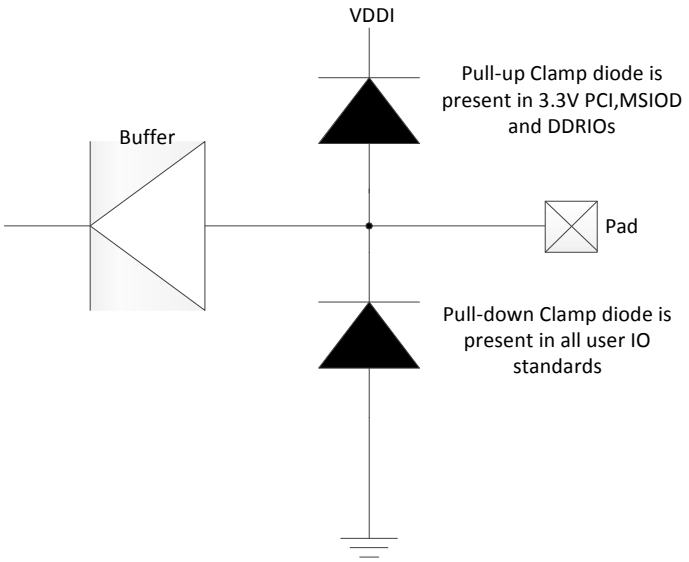


Figure 27 • **Internal Clamp Diode Control Circuitry**

Naming Conventions

User I/O Naming Conventions

The naming convention used for each FPGA user I/O is **IOxyBz**, where:

IO is the type of I/O—MSIO, MSIOD, or DDRIO.

x refers the I/O pair number in bank z.

y is P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/Os named P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.

B is bank.

z refers to bank number (0–9 for M2GL050-FG896).

Differential standards are implemented as true differential outputs and complementary single-ended outputs for SSTL/HSTL. In the single-ended mode, the I/O pair operates as two separate I/Os named P and N. All the configuration and data inputs/outputs are then separate and use names ending in P and N to differentiate between the two I/Os.

For more information, refer to the "I/Os" chapter of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

Dedicated Global I/O Naming Conventions

Dedicated global I/Os are dual-use I/Os which can drive the global blocks either directly or through clock conditioning circuits (CCC) or virtual clock conditioning circuits (VCCC). They can also be used as regular user I/Os. These global I/Os are the primary source for bringing in the external clock inputs into the IGLOO2 device.

In the M2GL050T-FG896 device, there are 16 global blocks located in the center of the fabric and 32 global I/Os located 8 each on the north, east, south, and west sides of the fabric. There are 6 CCC blocks, located 2 each on northwest, northeast, and southwest side of the fabric and 2 VCCC blocks on the southeast side of the fabric.

Dedicated global I/Os that drive the global blocks (GB) directly are named as **GBn,** where

n is 0 to 15.

Dedicated global I/Os that drive GBs through CCCs are named as **CCC_xyz_CLKlw**, where:

xy is the location—NE, SW, or NW.

z is 0 or 1.

l represents input clock

w refers to one of the four possible output clocks of the associated CCC_xyz—GL0, GL1, GL2, or GL3.

Dedicated global I/Os that drive GBs through VCCCs are named as **VCCC_SEz**, where:

SE is southeast.

z is 0 or 1.

Unused dedicated global I/Os behave similarly to unused regular User I/Os (MSIO, MSIOD, DDRIO).

Libero configures unused User I/Os as input buffer disabled, output buffer tristated with weak pull-up.

For further details, refer to the "Fabric Global Routing Resources" chapter of the *UG0449: SmartFusion2 SoC FPGA and IGLOO2 FPGA Clocking Resources User Guide*.

MDDR/FDDR Interface

IGLOO2 devices have MDDR/FDDR blocks. The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR, DDR2, and DDR3 memories. It supports 8-/16-/32-bit data bus width modes. The DDRIO uses fixed impedance calibration for different drive strengths. These values can be programmed using Libero SoC software for the selected I/O standard. The values are fed to the pull-up/pull-down reference network to match the impedance with an external resistor. For more information about reference resistor values (for different drive modes), refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

DDR Controller Pins

Table 4 shows the DDR Controller pins.

Table 4 • **DDR Controller Pins**

Pin Name	Type	Reference Resistor (Ω)
xDDR_CAS_N	Out	DRAM CASN.
xDDR_CKE	Out	DRAM Clock enable.
xDDR_CLK	Out	DRAM single-ended clock for differential pads.
xDDR_CLK_N	Out	DRAM single-ended clock for differential pads.
xDDR_CS_N	Out	DRAM Chip select.
xDDR_ODT	Out	DRAM on-die termination (ODT). 0: Termination OFF 1: Termination ON
xDDR_RAS_N	Out	DRAM RASN
xDDR_RESET_N	Out	DRAM reset for DDR3
xDDR_WE_N	Out	DRAM Write enable
xDDR_ADDR[15:0]	Out	DRAM address bits.
xDDR_BA[2:0]	Out	DRAM bank address.
xDDR_DM_RDQS[3:0]	In/out	DRAM data mask from bidirectional pads.
xDDR_DQS[3:0]	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS[3:0]_N	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQ[31:0]	In/out	DRAM data input or output for bidirectional pads.
xDDR_DQ_ECC[3:0]	In/out	DRAM data input or output for SECDED.
xDDR_DM_RDQS_ECC	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS_ECC	In/out	DRAM single-ended data strobe output for bidirectional pads.
xDDR_DQS_ECC_N	In/out	DRAM data input or output for bidirectional pads.
xDDR_TMATCH_[0/1]_IN	In	DQS enable input for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_[0/1]_OUT.
xDDR_TMATCH_[0/1]_OUT	Out	DQS enable output for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_[0/1]_IN.
xDDR_TMATCH_ECC_IN	In	DQS enable input for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_ECC_OUT.

Notes:

1. *Though calibration is not required, it is recommended to use corresponding resistor placeholder to connect the xDDR_IMP_CALIB to the ground with or without a resistor.*
2. *x represents Fabric or MSS DDR.*

Table 4 • **DDR Controller Pins (continued)**

xDDR_TMATCH_ECC_OUT	Out	DQS enable output for timing match between DQS and system clock. For simulations, tie to xDDR_TMATCH_ECC_IN.
xDDR_IMP_CALIB	Ref	Pull-down with resistor depending on voltage/standard: • DDR2 - 150 Ω • DDR3 (1.5 V) - 240 Ω • LPDDR - 150 Ω

Notes:

1. *Though calibration is not required, it is recommended to use corresponding resistor placeholder to connect the xDDR_IMP_CALIB to the ground with or without a resistor.*
2. *x represents Fabric or MSS DDR.*

For more information about DDR memory calibration, refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

For DDR termination details refer *AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note*.

I/O Standards

Table 5 shows the supported I/O standards for different DDR memories.

Table 5 • **Supported I/O Standards for Different DDR Memories**

Memory Type	I/O Standard
DDR3	SSTL15I, SSTL15II
DDR2	SSTL18I, SSTL18II
LPDDR	LVCMOS18

Supply Pins

IGLOO2 devices support multi-standard I/Os (MSIOs), MSIODs, double data rate I/Os (DDRIOs), high performance memory subsystem (HPMS), high speed serial interfaces, and a debugging JTAG interface. IGLOO2 devices require the power supplies listed in Table 6.

Table 6 • **Supply Pins**

Name	Type	Description
VDD	Supply	DC core supply voltage. Must always power this pin.
VPP	Supply[1]	Power supply for charge pumps (for normal operation and programming). Must always power this pin.
VPPNVM	Supply[1]	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.
VDDIx	Bank power supplies[2]	VDDIx, Bank x power
VREFx	Supply[3]	Reference voltage for MDDR signals which is powered through corresponding Bank Supply (VDDIx). When **unused**, VREFx can be DNC or grounded (VSS).
CCC_NE0_PLL_VDDA	PLL power supplies[4]	Analog power pad for PLL0
CCC_NE1_PLL_VDDA		Analog power pad for PLL1
CCC_NW0_PLL_VDDA		Analog power pad for PLL2
CCC_NW1_PLL_VDDA		Analog power pad for PLL3
CCC_SW0_PLL_VDDA		Analog power pad for PLL4
CCC_SW1_PLL_VDDA		Analog power pad for PLL5
HPMS_MDDR_PLL_VDDA		Analog power pad for PLL of MDDR and HPMS
FDDR_PLL_VDDA		Analog power pad for PLL of FDDR

Notes:

1. *For details on VPP and VPPNVM power supplies, refer to Table 2 - Recommended Operating Conditions of the DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet.*
2. *For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*
3. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are being used as single-ended I/Os (and MDDR or FDDR functionalities are not being used), then VREFx can be left floating (DNC) even though the VDDIx powered to the corresponding supplies.*
4. *If used as PLL, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding on-board PLL return path. If PLL is unused or used as divider, the supply must connect directly to either 2.5 V or 3.3 V (without filter circuitry).*
5. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding on-board return path. If **unused**, must connect directly to the appropriate supplies (without filter circuitry).*
6. *If used, all CCC PLL pins must be powered through resistor and capacitors (filter circuitry) to the appropriate supply to the corresponding on-board return path. If unused must connect directly to the Ground (without filter circuitry).*

Table 6 • **Supply Pins (continued)**

Name	Type	Description
SERDES_x_VDD	SERDESx power supplies[5]	PCIe/PCS supply. It is a +1.2 V supply and internally shorted to VDD.
SERDES_x_L01_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for Lane0 and Lane1 of SERDESIFx, located on the left side. It is a +1.2 V SERDES PMA supply.
SERDES_x_L23_VDDAIO		Tx/Rx analog I/O voltage. Low voltage power for Lane2 and Lane3 of SERDESIFx, located on the right side. It is a +1.2 V SERDES PMA supply.
SERDES_x_L01_VDDAPLL		Analog power for SERDESx PLL of Lane0 and Lane1. In used condition, it must be connected to +2.5 V. In unused condition, it can be connected to either +2.5 V or VDD (1.2 V).
SERDES_x_L23_VDDAPLL		Analog power for SERDESx PLL of Lane0 and Lane1. In used condition, it must be connected to +2.5 V. In unused condition, it can be connected to either +2.5 V or VDD (1.2 V).
SERDES_x_L01_REFRET		Local on-chip ground return path for SERDES_x_L01_VDDAPLL for Lane0 and Lane1 of SERDESIF0, located on the left side. If unused, it must be grounded (VSS).
SERDES_x_L23_REFRET		Local on-chip ground return path for SERDES_x_L23_VDDAPLL for Lane2 and Lane3 of SERDESIF0, located on the right side. If unused, it must be grounded (VSS).
SERDES_x_PLL_VDDA		High supply voltage for PLL SERDESx. It can be +2.5 V or +3.3 V.
SERDES_x_PLL_VSSA		VDDA to on-die VSSA high pass filter connection for PLL SERDESx. If unused, it must be grounded (VSS).
CCC_NE0_PLL_VSSA	PLL return paths[6]	Return path for corresponding analog PLL VDDA supply. High frequency noise should be eliminated by placing the R-C filter circuitry in between VDDA and VSSA pins.
CCC_NE_PLL_VSSA		
CCC_NW0_PLL_VSSA		
CCC_NW1_PLL_VSSA		
CCC_SW0_PLL_VSSA		
CCC_SW1_PLL_VSSA		
HPMS_MDDR_PLL_VSSA		Analog ground pad for PLL of MDDR and HPMS
FDDR_PLL_VSSA		Analog ground pad for PLL of FDDR

Notes:

1. *For details on VPP and VPPNVM power supplies, refer to Table 2 - Recommended Operating Conditions of the DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet.*
2. *For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*
3. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are being used as single-ended I/Os (and MDDR or FDDR functionalities are not being used), then VREFx can be left floating (DNC) even though the VDDIx powered to the corresponding supplies.*
4. *If used as PLL, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding on-board PLL return path. If PLL is unused or used as divider, the supply must connect directly to either 2.5 V or 3.3 V (without filter circuitry).*
5. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding on-board return path. If **unused**, must connect directly to the appropriate supplies (without filter circuitry).*
6. *If used, all CCC PLL pins must be powered through resistor and capacitors (filter circuitry) to the appropriate supply to the corresponding on-board return path. If unused must connect directly to the Ground (without filter circuitry).*

Table 6 • **Supply Pins (continued)**

Name	Type	Description
VSS	Ground	Ground pad for core and I/Os. Must always connect to ground.
VSSNVM		Analog sense circuit ground of eNVM. Must always connect to ground.

Notes:

1. *For details on VPP and VPPNVM power supplies, refer to Table 2 - Recommended Operating Conditions of the DS0128: IGLOO2 FPGA and SmartFusion2 SoC FPGA Datasheet.*
2. *For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note. For more details on user I/O pins (MSIO, MSIOD, DDRIO) and supported voltage standards, refer to the Supported Voltage Standards table in the UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide.*
3. *Reference voltages should be powered with the appropriate bank supplies through voltage divider circuitry. If I/O banks are being used as single-ended I/Os (and MDDR or FDDR functionalities are not being used), then VREFx can be left floating (DNC) even though the VDDIx powered to the corresponding supplies.*
4. *If used as PLL, the supply must be connected over resistor and capacitors (filter circuitry) to a common PLL supply (2.5 V or 3.3 V) to the corresponding on-board PLL return path. If PLL is unused or used as divider, the supply must connect directly to either 2.5 V or 3.3 V (without filter circuitry).*
5. *If used, all SERDES PLL pins must be powered through resistor and capacitors (filter circuitry) to the correct appropriate supply to the corresponding on-board return path. If **unused**, must connect directly to the appropriate supplies (without filter circuitry).*
6. *If used, all CCC PLL pins must be powered through resistor and capacitors (filter circuitry) to the appropriate supply to the corresponding on-board return path. If unused must connect directly to the Ground (without filter circuitry).*

Additional Notes on Supply Pins

1. As an alternative to leaving unused positive and ground level supplies floating (not connected, open), they can be shorted to VSS on-board. This could be considered a better practice in avionics, so that floating supplies do not pick up charge from radiation.
2. For on-board connectivity solutions, refer to the *AC393: SmartFusion2 SoC FPGA and IGLOO2 FPGA Board Design Guidelines Application Note*.

JTAG Pins

JTAG pins can operate at any voltage—1.2 V / 1.5 V / 1.8 V /2.5 V / 3.3 V (nominal).

Table 7 • **JTAG Pin Names and Descriptions**

Name	Type	Bus Size	Description
JTAGSEL	In	1	JTAG controller selection. JTAGSEL should be pulled high to JTAG bank supply (VDDI) through 1 kΩ resistor.
JTAG_TCK	In	1	Test clock. Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/pull-down resistor. If JTAG is not used, Microsemi recommends tying it off. Connect TCK to GND or +3.3 V through a resistor placed close to the FPGA pin. This prevents totem-pole current on the input buffer and operation in case TMS enters an undesired state. *Note: To operate at all +3.3 V voltages, 500 Ω to 1 kΩ satisfies the requirements.*
JTAG_TDI	In	1	Test data. Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
JTAG_TDO	Out	1	Test data. Serial output for JTAG boundary scan, ISP, and UJTAG usage. The TDO pin does not have an internal pull-up/-down resistor.
JTAG_TMS	–	1	Test mode select. The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, and TRST). There is an internal weak pull-up resistor on the TMS pin.
JTAG_TRSTB	–	1	Boundary scan reset pin. The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor (1 k) could be included to ensure the TAP is held in Reset mode. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends that you tie off TRST to GND through a resistor (1 k) placed close to the FPGA pin.

Programming SPI

The system controller contains a dedicated SPI block for programming. The SPI is operated in either Master or Slave mode. In Master mode, the IGLOO2 device is interfaced with an external SPI flash device and the programming data is downloaded from it to the FPGA. In Slave mode, it is communicated with a remote device that initiates download of the programming data to the FPGA..

Table 8 • **Programming SPI Interface**

Name	Type	Description
SC_SPI_SS	Out	SPI slave select
SC_SPI_SDO	Out	SPI data output
SC_SPI_SDI	In	SPI data input
SC_SPI_CLK	Out	SPI clock
FLASH_GOLDEN_N	In	If pulled Low, this indicates that the device is to be re-programmed from an image in the external SPI flash attached to the SPI interface. If pulled High, the SPI is put into slave mode. Add an external pull-up resistor value of 10 kΩ to VDDI (Bank).

Notes:

1. *If unused, SPI programming pins must be left floating.*
2. *For more details related to reset, clock, and programming, refer to the AC393: SmartFusion2 SoC FPGA and IGLOO2 FPGA Board Design Guidelines Application Note.*
3. *For more information on remaining programming modes, refer to the UG0451: SmartFusion2 SoC FPGA and IGLOO2 FPGA Programming User Guide.*

Dedicated I/Os

Dedicated I/Os (Table 9 and Table 10 on page 39) can be used for a single purpose such as SERDES, device reset, or clock functions. IGLOO2 dedicated I/Os:

- Device reset pins
- Crystal oscillator pins
- SERDES I/Os
- Programming SPI pins

Table 9 • **Device Reset and Crystal Oscillator Pin Types and Descriptions**

Pin	Type	Description
Device Reset I/Os		
DEVRST_n	Input	Device reset; active Low and powered by VPP. It is an asynchronous signal and Schmitt trigger input with the maximum slew rate must not exceed 1 µs. When DEVRST_n is asserted, all user IOs are fully tri-stated. In unused condition, pull up to VPP through 10 kΩ resistor.
Crystal Oscillator I/Os[1, 2]		
XTLOSC_MAIN_EXTAL	Input	Crystal connection or external RC network.
XTLOSC_MAIN_XTAL	Input	Input clock from the main crystal oscillator.

Notes:

1. *The M2GL050 device has only a main crystal oscillator.*
2. *Crystal oscillator pins have a nominal 50 kΩ internal weak pull-ups to VPP. If unused, those pins can be left floating (DNC). The pins should not be grounded (VSS).*

SERDES I/Os

The SERDES I/Os available in IGLOO2 devices are dedicated for high speed serial communication protocols. The SERDES I/Os support protocols such as PCI Express 2.0, XAUI, serial gigabit media independent interface (SGMII), serial rapid IO (SRIO), and any user-defined high speed serial protocol implementation in fabric. Refer to the *AC393: SmartFusion2 SoC FPGA and IGLOO2 FPGA Board Design Guidelines Application Note* for further information.

***Table 10* • SERDES I/O Port Names and Descriptions**

Port Name	Type	Description
Data / Reference Pads		
SERDES_x_RXD0_P	Input[1]	Receive data. SERDES differential positive input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_RXD1_P		
SERDES_x_RXD2_P		
SERDES_x_RXD3_P		
SERDES_x_RXD0_N	Input[1]	Receive data. SERDES differential negative input for each lane. Each SERDESIF consists of 4 RX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1
SERDES_x_RXD1_N		
SERDES_x_RXD2_N		
SERDES_x_RXD3_N		
SERDES_x_TXD0_P	Output[2]	Transmit data. SERDES differential positive output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_TXD1_P		
SERDES_x_TXD2_P		
SERDES_x_TXD3_P		
SERDES_x_TXD0_N	Output[2]	Transmit data. SERDES differential negative output for each lane. Each SERDESIF consists of 4 TX signals. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_TXD1_N		
SERDES_x_TXD2_N		
SERDES_x_TXD3_N		
Common I/O Pads per SERDES Interface		
SERDES_x_L01_REXT	Reference[2]	External reference resistor connection to calibrate TX/RX termination value. Each SERDESIF consists of 2 REXT signals—one for Lane0 and Lane1, and another for Lane2 and Lane3. Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_L23_REXT		
SERDES_x_REFCLK0_P	Clock[3]	Reference clock differential positive. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_REFCLK1_P		
SERDES_x_REFCLK0_N	Clock[3]	Reference clock differential negative. Each SERDESIF consists of two signals (REFCLK0_P, REFCLK1_P). Here x = 0 for SERDESIF_0 and x = 1 for SERDESIF_1.
SERDES_x_REFCLK1_N		

Notes:

1. *If unused, must always connect to VSS (ground).*
2. *If the SERDES unit is not being used, these pins must remain floating (DNC).*
3. *These pins are MUXed with MSIOD functionality. If SERDES functionality and MSIOD functionality are not used, the pins must be left floating. Libero SoC will disable unused I/Os and weakly pull them up.*

Special Pins

The two live probe I/O cells are dual-purpose. If live probe functionality will never be used on these I/Os, the user can configure the I/O as an input, output, or bidirectional. However, if the intent is to perform live switching between the user I/O and probe functionality, then use the I/O only as an output. If it were configured as an input during general use, then as soon as it is switched over to live probe operation, the probe circuitry would drive out onto this I/O, potentially causing device damage.

Table 11 • **Special Pins**

Name	Type	Description
PROBE_A	In/out	The two live probe I/O cells are dual-purpose: 1. Live probe functionality 2. User I/O
PROBE_B	In/out	
CCC_xyz_CLKI0	Input	Input clock from dedicated input pad 0. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI1	Input	Input clock from dedicated input pad 1. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI2	Input	Input clock from dedicated input pad 2. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
CCC_xyz_CLKI3	Input	Input clock from dedicated input pad 3. The xy portion refers to the CCC location (NE, SW, SE, or NW) and z represents the CCC number (0 or 1).
GBx	Input	GB is a multiplexer that generates an independent global signal. The GBs can be driven from multiple sources such as dedicated global I/Os, fabric CCCs, VCCCs, and fabric routing
xDDR_TMATCH_[0/1]_IN	Input	DQS enable input for timing match between DQS and system clock. TMATCH_IN and TMATCH_OUT pins need to be looped back with the trace length as short as possible.
xDDR_TMATCH_[0/1]_OUT	Output	DQS enable output for timing match between DQS and system clock.
DNC	–	Do not connect. This pin should not be connected to any signals on the PCB; leave this pin unconnected.
NC	–	No connect This pin is not connected to circuitry within the device. This pin can be driven to any voltage or can be left floating with no effect on the operation of the device.

Input Only Pins

These pins are differentially paired with Flash_golden_n (input only pin) and are input only when used to connect to the FPGA fabric.

Table 12 • **Input Only Pins**

Device	Pin	Description
M2GL50T-FG896	H27	MSI46NB1 cannot be configured as differential pin and it is an input only pin.
M2GL090T-FG676	D23	MSI59NB2 cannot be configured as differential pin and it is an input only pin.
M2GL090T-FG484	D21	MSI59NB2 cannot be configured as differential pin and it is an input only pin.
M2GL060T-FG484	D21	MSI47NB2, cannot be configured as differential pin and it is input only pin.
M2GL050T-FG484	D21	MSI46NB1 cannot be configured as differential pin and it is an input only pin.
M2GL025T-FG484	D21	MSI32NB1 cannot be configured as differential pin and it is an input only pin.
M2GL010T-FG484	D21	MSI26NB1 cannot be configured as differential pin and it is an input only pin.
M2GL005-FG484	D21	MSI16NB1 cannot be configured as differential pin and it is an input only pin.
M2GL050T-VF400	D18	MSI46NB1 cannot be configured as differential pin and it is an input only pin.
M2GL025T-VF400	D18	MSI32NB1 cannot be configured as differential pin and it is an input only pin.
M2GL010T-VF400	D18	MSI26NB1 cannot be configured as differential pin and it is an input only pin.
M2GL005-VF400	D18	MSI16NB1 cannot be configured as differential pin and it is an input only pin.
M2GL025T-VF256	G12	MSI26NB1 cannot be configured as differential pin and it is an input only pin.
M2GL010T-VF256	G12	MSI26NB1 cannot be configured as differential pin and it is an input only pin.
M2GL005-VF256	D12	MSI16NB1 cannot be configured as differential pin and it is an input only pin.

High Performance Memory Subsystem

Table 13 • **High Performance Memory Subsystem Pin Names and Descriptions**

Name	Type	Description
SPI_0_SS0	Out	SPI slave select0. Can also be used as fabric I/O.
SPI_0_CLK	Out	SPI clock. Can also be used as fabric I/O.
SPI_0_SDO	Out	SPI data output. Can also be used as fabric I/O.
SPI_0_SDI	In	SPI data input. Can also be used as fabric I/O.

I/O Programmable Features

IGLOO2 devices support different I/O programmable features for MSIO, MSIOD, and DDRIO. Each I/O pair (P, N) supports the following programmable features:

- Programmable drive strength
- Programmable weak pull-up and pull-down
- Configurable ODT and driver impedance
- Programmable input delay
- Programmable Schmitt input and receiver

For more information on IGLOO2 I/O programmable features, refer to the "IGLOO2 I/O Features" table of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

Packaging Information

FC1152

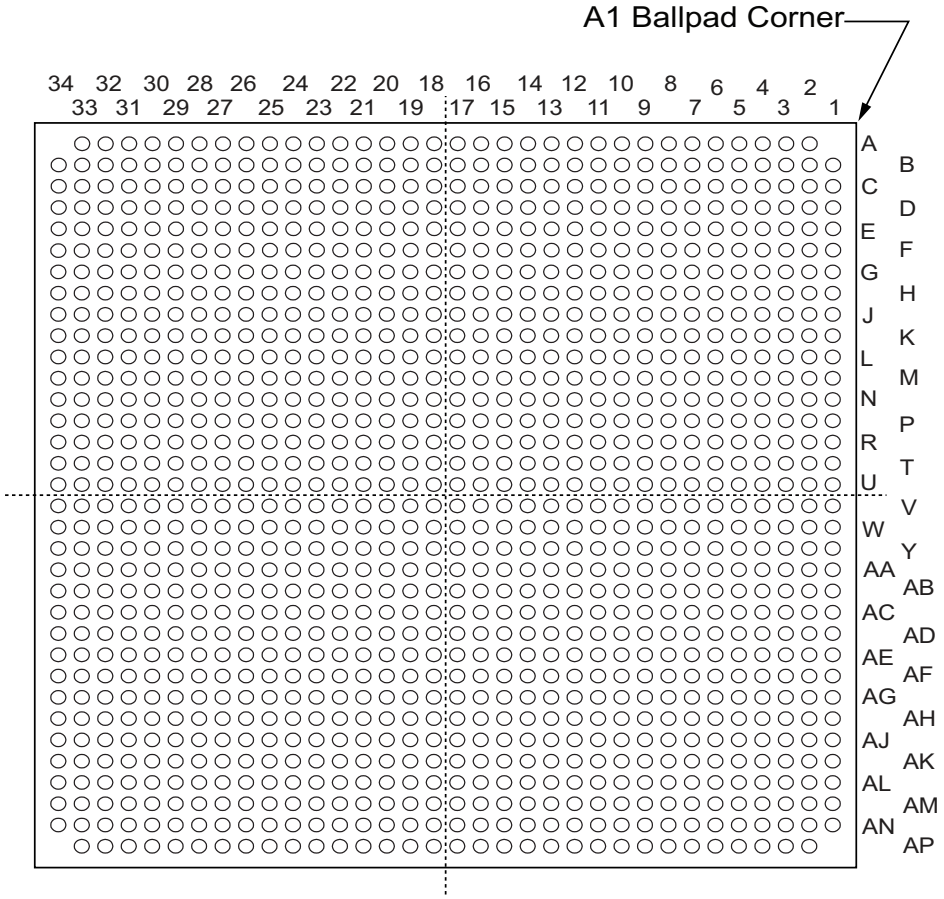


***Figure 28* • FC1152 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FC1152 package depicted in Figure 28 are found in the Excel® spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132144

The following devices are available in the FC1152:

M2GL150(T), (TS)

FG896

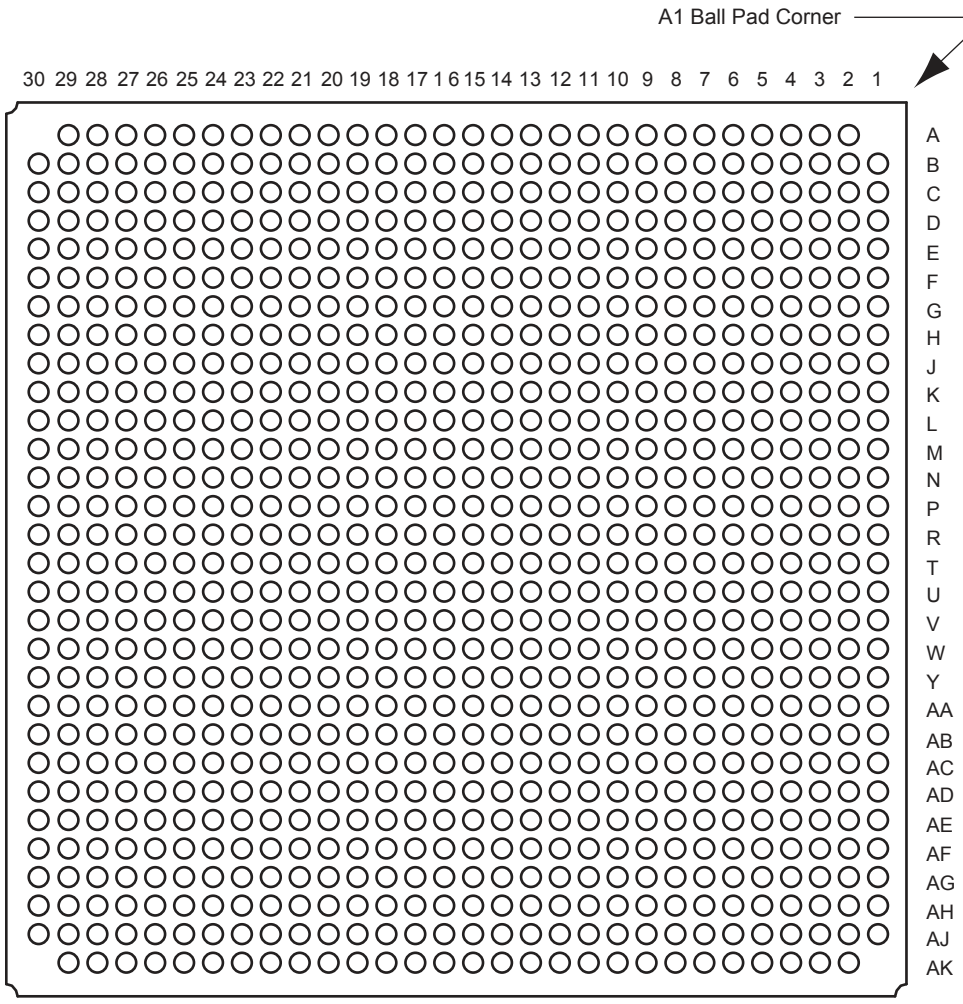


Figure 29 • **FG896 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FG896 package depicted in Figure 29 are found in the Excel spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132146

The following devices are available in the FG896:

M2GL050(T), (TS)

FG676

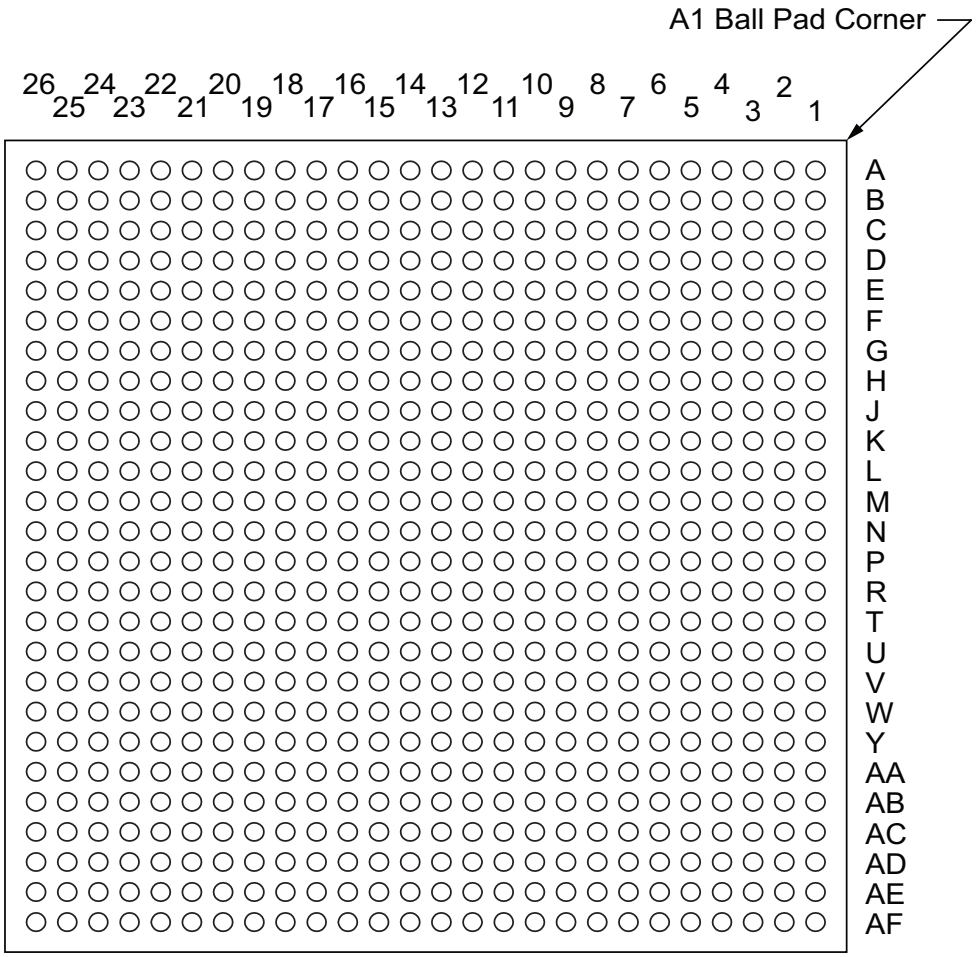


***Figure 30* • FG676 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FG676 package depicted in Figure 30 are found in the Excel® spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132534

The following devices are available in the FG676:

M2GL090(T), (TS)

M2GL060(T), (TS)

FCS536

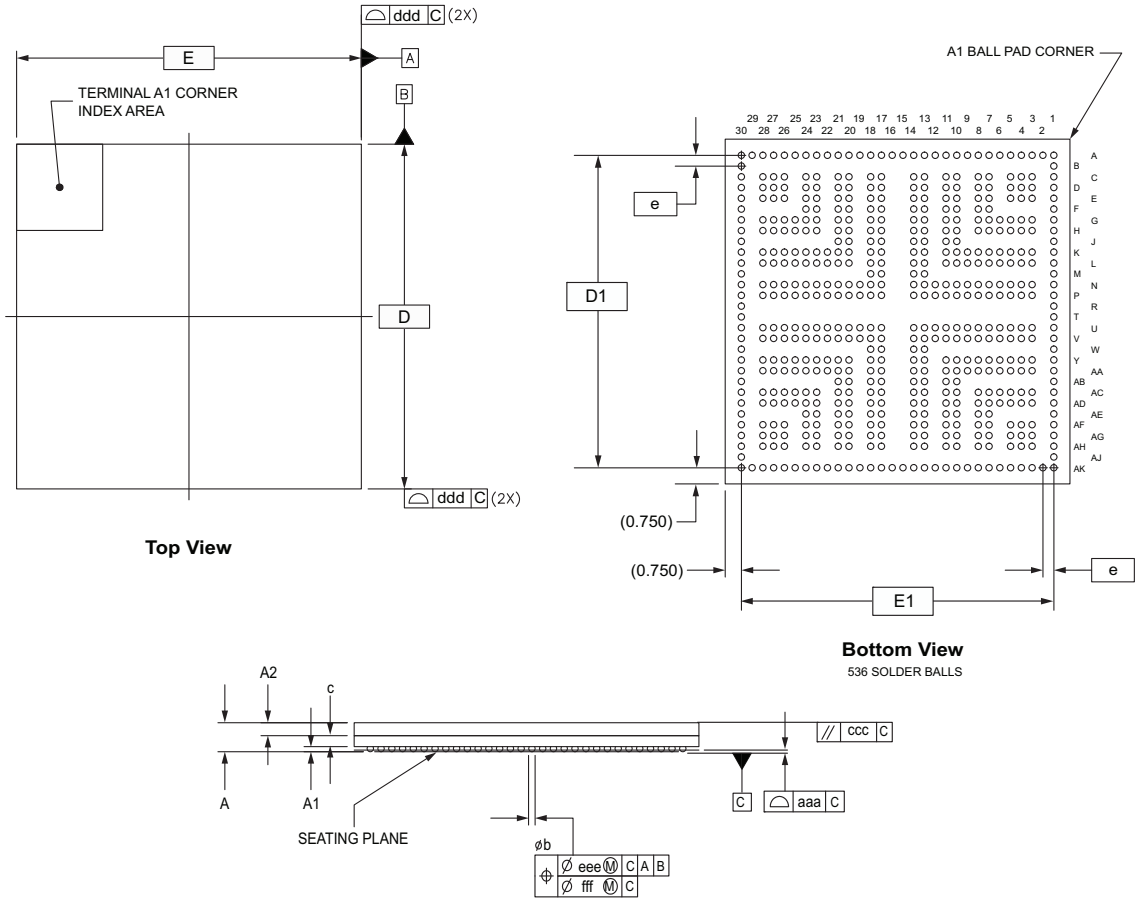


Figure 31 • **FCS536 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FCS536 package depicted in Figure 31 are found in the Excel® spreadsheet located here:

http://www.microsemi.com/document-portal/doc_download/134192-igloo2-fcs536-pinouts

The following devices are available in the FCS536:

M2GL150(T), (TS)

FCV484

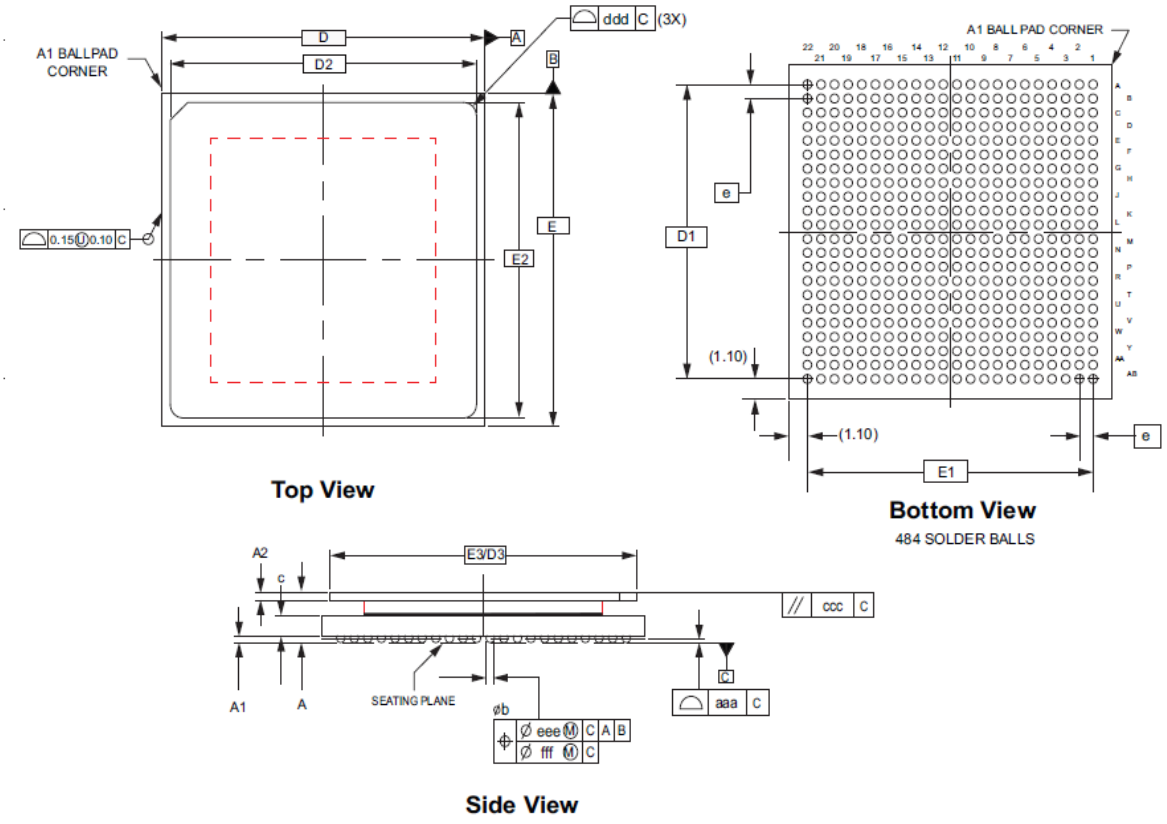


Figure 32 • **FCV484 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FCV484 package depicted in Figure 32 are found in the Excel® spreadsheet located here:

http://www.microsemi.com/document-portal/doc_download/134544-igloo2-fcv484-pinouts

The following devices are available in the FCV484:

M2GL150(T), (TS)

FG484

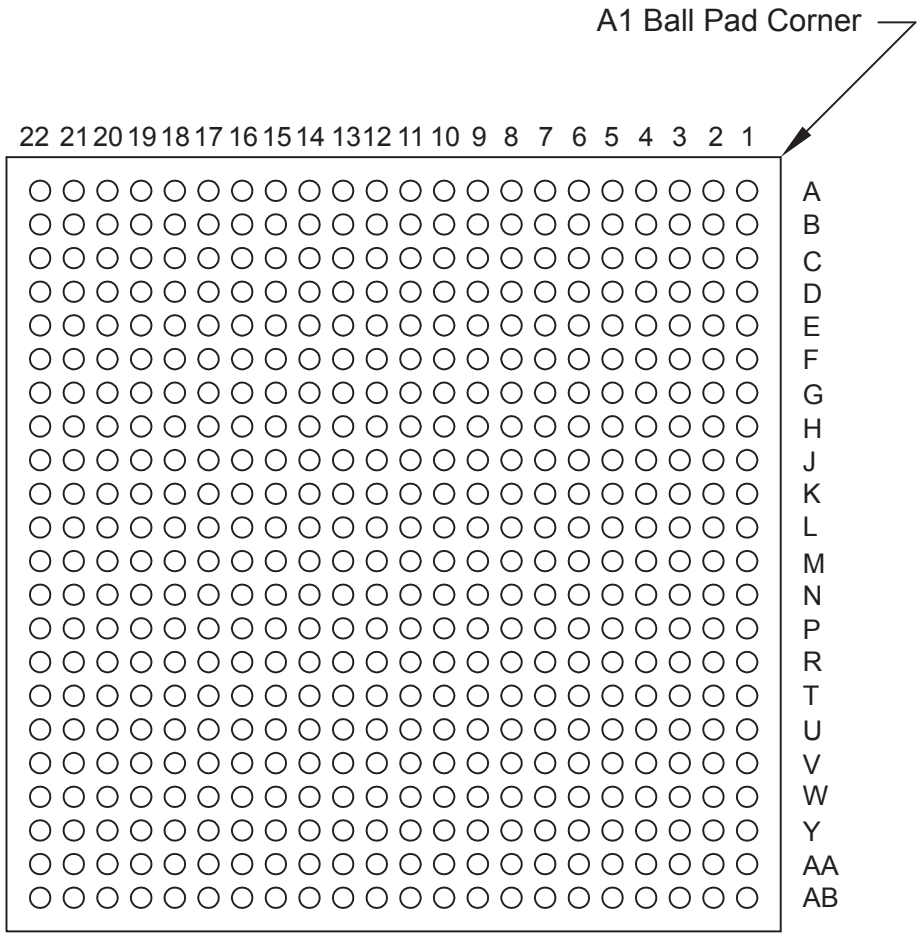


Figure 33 • **FG484 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FG484 package depicted in Figure 33 are found in the Excel® spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132145

The following devices are available in the FG484:

M2GL005(S)

M2GL010(T), (TS)

M2GL025(T), (TS)

M2GL050(T), (TS)

M2GL060(T), (TS)

M2GL090(T), (TS)

VF400

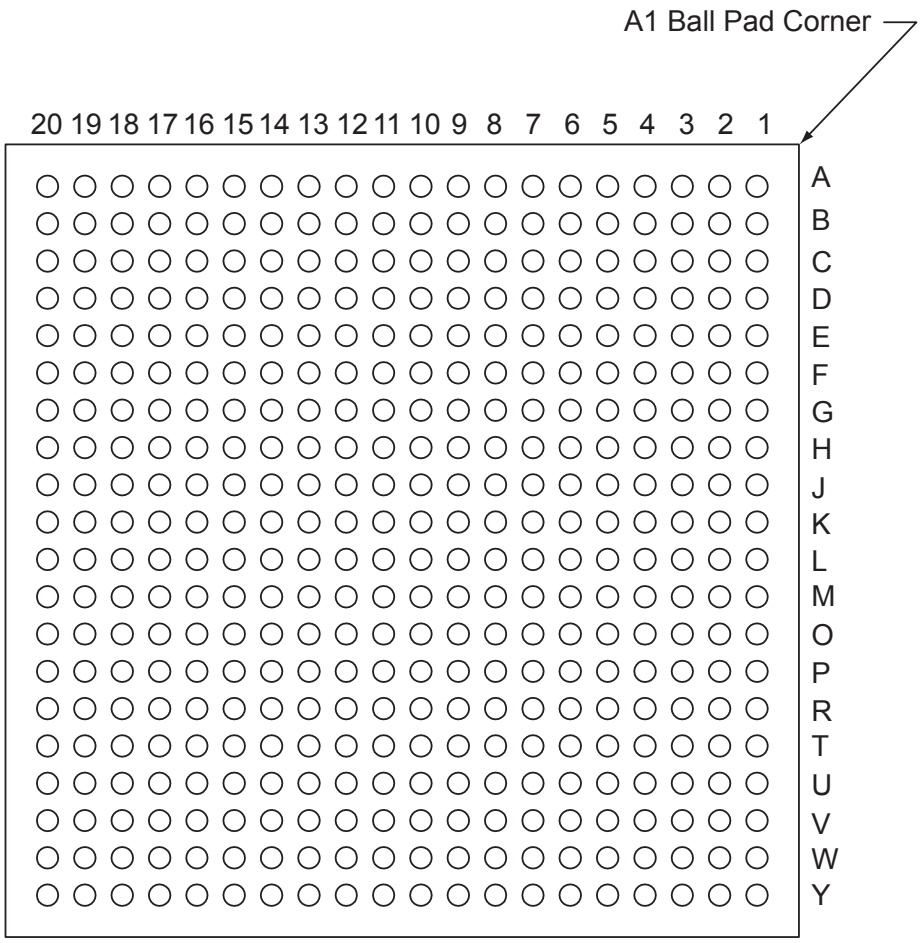


Figure 34 • **VF400 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at: *Packaging Resource Center*.

Pin Tables

Pin tables for the VF400 package depicted in Figure 34 are found in the Excel spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132147

The following devices are available in the VF400:

M2GL005(S)
M2GL010(T), (TS)
M2GL025(T), (TS)
M2GL050(T), (TS)
M2GL060(T), (TS)

FCS325

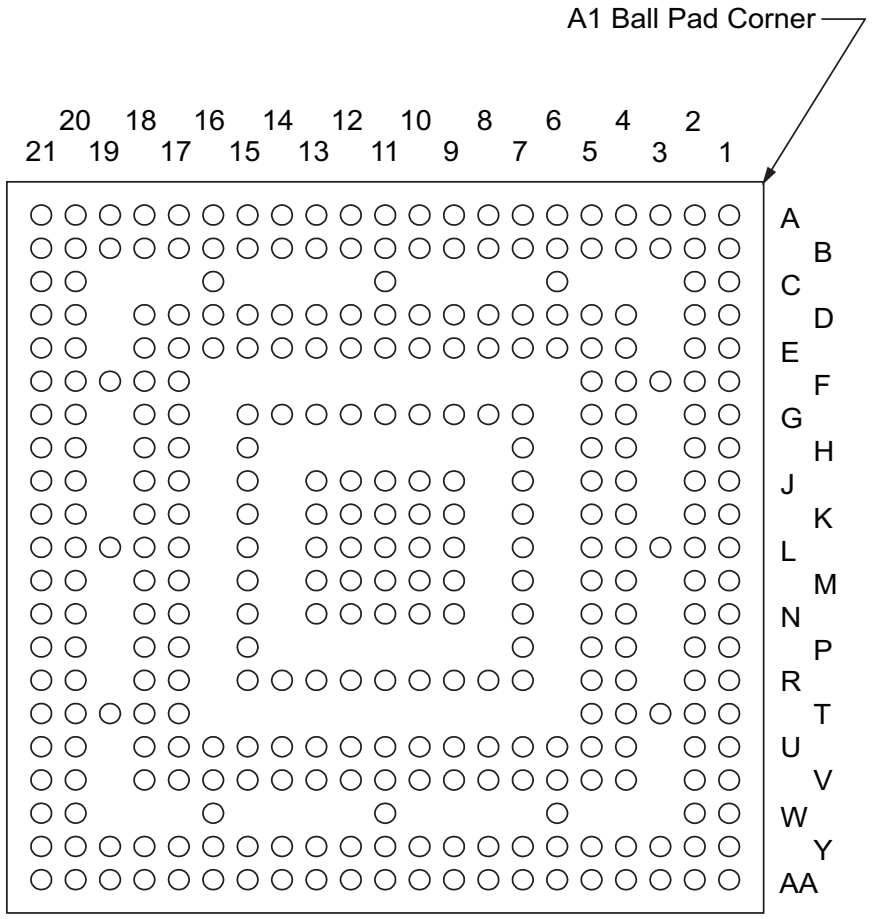


Figure 35 • **FCS325 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the FCS325 package depicted in Figure 35 are found in the Excel® spreadsheet located here:

http://www.microsemi.com/index.php?option=com_docman&task=doc_download&gid=132670

The following devices are available in the FCS325:

M2GL025(T), (TS)
M2GL050(T), (TS)
M2GL090(T), (TS)

VF256

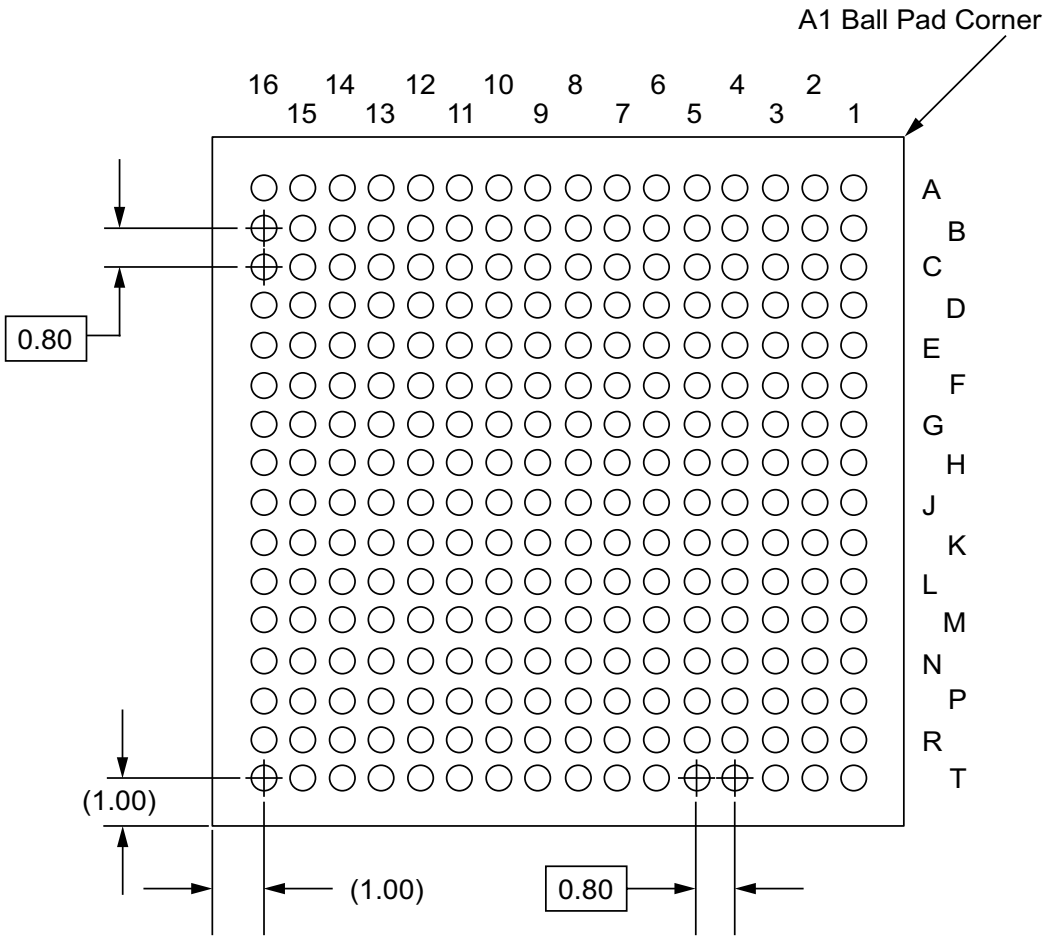


***Figure 36* • VF256 Package Drawing**

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the VF256 package depicted in Figure 36 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/document-portal/doc_download/133774-igloo2-vf256-pinouts*

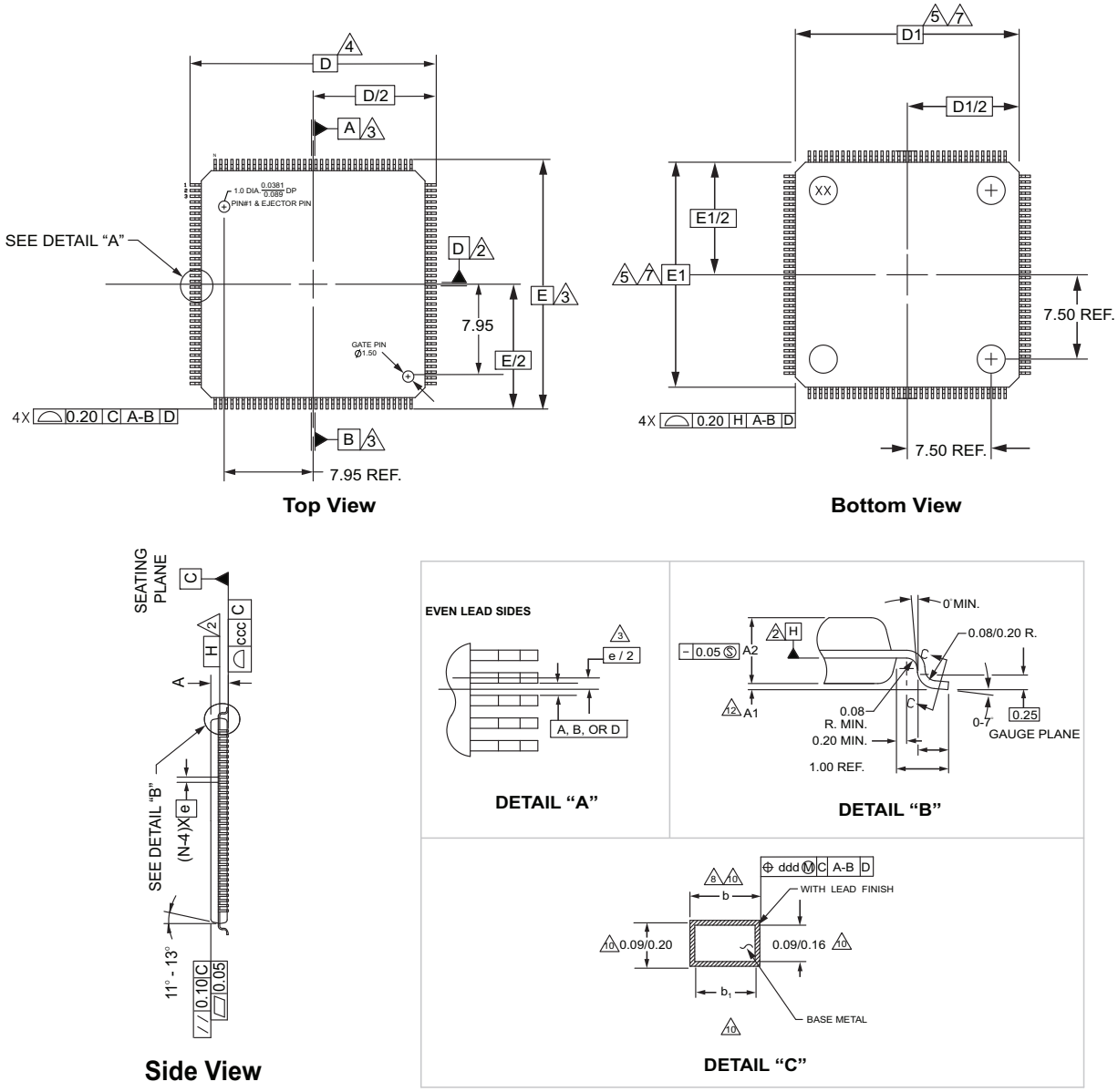
The following devices are available in the VF256:

M2GL005(S)

M2GL010(T), (TS)

M2GL025(T), (TS)

TQ144



NOTES: UNLESS OTHERWISE SPECIFIED

1. *All dimensioning and tolerances confirm to ASME Y14.5-1994.*
2. *Datum plane **H** located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.*
3. *Datums **A-B** and **D** to be determined at centerline between leads where leads exit plastic body at datum plane **H**.*
4. *To be determined at seating plane **C**.*
5. *Dimensions **D1** and **E1** do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimension **D1** and **E1** include mold mismatch and are determined at datum plane **H**.*
6. *N is number of terminals.*
7. *Package top dimensions are smaller than bottom dimensions by 0.10 millimeters and top of package will not overhang bottom of package.*
8. *Dimension **b** does not include damber protrusion. Allowable damber protrusion shall be not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Damber can not be located on the lower radius or the foot.*
9. *All dimensions are in millimeters.*
10. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
11. *This drawing conforms to JEDEC registered outline m2s-026-c, variation BFB.*
12. *A1 is defined as the distance from the seating plane to the lowest point of the package body.*

Figure 37 • **TQ144 Package Drawing**

Notes:

1. *All dimensioning and tolerances confirm to ASME Y14.5-1994.*
2. *Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.*

3. *Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.*
4. *To be determined at seating plane C.*
5. *Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimension D1 and E1 include mold mismatch and are determined at datum plane H.*
6. *N is number of terminals.*
7. *Package top dimensions are smaller than bottom dimensions by 0.10 millimeters and top of package will not overhang bottom of package.*
8. *Dimension b does not include damber protrusion. Allowable damber protrusion shall be not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Damber can not be located on the lower radius or the foot.*
9. *All dimensions are in millimeters.*
10. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
11. *This drawing conforms to JEDEC registered outline m2s-026-c, variation BFB.*
12. *A1 is defined as the distance from the seating plane to the lowest point of the package body.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at *Packaging Resource Center*.

Pin Tables

Pin tables for the TQ144 package depicted in Figure 37 are found in the Excel® spreadsheet located here: *http://www.microsemi.com/document-portal/doc_download/133135-igloo2-tq144-pinouts*

The following devices are available in the TQ144:

M2GL010
M2GL005 (S)

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 6 (January 2016	Added Figure 19 • IGLOO2 M2GL060TS/M2GL060T/M2GL060-FCS325 I/O Bank Locations (SAR 74266).	19
	Added "MDDR/FDDR Interface" section (SAR 69579).	32
Revision 5 (July 2015)	Added Figure 7 • IGLOO2 M2GL060TS/M2GL060T/M2GL060-FG484 I/O Bank Locations (SAR 67177).	7
	Updated Table 1 • Organization of I/O Banks in IGLOO2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484.	27
	Added Figure 27 • Internal Clamp Diode Control Circuitry.	30
	Updated Table 4 • Reference Resistors (SAR 67026).	32
	Updated "Supply Pins" section (SAR 65339).	34
	Updated "Programming SPI" section (SAR 66178).	38
	Updated Table 12 • Input Only Pins.	41
Revision 4 (February 2015)	Added new Figure 4 • IGLOO2 M2GL060TS/ M2GL060T/M2GL060-FG676 I/O Bank Locations (SAR 64505).	4
	Added new Figure 5 • IGLOO2 M2GL150TS/M2GL150T/M2GL150-FCS536 I/O Bank Locations (SAR 64505).	5
	Added new Figure 12 • IGLOO2 M2GL150TS/M2GL150T/M2GL150-FCV484 I/O Bank Locations (SAR 64505).	12
	Added new Figure 13 • IGLOO2 M2GL060TS/M2GL060T/M2GL060-VF400 I/O Bank Locations (SAR 64505).	13
	Remove all instances of and references to M2GL100 device (SAR 62858).	N/A
	Replaced VQ144 with TQ 144 from Table 2 • Organization of I/O Banks in IGLOO2 Devices - VF400, FCS325, VF256, and TQ144.	29
	Updated "Dedicated Global I/O Naming Conventions" section (SAR 63992).	31
	Updated Table 6	34
	Updated Table 11	40

Revision	Changes	Page
Revision 3 (June 2014)	Updated Notes for Bank Location figures (SAR 58571).	
	Added new Figure 23 • IGLOO2 M2GL010TS/M2GL010T/M2GL010-VF256 I/O Bank Locations, Figure 24 • IGLOO2 M2GL005S/M2GL005-VF256 I/O Bank Locations, and Figure 25 • IGLOO2 M2GL010-TQ144 I/O Bank Locations (SAR 58572).	23, 24, and 25
	Modified Figure 26 • IGLOO2 M2GL005S/M2GL005-TQ144 I/O Bank Locations (SAR 58572).	26
	Modified Table 1 • Organization of I/O Banks in IGLOO2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 by moving VF400 and FCS 325 devices to Table 2 • Organization of I/O Banks in IGLOO2 Devices - VF400, FCS325, VF256, and TQ144 (SAR 58572).	27
	Added VF256 and VQ144 devices to Table 2 • Organization of I/O Banks in IGLOO2 Devices - VF400, FCS325, VF256, and TQ144 (SAR 58572).	29
	Modified notes in Table 4 • Reference Resistors (SAR 58574).	32
	Modified notes in Table 6 • Supply Pins (SAR 58575).	34
	Modified Table 6 • Supply Pins by adding 'x' to supply pin names and deleting the individual pin names (SAR 58572).	34
	Added Table 12 • Input Only Pins (SAR 58576).	34
	Added Figure 36 • VF256 Package Drawing and Figure 37 • TQ144 Package Drawing (SAR 58572).	50 and 51
Revision 2 (March 2014)	Modified Notes for the following figures: Figure 1 • IGLOO2 M2GL150TS/M2GL150T/M2GL150-FC1152 I/O Bank Locations, Figure 2 • IGLOO2 M2GL100TS/M2GL100T-FC1152 I/O Bank Locations, and Figure 6 • IGLOO2 M2GL090TS/M2GL090T/M2GL090-FG484 I/O Bank Locations (SAR 55861).	1, 2, and 6
	Figure 18 • IGLOO2 M2GL090TS/M2GL090T/M2GL090-FCS325 I/O Bank Locations, Figure 22 • IGLOO2 M2GL025TS/M2GL025T/M2GL025-VF256 I/O Bank Locations, and Figure 26 • IGLOO2 M2GL005S/M2GL005-TQ144 I/O Bank Locations are new (SAR 55996).	18, 22, and 26
	Updated Table 1 • Organization of I/O Banks in IGLOO2 Devices - FC1152, FCS536, FCV484, FG896, FG676, and FG484 for I/O types (SARs 53411 and 55862).	27
	Note added for VPP and VPPNVM for 090, 100, and 150 devices in Table 6 • Supply Pins for I/O types (SAR 55857).	34
	Added descriptions for TMATCH pins to Table 11 • Special Pins (SAR 54079).	40

Revision	Changes	Page
Revision 1 (January 2014)	Table 3 • User I/O Types was corrected to change LVDS to LVDS2V5 (SAR 47753).	30
	Updated description column in Table 3 • User I/O Types (SAR 48665).	30
	Updated description column for VREF0 and VREF5 in Table 6 • Supply Pins (SAR 47164).	34
	Updated description column for FLASH_GOLDEN_N in Table 8 • Programming SPI Interface (SAR 52247).	38
	Updated description column in Table 9 • Device Reset and Crystal Oscillator Pin Types and Descriptions for DEVRST_N (SARs 50803, 52525).	38
	Updated the links (SAR 52236).	N/A
	Figure 1 • IGLOO2 M2GL150TS/M2GL150T/M2GL150-FC1152 I/O Bank Locations Figure 2 • IGLOO2 M2GL100TS/M2GL100T-FC1152 I/O Bank Locations Figure 3 • IGLOO2 M2GL090TS/M2GL090T/M2GL090-FG676 I/O Bank Locations Figure 11 • IGLOO2 M2GL005S/M2GL005-FG484 I/O Bank Locations Figure 17 • IGLOO2 M2GL005S/M2GL005-VF400 I/O Bank Locations Figure 20 • IGLOO2 M2GL050TS/M2GL050T/M2GL050-FCS325 I/O Bank Locations are new I/O Bank Location Figures for the FC1152, FG676, FG484, VF400, and FCS325 (SAR 52410).	1 2 3 11 17 20
	Figure 6 • IGLOO2 M2GL090TS/M2GL090T/M2GL090-FG484 I/O Bank Locations Figure 21 • IGLOO2 M2GL025TS/M2GL025T/M2GL025-FCS325 I/O Bank Locations are new I/O Bank Location Figures for the FG484 and FCS325 (SAR 52721).	6 – 20
	Figure 28 • FC1152 Package Drawing Figure 30 • FG676 Package Drawing Figure 35 • FCS325 Package Drawing are new package drawings for the FC1152, FG676 and FCS325 (SAR 52410).	42 44 49
Revision 0 (June 2013)	Initial Release	N/A

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