



# STW9N150

N-channel 1500 V - 1.8  $\Omega$  - 8 A - TO-247  
very high voltage PowerMESH™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STW9N150	1500 V	< 2.5 $\Omega$	8 A	320 W

- 100% avalanche tested
- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitances
- High speed switching
- Very low on-resistance

## Application

- Switching applications

## Description

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the company's proprietary edge termination structure, gives the lowest R<sub>DS(on)</sub> per area, unrivalled gate charge and switching characteristics.

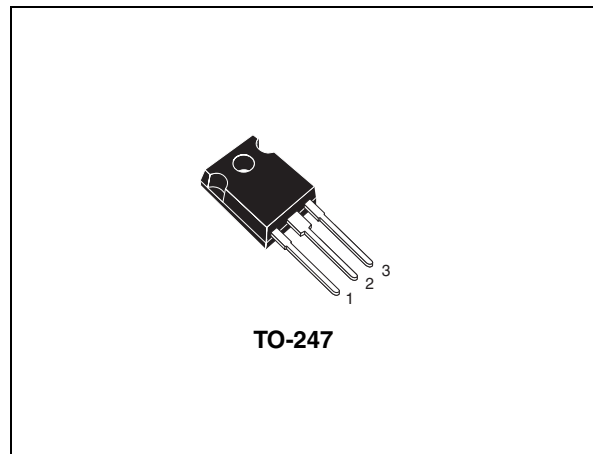


Figure 1. Internal schematic diagram

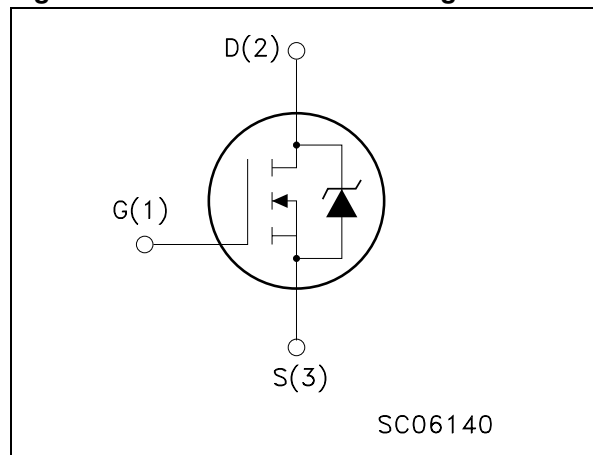


Table 1. Device summary

Order code	Marking	Package	Packaging
STW9N150	9N150	TO-247	Tube

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	1500	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	8	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	320	W
	Derating factor	2.56	W/ $^\circ\text{C}$
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.39	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$T_J$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	8	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	720	mJ

## 2 Electrical characteristics

(T<sub>case</sub> = 25°C unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	1500			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> = 125 °C			10 500	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 30 V			± 100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A		1.8	2.5	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4 A		7.5		S
C <sub>iss</sub> C <sub>OSS</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		3255 294 22.4		pF pF pF
C <sub>OSS eq.</sub>	Equivalent Output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 1200 V		118		pF
R <sub>g</sub>	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain		2.4		Ω
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 1200 V, I <sub>D</sub> = 8 A, V <sub>GS</sub> = 10 V (see Figure 15)		89.3 15.8 50.4		nC nC nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 750 \text{ V}$ , $I_D = 4 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 14)		41		ns
$t_r$	Rise time			14.7		ns
$t_{d(off)}$	Turn-off-delay time			86		ns
$t_f$	Fall time			52		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current				8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8 \text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 16)		988		ns
$Q_{rr}$	Reverse recovery charge			9.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			19.3		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 16)		884		ns
$Q_{rr}$	Reverse recovery charge			8.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			18.6		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

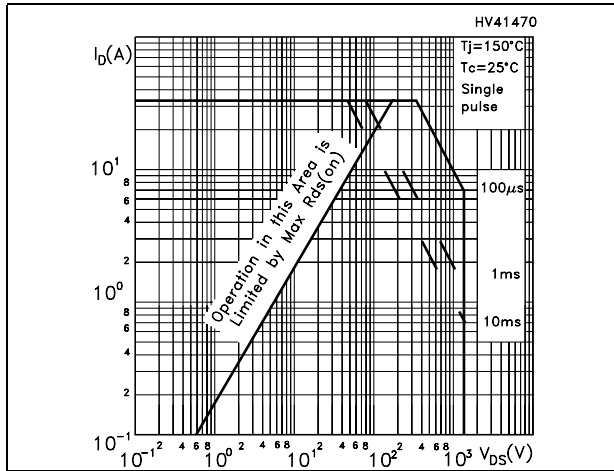


Figure 3. Thermal impedance

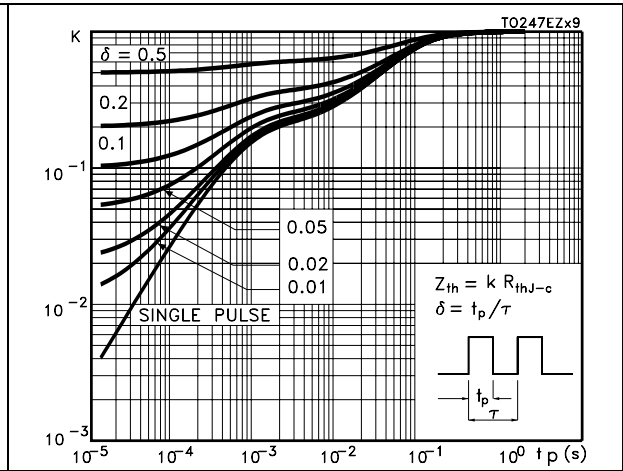


Figure 4. Output characteristics

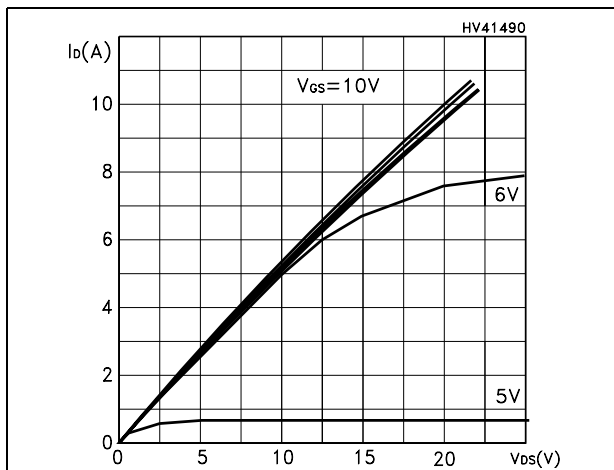


Figure 5. Transfer characteristics

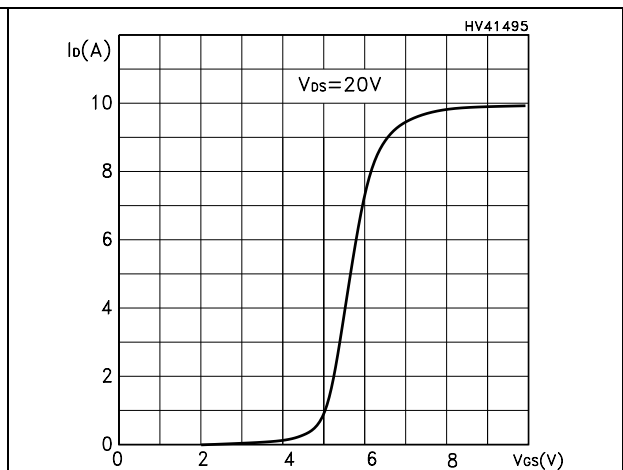


Figure 6. Normalized  $BV_{DSS}$  vs temperature

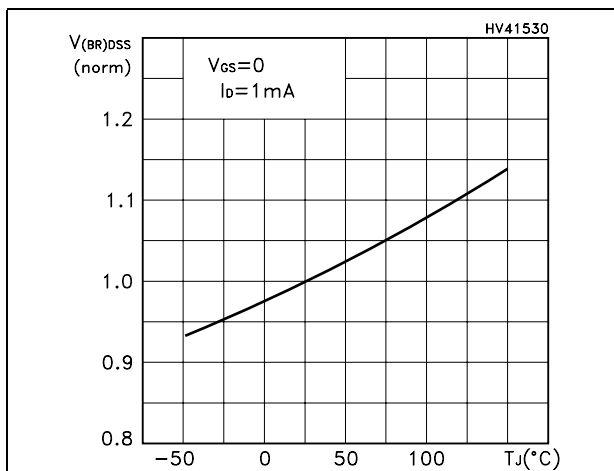


Figure 7. Static drain-source on resistance

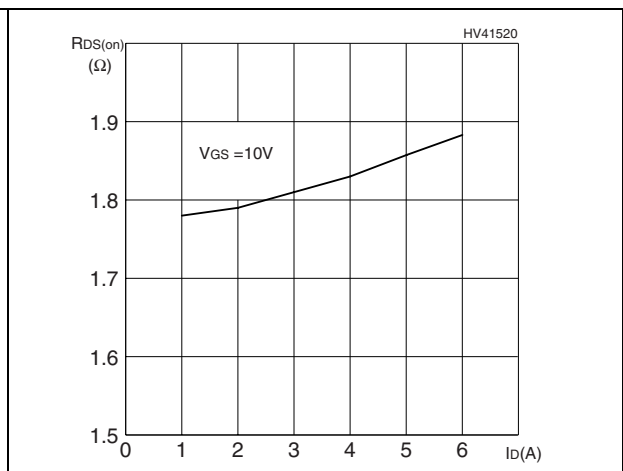


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

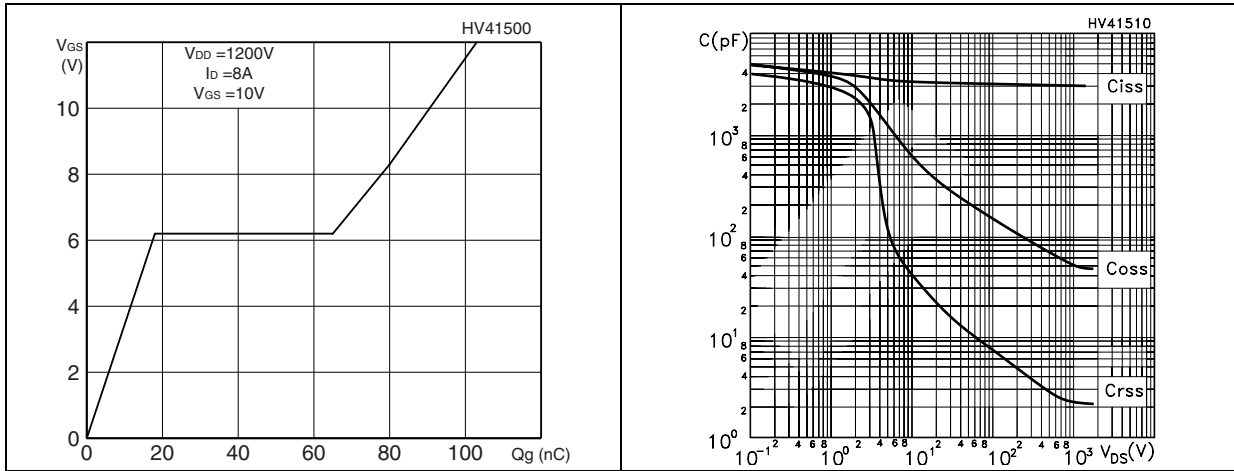


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

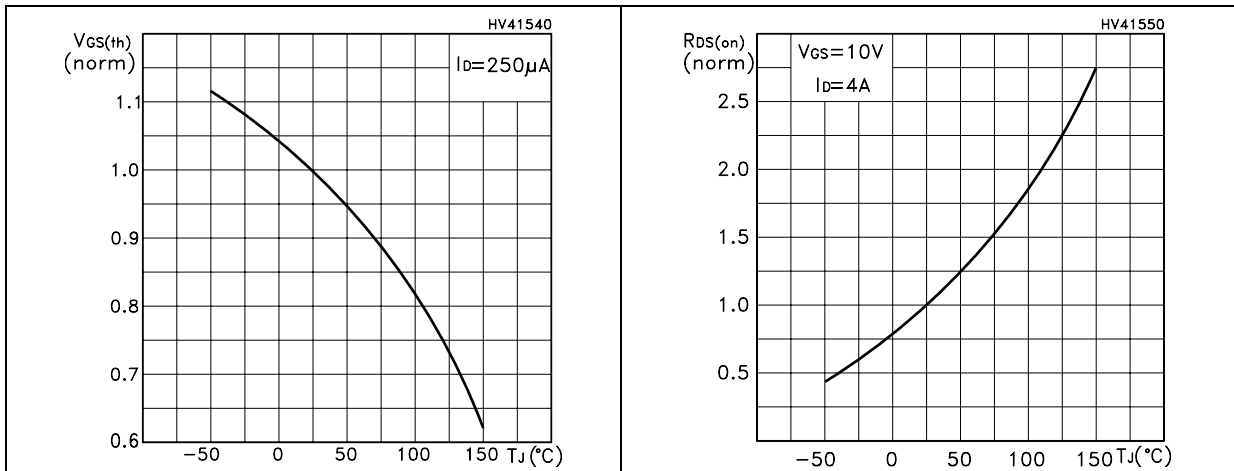
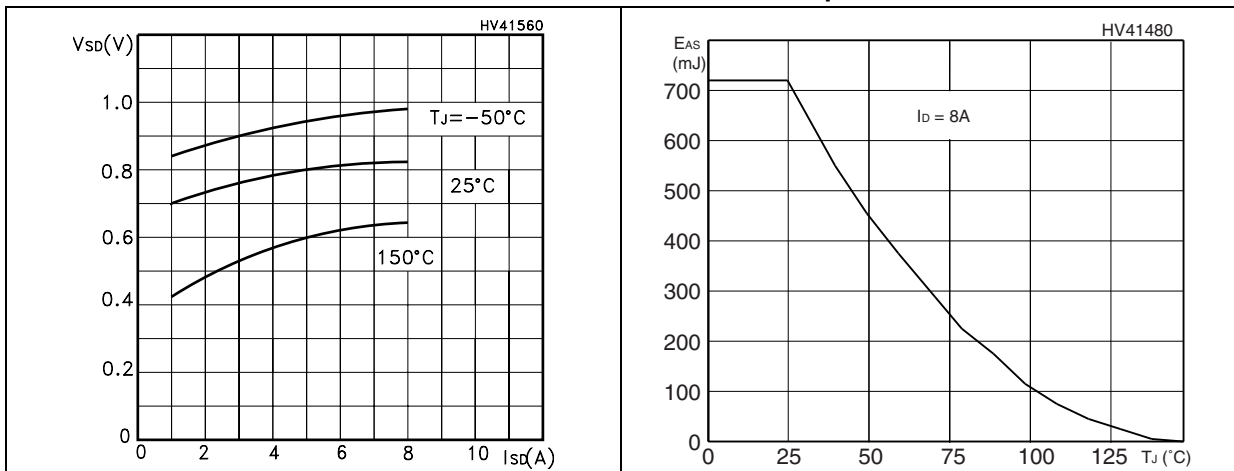
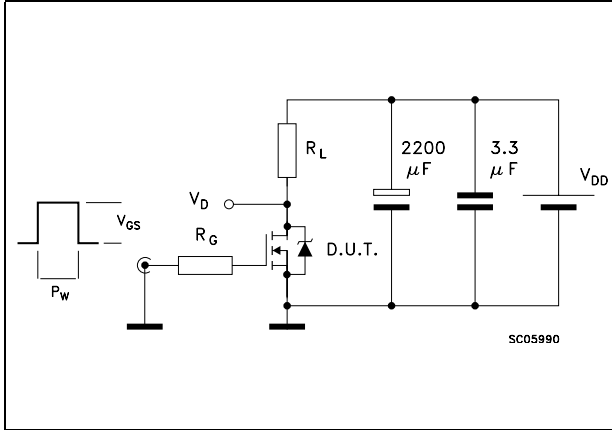


Figure 12. Source-drain diode forward characteristics Figure 13. Maximum avalanche energy vs temperature

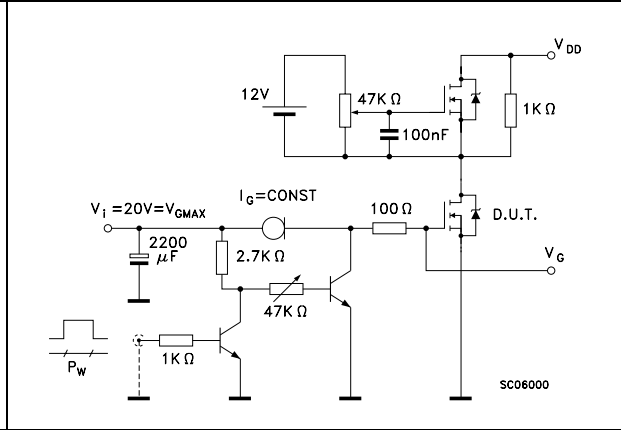


### 3 Test circuits

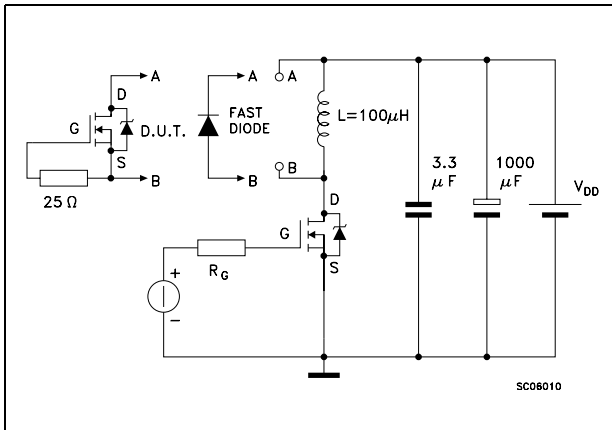
**Figure 14. Switching times test circuit for resistive load**



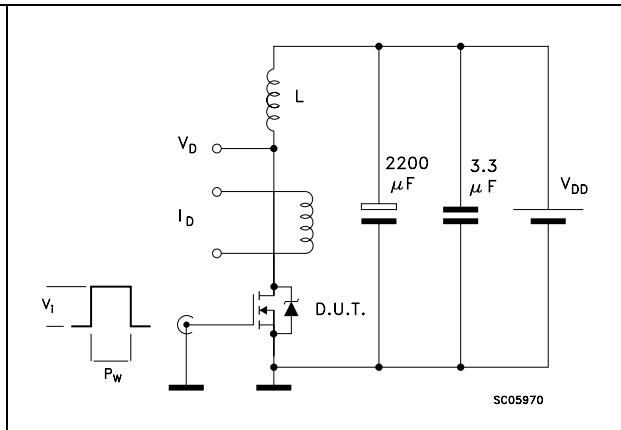
**Figure 15. Gate charge test circuit**



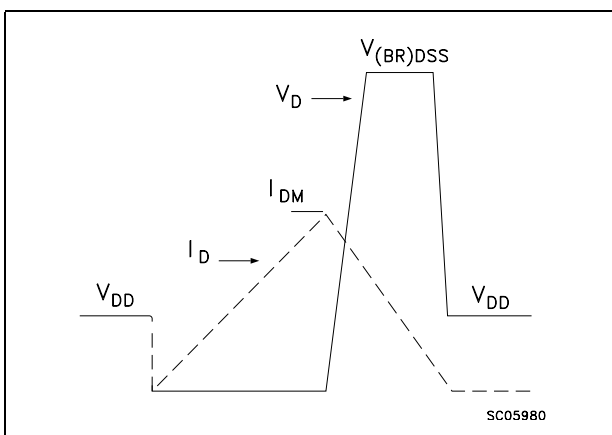
**Figure 16. Test circuit for inductive load switching and diode recovery times**



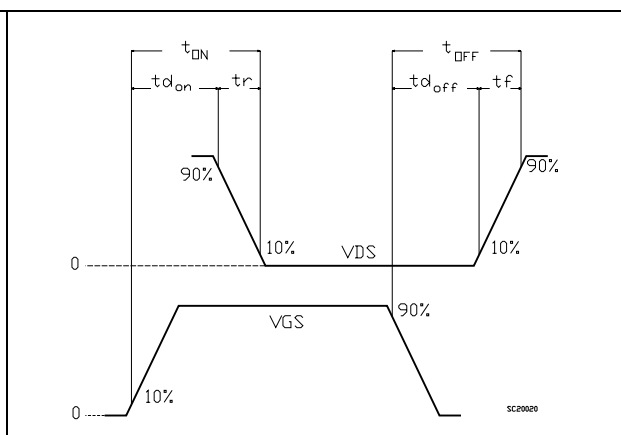
**Figure 17. Unclamped Inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**



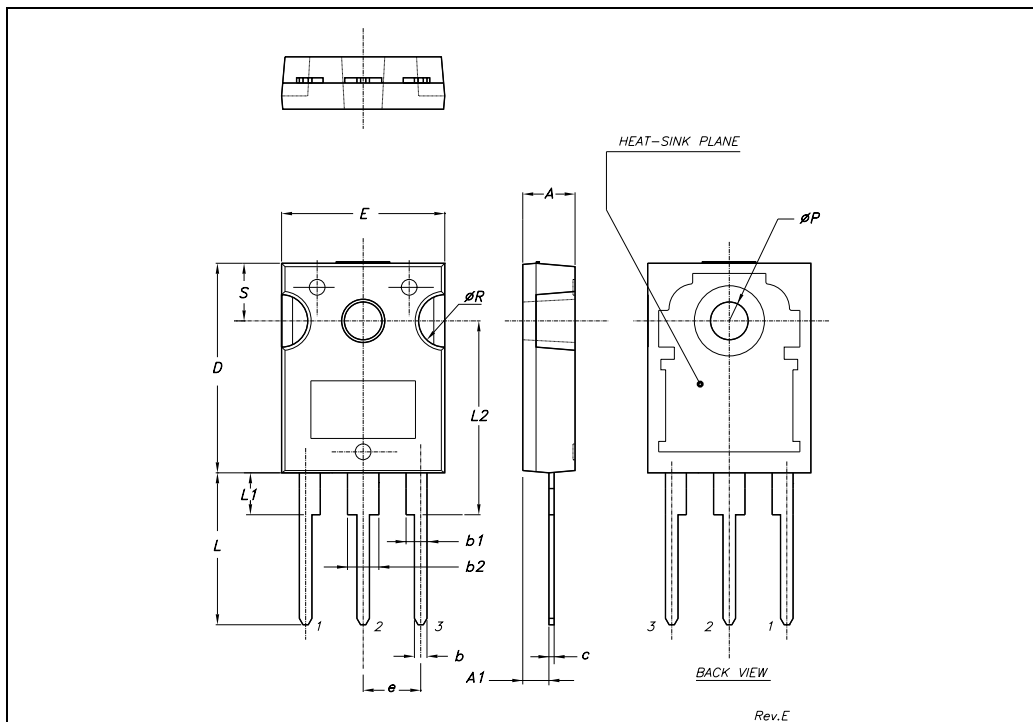


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
24-May-2007	1	First release
04-Jan-2007	2	Document status promoted from preliminary data to datasheet

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