DS8500 Evaluation Kit

Evaluates: DS8500

General Description

The DS8500 evaluation kit (EV kit) provides a convenient and a quick platform to evaluate the DS8500 HART modem. The EV kit is specifically kept generic to allow the user to evaluate DS8500 in both slave and master designs.

EV Kit Contents

- **DS8500 EV Kit Board**

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C4	3	1.0µF, 10V capacitors
C3	1	2.2nF, 10V C0G capacitors
C5, C6, C10, C11	4	100nF capacitors
C7, C8	0	Not installed, capacitors
C9	1	10nF, 10V C0G capacitors
C12	1	4.7µF, 10V capacitor
C13, C14	2	27pF, 10V C0G capacitors
C15	1	10µF, 6.3V capacitor
P1	1	8-pin port
P2	1	5-pin port
R1	1	1.58kΩ ±1% resistor
R2, R4	2	301kΩ ±1% resistors
R3	1	1.0Ω resistor
TP1, TP2	2	Test points
U1	1	HART modem with FSK modulation demodulation (20 TQFN-EP*) Maxim DS8500-JND+
U2	1	Micropower rail-to-rail I/O op amp (5 SOT23) Maxim MAX4040EUK
Y1	1	3.6864MHz crystal
—	1	PCB: DS8500 EV KIT

**EP = Exposed pad.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Features

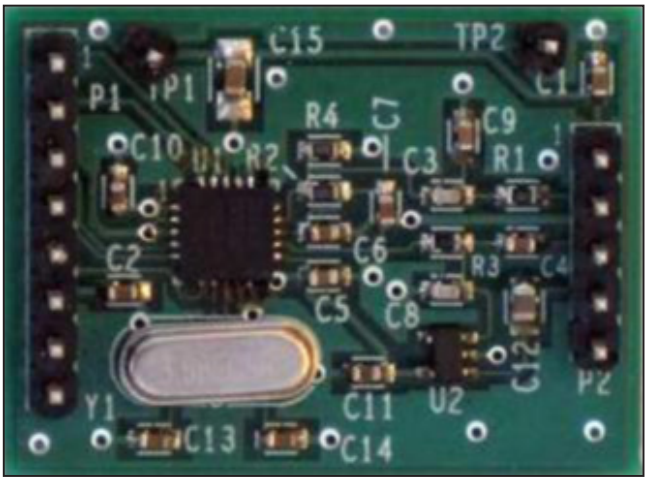
- **On-Board 3.6864MHz Crystal**
- **HART Receive Filters**
- **Small PCB Footprint**

Ordering Information

PART	TYPE
DS8500-KIT#	EV Kit

#Denotes a RoHS-compliant device that may include lead(Pb) that is exempt under the RoHS requirements.

DS8500 EV Kit Board



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5641; Rev 0; 11/10

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_Detailed Description of Hardware

This document must be used in conjunction with the following documents:

- DS8500 IC Data Sheet
- DS8500 EV Kit Data Sheet (this document)
- Application Note 4676: *Introduction to the DS8500 HART Modem*

The DS8500 evaluation kit (EV kit) contains all the necessary receive and transmit filters that are required for HART communication to a 4-20mA current loop in a process control application. The EV board is prepopulated with all the passives and the crystal required for proper operation. Port pins provide easy monitoring of the signals associated with the device.

Power Supply: A typical 3.3V power supply needs to be connected to V33 to power-up the IC along with the board.

Clock Source: The 3.6864MHz crystal provides the clock source to the DS8500 IC.

Receive Filters: The resistors and capacitors are populated on the board to separate the HART signal (FSK_IN) from the noise of the 4-20mA current loop. For the receive side a simple lowpass (10.1kHz) and a highpass (481Hz) filter is sufficient to separate the HART signal. These filters are realized by the following components:

- LoPass: 10.1kHz (R1, C3)
- HiPass: 481Hz (R2, R4, C7)

DC Bias Voltage: The resistor-divider formed by R2 and R4 provides a DC bias voltage of $V_{REF}/2$ for the incoming FSK_IN receive signal.

Port Pins P1, P2: The port pins P1 (controller interface) and P2 (HART interface) provide access to device.

Table 1. Port Pin Description

PORT PIN #	PIN NAME	PIN TYPE	DESCRIPTION
P1.1	HRXD	Output	Digital data output from DS8500 (DOUT)
P1.2	HTXD	Input	Digital data input to DS8500(DIN)
P1.3	RST_N	Input	Active-low reset signal to DS8500
P1.4	HOCD	Output	Carrier-detect output from DS8500
P1.5	HRTS	Input	Request-to-send signal to DS8500
P1.6	V33	Power	3.3V power supply
P1.7, P1.8	GND	Power	Ground
P2.1	V33	Power	3.3V power supply
P2.2	FSKIN	Input	HART input from 4-20mA current loop
P2.3	FSKOUT	Output	HART output from DS8500
P2.4	OUT_B	Output	HART output by a unity gain amplifier, U2 (MAX4040EUK)
P2.5	GND	Power	Ground

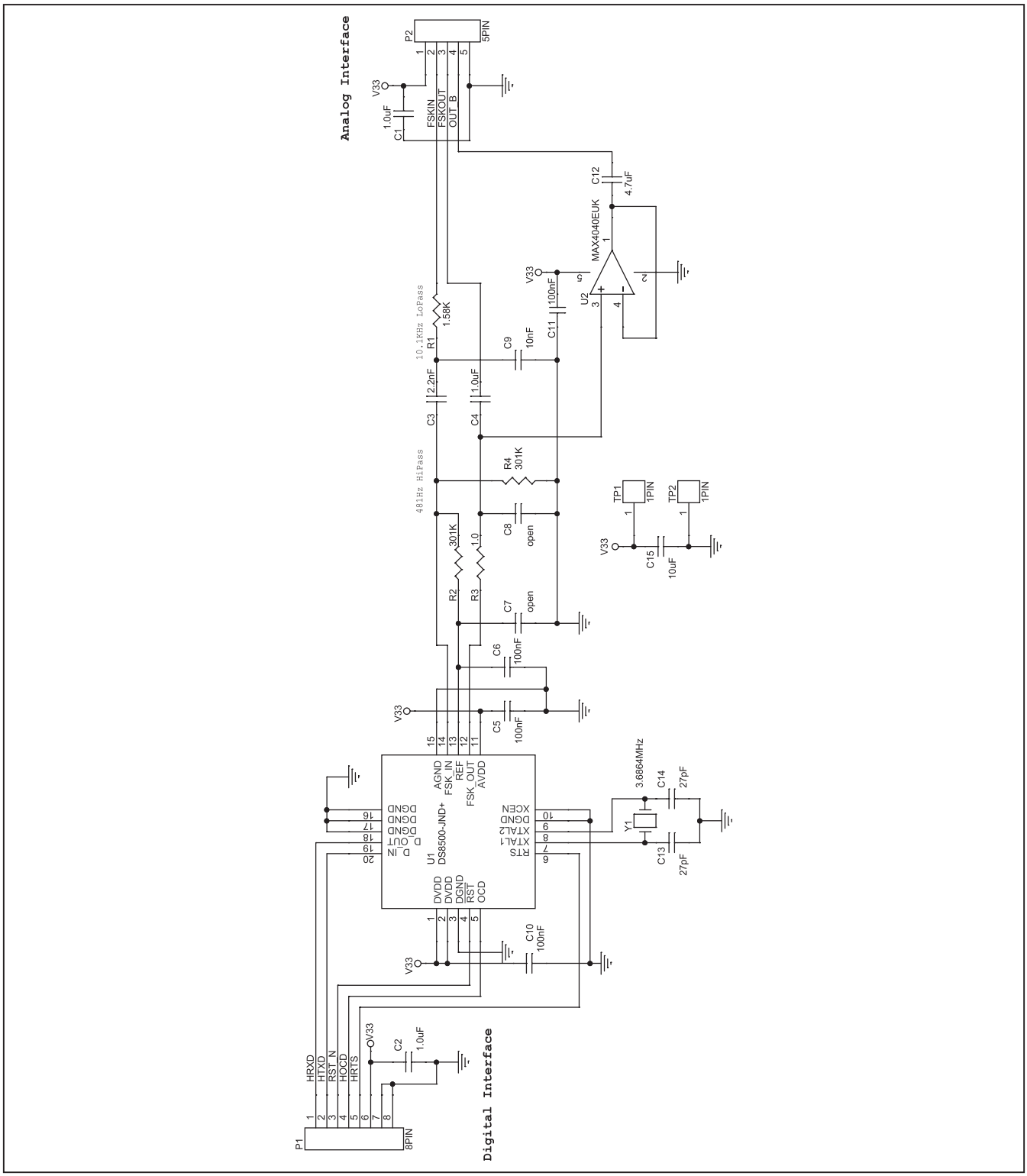

Figure 1. DS85000 EV Kit Schematic

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/10	Initial release	—