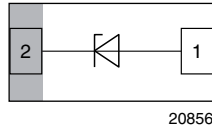
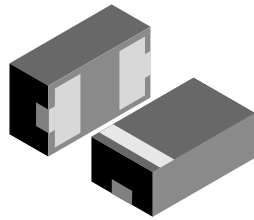


### ESD-Protection Diode in LLP1006-2L



20856



20855

#### MARKING (example only)



Bar = cathode marking  
 X = date code  
 Y = type code (see table below)

#### FEATURES

- Ultra compact LLP1006-2L package
- Low package height < 0.4 mm
- 1-line ESD-protection
- Low leakage current < 0.01  $\mu$ A
- Low load capacitance  $C_D = 12.5$  pF ( $V_R = 6$  V;  $f = 1$  MHz)
- ESD-protection acc. IEC 61000-4-2  $\pm 30$  kV contact discharge  
 $\pm 30$  kV air discharge
- High surge current acc. IEC61000-4-5  $I_{PP} > 4$  A
- Soldering can be checked by standard vision inspection. No X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VESD12A1C-HD1	VESD12A1C-HD1-GS08	8000	8000

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VESD12A1C-HD1	LLP1006-2L	G	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VESD12A1C-HD1					
PARAMETER	TEST CONDITIONS		SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5; $t_p = 8/20$ $\mu$ s; single shot		$I_{PPM}$	4	A
Peak pulse power	Acc. IEC 61000-4-5; $t_p = 8/20$ $\mu$ s; single shot		$P_{PP}$	92	W
ESD immunity	Contact discharge, acc. IEC61000-4-2; 10 pulses		$V_{ESD}$	$\pm 30$	kV
	Air discharge, acc. IEC61000-4-2; 10 pulses		$V_{ESD}$	$\pm 30$	kV
Operating temperature	Junction temperature		$T_J$	-40 to +125	°C
Storage temperature			$T_{STG}$	-55 to +150	°C

PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and International patents.

## BiAs-MODE (Bidirectional asymmetrical protection mode)

With the VESD12A1C-HD1 one signal- or data-lines (L1) can be protected against voltage transients. With pin 1 connected to ground and pin 2 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage ( $V_{RWM}$ ) the protection diode between data line and ground offers a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage ( $V_C$ ) is defined by the breakthrough voltage ( $V_{BR}$ ) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage ( $V_F$ ) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the VESD12A1C-HD1 clamping behavior is bidirectional and asymmetrical (BiAs).



<b>ELECTRICAL CHARACTERISTICS VESD12A1C-HD1</b> BiAs mode (between pin 1 and pin 2)						
$(T_{amb} = 25\text{ }^{\circ}\text{C, unless otherwise specified})$						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	12	V
Reverse voltage	at $I_R = 0.1\text{ }\mu\text{A}$	$V_R$	12	-	-	V
Reverse current	at $V_{RWM} = 12\text{ V}$	$I_R$	-	< 0.01	0.1	$\mu\text{A}$
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	$V_{BR}$	13.5	14	16	V
Reverse clamping voltage	at $I_{PP} = 1\text{ A}$	$V_C$	-	15.8	17	V
	at $I_{PP} = I_{PPM} = 4\text{ A}$	$V_C$	-	20	23	V
Forward clamping voltage	at $I_{PP} = 0.2\text{ A}$	$V_F$		0.9	1.2	V
	at $I_{PP} = 1\text{ A}$	$V_F$		1.1	1.5	V
	at $I_{PP} = I_{PPM} = 4\text{ A}$	$V_F$		1.7	2.1	V
Capacitance	at $V_R = 0\text{ V; } f = 1\text{ MHz}$	$C_D$	-	30	36	pF
	at $V_R = 6\text{ V; } f = 1\text{ MHz}$	$C_D$	-	12.5	-	pF

**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

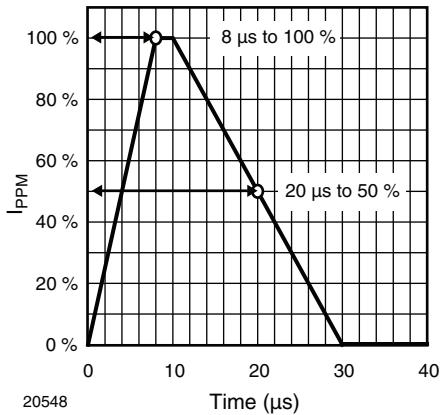


Fig. 1 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form (acc. IEC 61000-4-5)

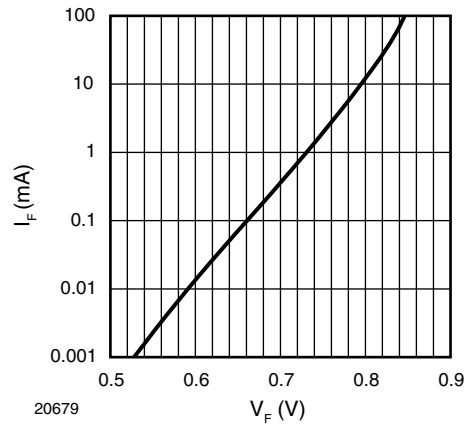


Fig. 4 - Typical Forward Current  $I_F$  vs. Forward Voltage  $V_F$

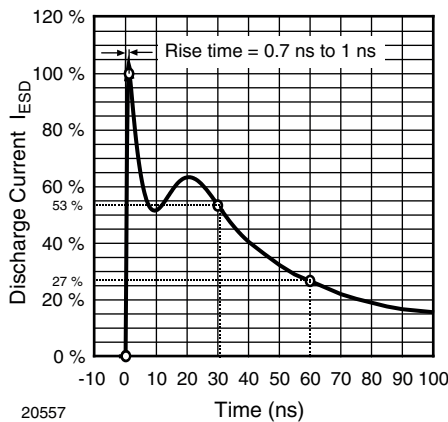


Fig. 2 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

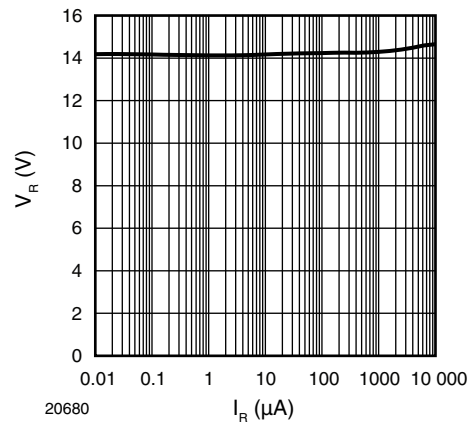


Fig. 5 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

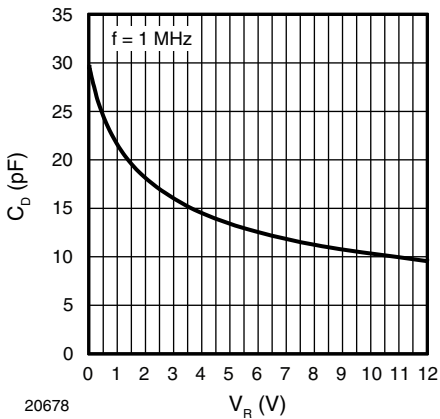


Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$

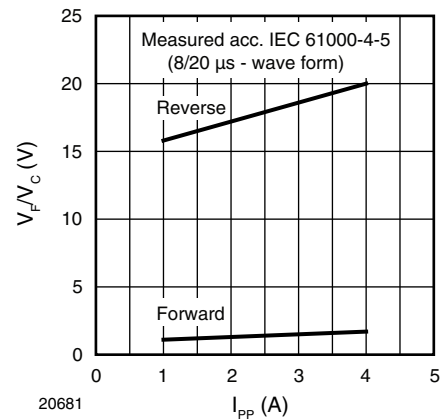


Fig. 6 - Typical Clamping Voltage vs. Peak Pulse Current  $I_{PP}$

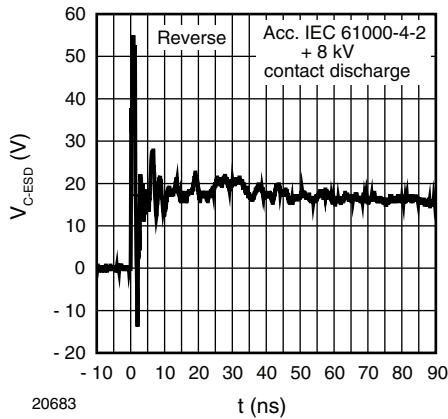


Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

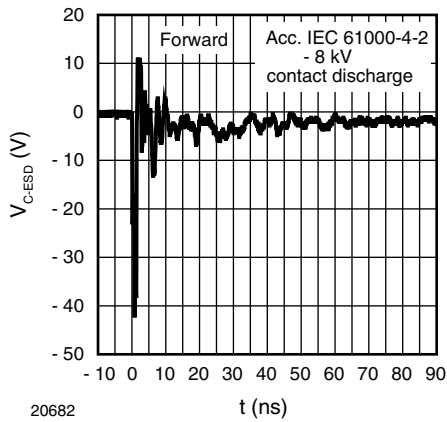


Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

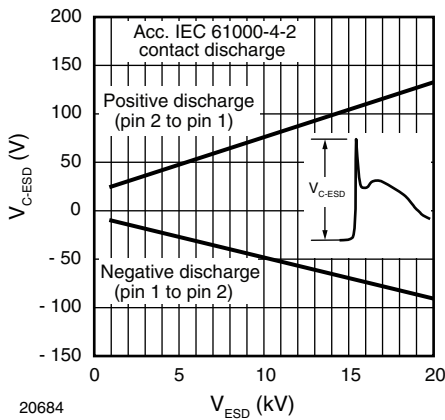
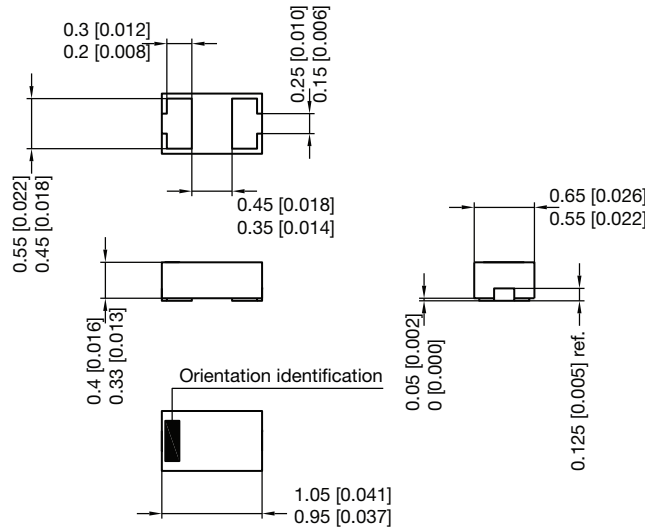


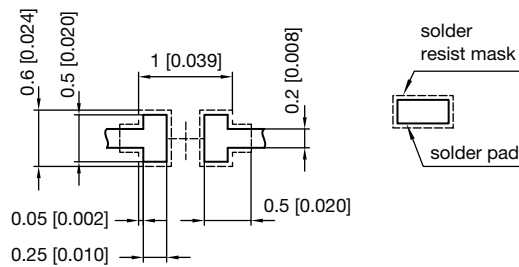
Fig. 9 - Typical Clamping Voltage at ± ESD Contact Discharge  
Fig. 10 - (acc. IEC 61000-4-2)



**PACKAGE DIMENSIONS** in millimeters (inches): **LLP1006-2L**

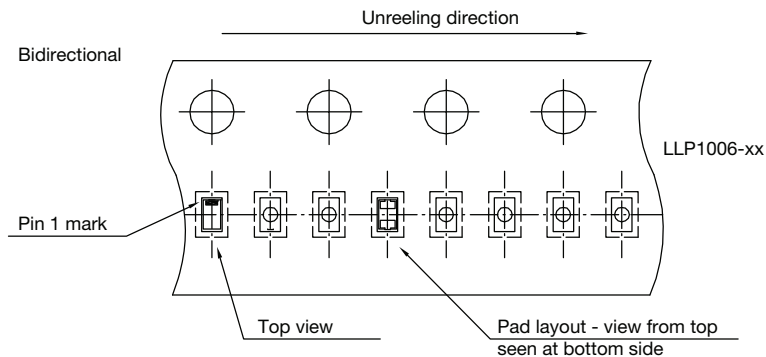


Foot print recommendation:



Pad Design Patented:  
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Document no.: S8-V-3906.04-005 (4)  
Rev. 7 - Date: 11.May 2016  
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