

## +1.8V, Low Power, 16-Bit Sigma-Delta A/D Converter

### Features

- 16-bit Resolution at Eight Conversions Per Second, Adjustable Down to 10-bit Resolution at 512 Conversions Per Second
- 1.8V – 5.5V Operation, Low Power Operating 260 $\mu$ A; Sleep: 0.75 $\mu$ A
- microPort™ Serial Bus Requires only two Interface Lines
- Uses Internal or External Reference
- Automatically Enters Sleep Mode when not in use

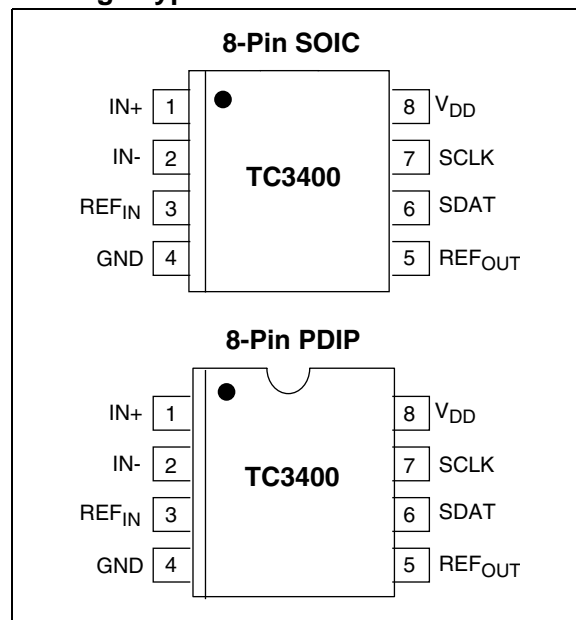
### Applications

- Consumer Electronics, Thermostats, CO Monitors, Humidity Meters, Security Sensors
- Embedded Systems, Data Loggers, Portable Equipment
- Medical Instruments

### Device Selection Table

Part Number	Package	Temperature Range
TC3400VPA	8-Pin PDIP (Narrow)	0°C to +85°C
TC3400VOA	8-Pin SOIC (Narrow)	0°C to +85°C

### Package Type



### General Description

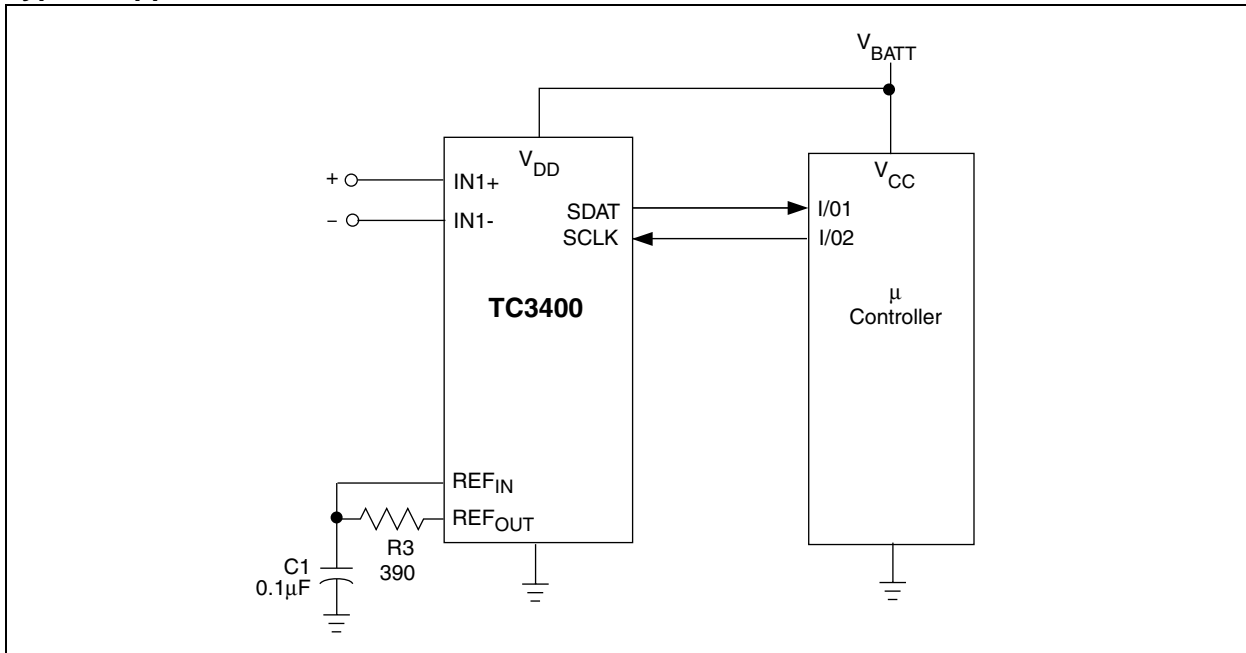
The TC3400 is a low cost, low power analog-to-digital converter based on Microchip's Sigma-Delta technology. It will perform 16-bit conversions (15-bit plus sign) at up to eight per second. The TC3400 is optimized for use as a microcontroller peripheral in low cost, battery operated systems. A voltage reference is included, or an external reference can be used.

The TC3400's 2-wire microPort™ digital interface is used for starting conversions and for reading out the data. Driving the SCLK line low starts a conversion. After the conversion starts, each additional falling edge (up to six) detected on SCLK for  $t_4$  seconds reduces the A/D resolution by one bit and cuts conversion time in half. After a conversion is completed, clocking the SCLK line puts the MSB through LSB of the resulting data word onto the SDAT line, much like a shift register. The part automatically sleeps when not performing a data conversion.

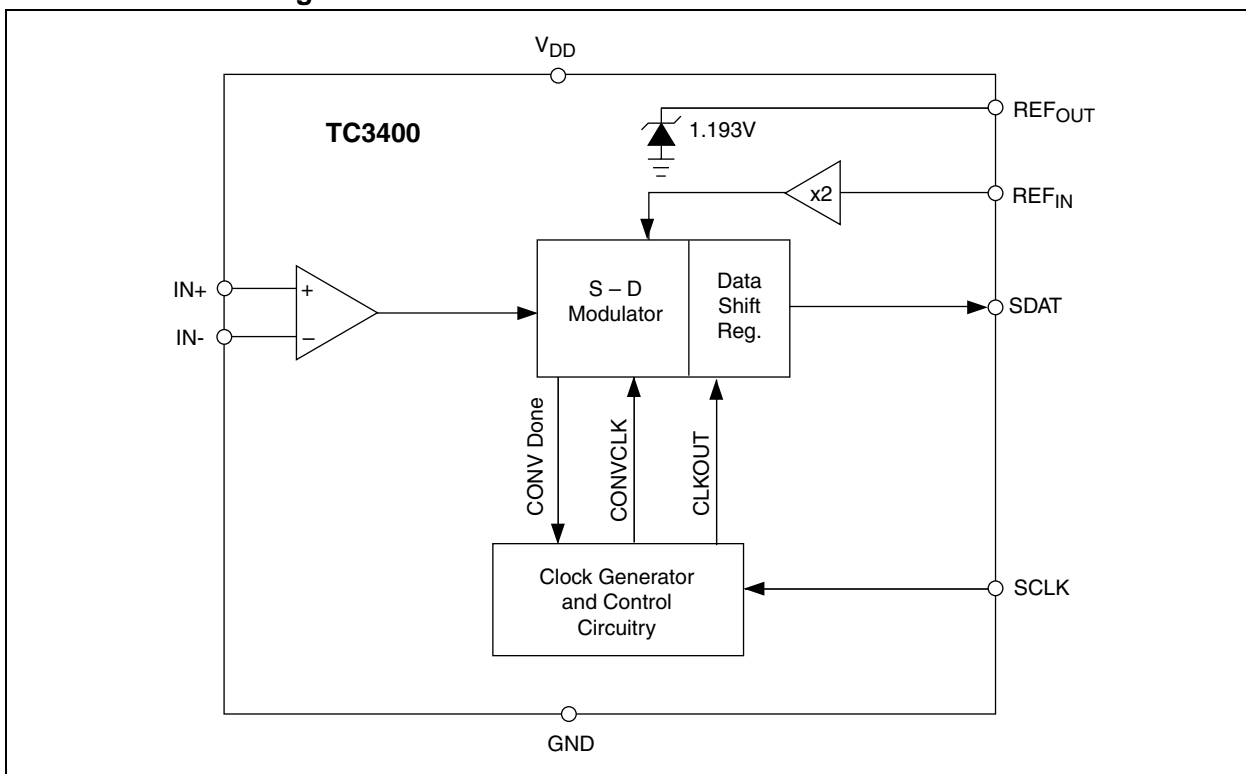
The TC3400 is available in a 8-Pin PDIP and a 8-Pin SOIC package.

# TC3400

## Typical Application



## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings\*

Supply Voltage .....	6.0V
Input Voltage (All Other Pins):	
..... (GND – 0.3V) to (V <sub>DD</sub> + 0.3V)	
Operating Temperature Range .....	0°C to 85°C
Storage Temperature .....	-65°C to +150°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### TC3400 DC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** T<sub>A</sub> = 25°C and V<sub>DD</sub> = 2.7V, unless otherwise specified. **Boldface** type specifications apply for temperatures of 0°C to 85°C. V<sub>REF</sub> = 1.25V, Internal Clock Frequency = 520kHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Power Supply</b>						
V <sub>DD</sub>	Supply Voltage	1.8	—	5.5	V	
I <sub>DD</sub>	Supply Current, During Data Conversion	—	260	—	μA	
I <sub>DD</sub> SLEEP	Supply Current, Sleep Mode	—	0.75	1.5	μA	T <sub>A</sub> = +25°C
		—	<b>1.2</b>	<b>3.0</b>	μA	
<b>Accuracy (Differential Inputs)</b>						
RES	Resolution	—	16	—	Bits	
INL	Integral Non-Linearity	—	.0038	—	%FSR	V <sub>DD</sub> = 2.7V
V <sub>OS</sub>	Offset Error	—	—	<b>±0.9</b>	%FSR	IN+, IN- = 0V
V <sub>NOISE</sub>	Referred to input	—	60	—	μVrms	
CMR	Common Mode Rejection	—	75	—	dB	At DC
FSE	Full Scale Error	—	0.4%	—	%FS	
PSRR	Power Supply Rejection Ratio	—	75	—	dB	V <sub>DD</sub> = 2.5V to 3.5V
<b>IN+, IN-</b>						
V <sub>IN±</sub>	Differential Input Voltage	—	—	2.5	V	<b>Note 1</b>
	Absolute Voltage Range on IN+, IN-	—	—	V <sub>DD</sub>	V	
	Input Bias Current	—	1	100	nA	
C <sub>IN</sub>	Input Sampling Capacitance	—	2	—	pF	
R <sub>IN</sub>	Differential Input Resistance	—	2.0	—	MΩ	<b>Note 2</b>
<b>REF<sub>IN</sub>, REF<sub>OUT</sub></b>						
V <sub>REF</sub>	REF <sub>IN</sub> Voltage Range	0	—	1.25	V	
I <sub>REF</sub>	REF <sub>IN</sub> Input Current	—	1	—	μA	
V <sub>REFOUT</sub>	REF <sub>OUT</sub> Voltage	—	1.193	—	V	
REF <sub>SINK</sub>	REF <sub>OUT</sub> Current Sink Capability	—	10	—	μA	
REF <sub>SRC</sub>	REF <sub>OUT</sub> Current Source Capability	300	—	—	μA	

**Note 1:** Differential input voltage defined as (V<sub>IN+</sub> – V<sub>IN-</sub>).

**2:** Resistance from INn+ to INn- or INn to GND.

**3:** @ V<sub>DD</sub> = 1.8V, I<sub>SOURCE</sub> ≤ 200μA.

# TC3400

## TC3400 DC ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:**  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 2.7\text{V}$ , unless otherwise specified. **Boldface** type specifications apply for temperatures of  $0^\circ\text{C}$  to  $85^\circ\text{C}$ .  $V_{REF} = 1.25\text{V}$ , Internal Clock Frequency = 520kHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>SCLK</b>						
$V_{IL}$	Input Low Voltage	—	—	<b><math>0.3 \times V_{DD}</math></b>	V	
$V_{IH}$	Input High Voltage	<b><math>0.7 \times V_{DD}</math></b>	—	—	V	
$I_{LEAK}$	Leakage Current	—	1	—	$\mu\text{A}$	
<b>SDAT</b>						
$V_{OL}$	Output Low Voltage	—	—	0.4	V	$I_{OL} = 1.5\text{mA}$
$V_{OH}$	Output High Voltage (SDAT)	$0.9 \times V_{DD}$	—	—	V	$I_{SOURCE} = 400\mu\text{A}$ ( <b>Note 3</b> )

- Note 1:** Differential input voltage defined as  $(V_{IN+} - V_{IN-})$ .  
**Note 2:** Resistance from  $INn+$  to  $INn-$  or  $INn$  to GND.  
**Note 3:** @  $V_{DD} = 1.8\text{V}$ ,  $I_{SOURCE} \leq 200\mu\text{A}$ .

## TC3400 AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:**  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 2.7\text{V}$ , unless otherwise specified. **Boldface** type specifications apply for temperatures of  $0^\circ\text{C}$  to  $85^\circ\text{C}$ .  $V_{REF} = 1.25\text{V}$ , Internal Clock Frequency = 520kHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_1$	Resolution Reduction Clock Width	1	—	—	$\mu\text{sec}$	Width of SCLK (Negative)
$t_2$	Resolution Reduction Clock Width	1	—	—	$\mu\text{sec}$	Width of SCLK (Positive)
$t_3$	Conversion Time (15-bit Plus Sign)	—	125	—	msec	16-bit Conversion, $T_A = 25^\circ\text{C}$ ( <b>Note 1</b> )
	Conversion Time (14-bit Plus Sign)	—	$t_3/2.0$	—	msec	15-bit Conversion
	Conversion Time (13-bit Plus Sign)	—	$t_3/4.0$	—	msec	14-bit Conversion
	Conversion Time (12-bit Plus Sign)	—	$t_3/7.8$	—	msec	13-bit Conversion
	Conversion Time (11-bit Plus Sign)	—	$t_3/15.1$	—	msec	12-bit Conversion
	Conversion Time (10-bit Plus Sign)	—	$t_3/28.6$	—	msec	11-bit Conversion
	Conversion Time (9-bit Plus Sign)	—	$t_3/51.4$	—	msec	10-bit Conversion
$t_4$	Resolution Reduction Window	—	$t_3/85.7$	—	msec	Width of SCLK
$t_5$	SCLK to Data Valid	<b>1000</b>	—	—	nsec	SCLK Falling Edge to SDAT Valid
$t_8$	Acknowledge Delay	—	—	<b>1000</b>	nsec	SCLK to SDAT Delay

- Note 1:** Nominal temperature drift is  $-2830\text{ppm}/^\circ\text{C}$  for temperature less than  $25^\circ\text{C}$  and  $-1340\text{ppm}/^\circ\text{C}$  for temperatures greater than  $25^\circ\text{C}$ .

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin No. (8-Pin SOIC) (8-Pin PDIP)	Symbol	Description
1	IN+	Analog Input. This is the positive terminal of a true differential input consisting of IN+ and IN-. $V_{IN1} = (IN+ - IN-)$ . See Section 1.0 Electrical Characteristics.
2	IN-	Analog Input. This is the negative terminal of a true differential input consisting of IN+ and IN-. $V_{IN} = (IN+ - IN-)$ IN- can swing to, but not below, ground.
3	REF <sub>IN</sub>	Analog Input. The converter's reference voltage is the differential between this pin and ground times two. It may be tied directly to REF <sub>OUT</sub> or scaled using a resistor divider. Any user supplied reference voltage less than 1.25V may be used in place of REF <sub>OUT</sub> .
4	GND	Ground Terminal.
5	REF <sub>OUT</sub>	Analog Output. The internal reference connects to this pin. It may be scaled externally, if desired, and tied to the REF <sub>IN</sub> input to provide the converter's reference voltage. Care must be taken in connecting external circuitry to this pin.
6	SDAT	Digital Output (push-pull). This is the microPort™ serial data output. SDAT is driven low while the TC3400 is converting data, effectively providing a "busy" signal. After the conversion is complete, every high to low transition on the SCLK pin puts a bit from the resulting data word on the SDAT pin (from MSB to LSB).
7	SCLK	Digital Input. This is the microPort™ serial clock input. The TC3400 comes out of sleep mode and a conversion cycle begins when this pin is driven low. After the conversion starts, each additional falling edge (up to six) detected on SCLK for $t_4$ seconds reduces the A/D resolution by one bit. When the conversion is complete, the data word can be shifted out on the SDAT pin by clocking the SCLK pin.
8	V <sub>DD</sub>	Power Supply Input.

## 3.0 DETAILED DESCRIPTION

The TC3400 is a 16-bit sigma-delta A/D converter with one differential input. See the Typical Application circuit and the Functional Block diagram. The key components of the TC3400 are described below.

Also refer to Figure 3-4, A/D Operational Flowchart and the Timing Diagrams, Figure 3-1, Figure 3-2 and Figure 3-3).

### 3.1 A/D Converter Operation

When the TC3400 is not converting, it is in sleep mode with both the SCLK and SDAT lines high. An A/D conversion is initiated by a high to low transition on the SCLK line at which time the internal clock of the TC3400 is started. Each additional high to low transition of SCLK (following the initial SCLK falling edge) during the time interval  $t_4$ , will decrement the conversion resolution by one bit and reduce the conversion time by one half. The time interval  $t_4$  is referred to as the resolution reduction window. The minimum conversion resolution is 10-bits so any more than 6 SCLK transitions during  $t_4$  will be ignored.

After each high to low transition of SCLK, in the  $t_4$  interval, the SDAT output is driven high by the TC3400 to acknowledge that the conversion has been decremented. When the SCLK returns high or the  $t_4$  interval ends, the SDAT line returns low (see Figure 3-2). When the conversion is complete SDAT is driven high. The TC3400 now enters sleep mode and the conversion value can be read as a serial data word on the SDAT line.

### 3.2 Reading the Data Word

After the conversion is complete and SDAT goes high, the conversion value can be clocked serially onto the SDAT line by high to low transitions of the SCLK. The data word is in two's complement format with the sign bit clocked onto the SDAT line, first followed by the MSB and ending in the LSB. For a 16-bit conversion the data word would consist of a sign bit followed by 15 magnitude bits, Table 3-1 shows the data word versus input voltage for a 16-bit conversion. Note that the full scale input voltage range is  $\pm(2 \text{ REF}_{\text{IN}} - 1\text{LSB})$ . When  $\text{REF}_{\text{OUT}}$  is fed back directly to  $\text{REF}_{\text{IN}}$ , an LSB is  $73\mu\text{V}$  for a 16-bit conversion, as  $\text{REF}_{\text{OUT}}$  is typically 1.193V.

Figure 3-3 shows typical SCLK and SDAT waveforms for 16, 12 and 10-bit conversions. Note that any complete convert and read cycle requires 17 negative edge clock pulses. The first is the convert command. Then, up to six of these can occur in the resolution reduction window,  $t_4$ , to decrement resolution. The remaining pulses clock out the conversion data word.

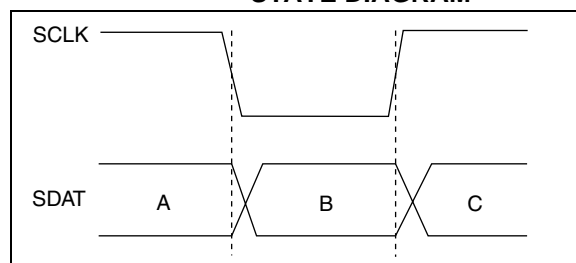
**TABLE 3-1: DATA CONVERSION WORD VS. VOLTAGE INPUT ( $\text{REF}_{\text{IN}} = 1.193\text{V}$ )**

Data Word	INn+ – INn- (Volts)
0111 1111 1111 1111	2.38596 (Positive Full Scale)
0000 0000 0000 0001	72.8 E -6
0000 0000 0000 0000	0
1111 1111 1111 1111	-72.8 E -6
1000 0000 0000 0001	-2.38596 (Negative Full Scale)
1000 0000 0000 0000	Reserved Code

The SCLK input has a filter which rejects any positive or negative pulse of width less than 50nsec to reduce noise. The rejection width of this pulse can vary between 50nsec and 750nsec depending on processing parameters and supply voltage.

Figure 3-1 and Table 3-2 show information for determining the mode of operation for the TC3400 part by recording the value of SDAT for SCLK in a high, then low, then high state. For example, if SCLK goes through a 1-0-1 transition and the corresponding values of SDAT are 1-1-0, then the SCLK falling edge started a new data conversion. A 0-1-0 for SDAT would have indicated a resolution reduction had occurred. This is useful if the microcontroller has a watchdog reset or otherwise loses track of where the TC3400 is in the conversion and data readout sequence. The microcontroller can simply transition SCLK until it "finds" a Start Conversion condition.

**FIGURE 3-1: SCLK, SDAT LOGIC STATE DIAGRAM**

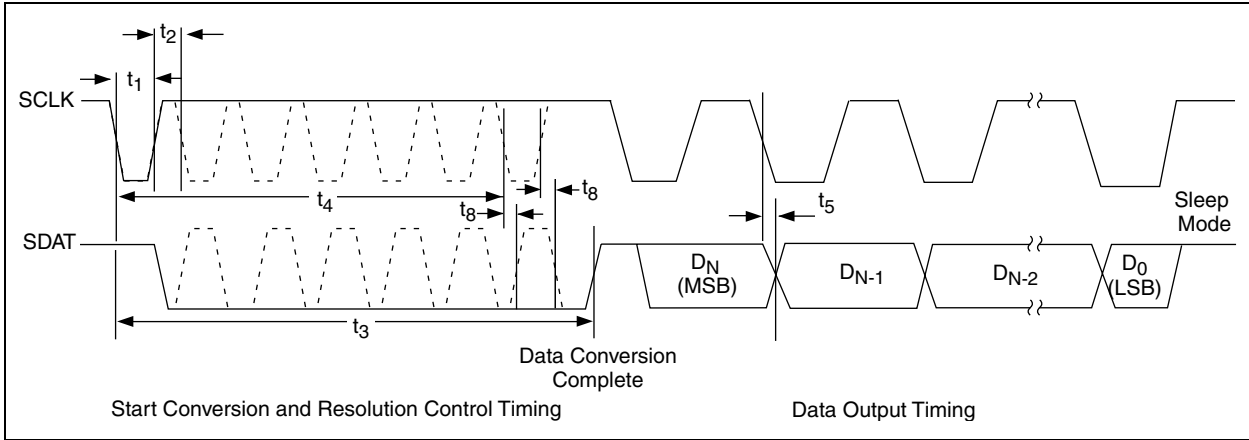


**TABLE 3-2: SCLK, SDAT LOGIC STATE**

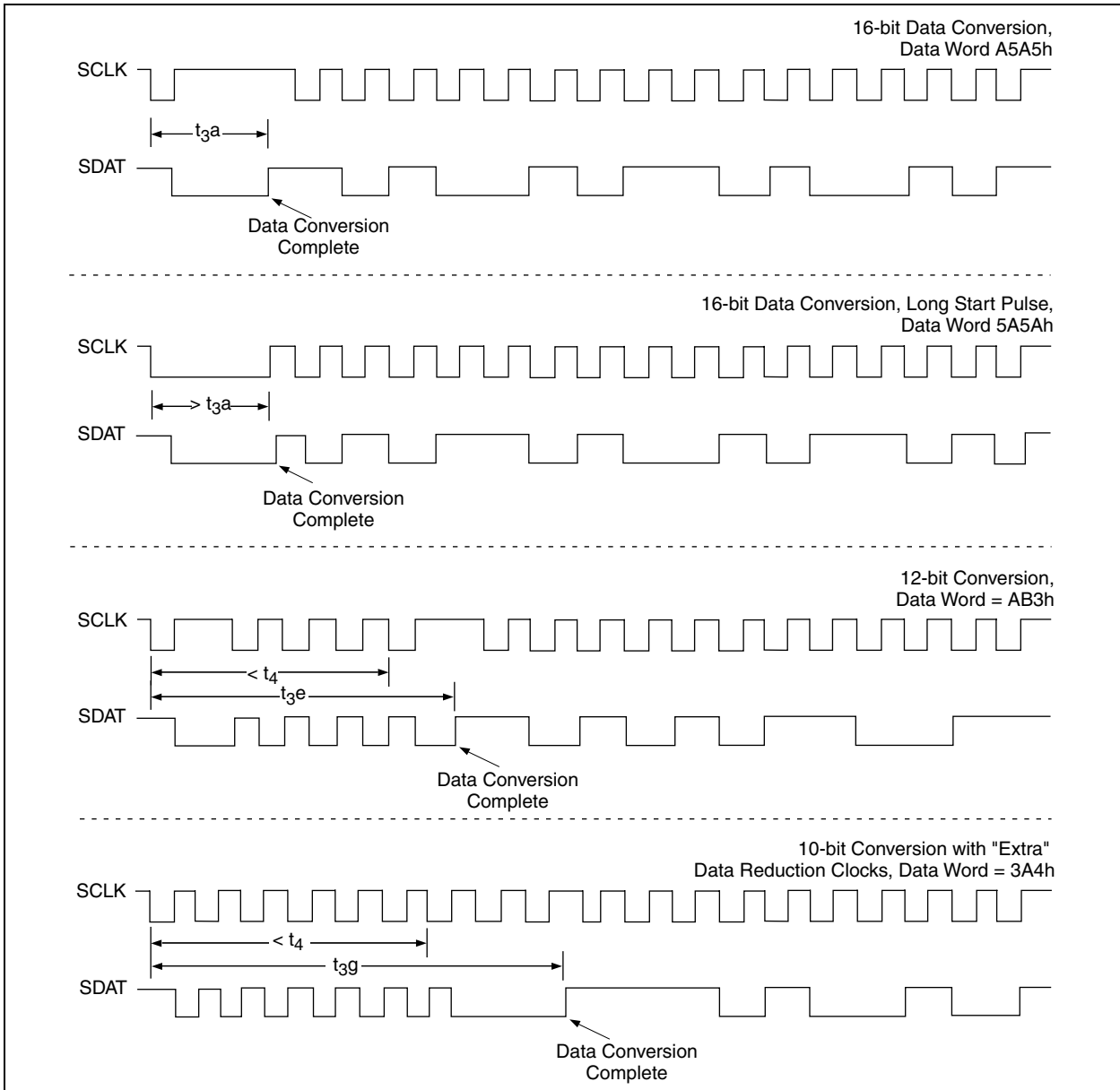
A	B	C	Status
1	1	0	Start Conversion
0	1	0	Resolution Reduction
x	1	1	Data Transfer
x	0	0	Data Transfer or Busy*

**\*Note:** The code X00 has a dual meaning: Data Transfer or Busy converting. To avoid confusion, the user should send only the required number of pulses for the desired resolution, then wait for SDAT to rise to 1, indicating conversion is complete before clocking SCLK again to read out data bits.

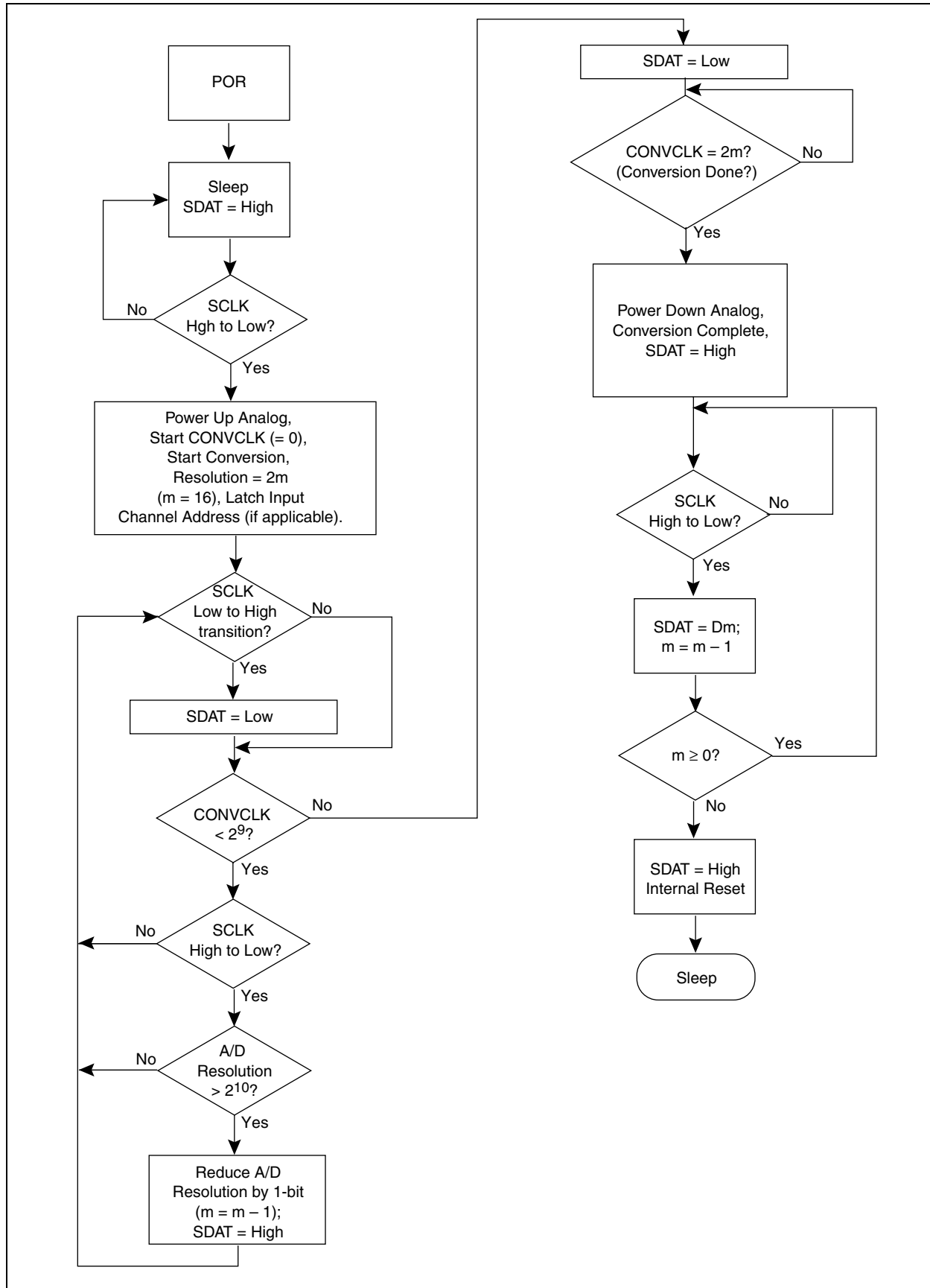
**FIGURE 3-2: CONVERSION AND DATA OUTPUT TIMING**



**FIGURE 3-3: SCLK AND SDAT WAVEFORMS FOR 16, 12 AND 10-BIT CONVERSIONS**



**FIGURE 3-4: A/D OPERATIONAL FLOWCHART**





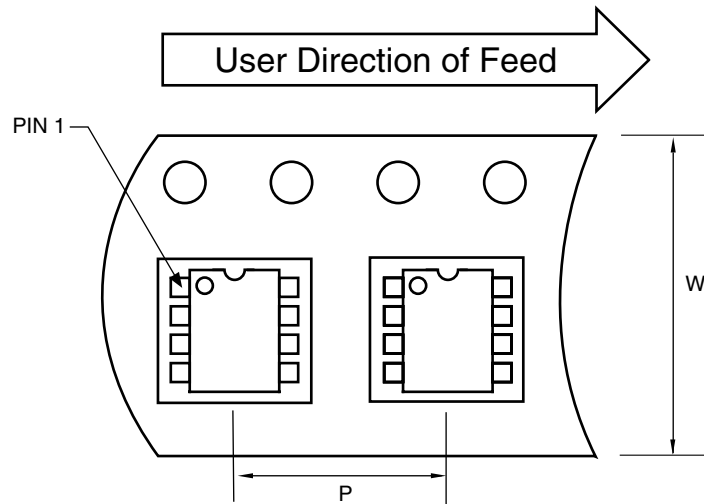
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

Package marking data not available at this time.

### 4.2 Taping Forms

#### Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Standard Reel Component Orientation  
for TR Suffix Device

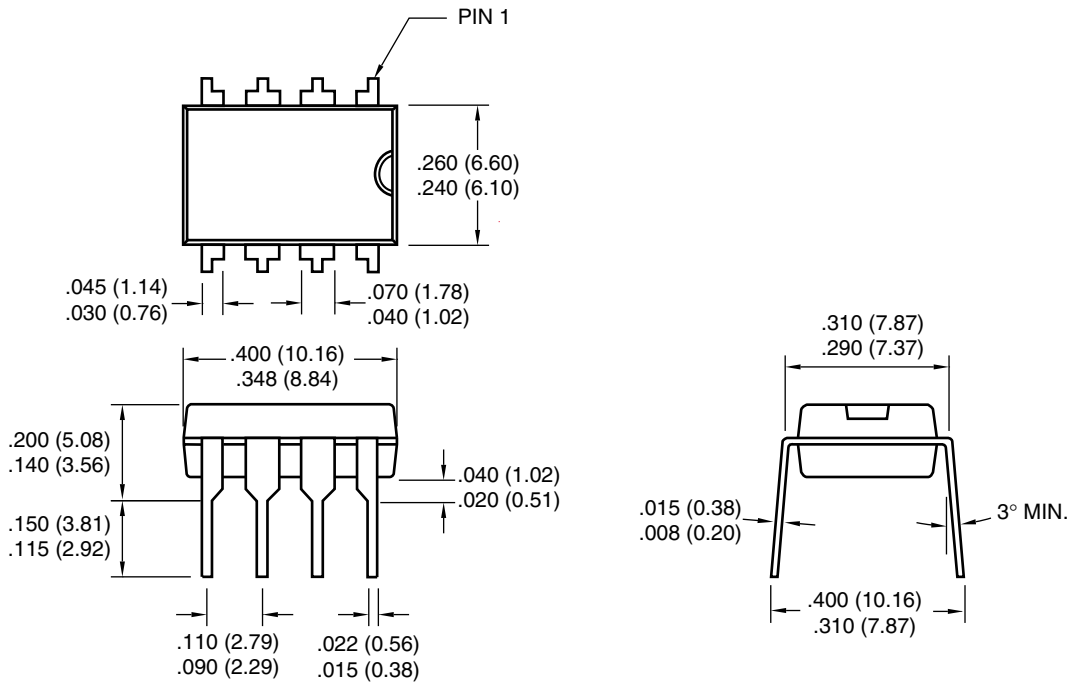
#### Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

# TC3400

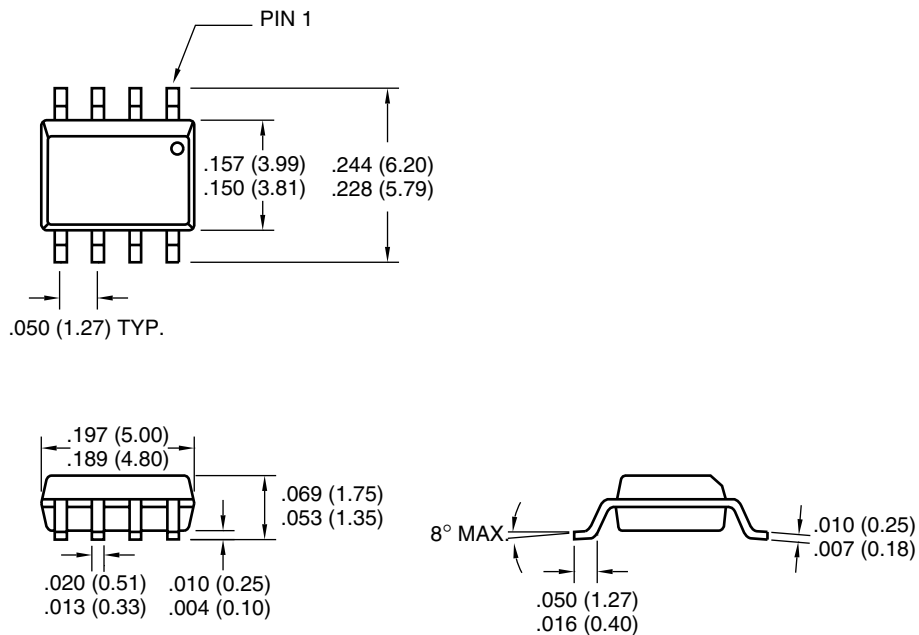
## 4.3 Package Dimensions

### 8-Pin Plastic DIP



Dimensions: inches (mm)

### 8-Pin SOIC



Dimensions: inches (mm)

NOTES:

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Tel: 631-273-5305 Fax: 631-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Microchip Technology Australia Pty Ltd  
Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

#### China - Beijing

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Beijing Liaison Office  
Unit 915  
Bei Hai Wan Tai Bldg.  
No. 6 Chaoyangmen Beidajie  
Beijing, 100027, No. China  
Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Chengdu

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Chengdu Liaison Office  
Rm. 2401, 24th Floor,  
Ming Xing Financial Tower  
No. 88 TIDU Street  
Chengdu 610016, China  
Tel: 86-28-86766200 Fax: 86-28-86766599

#### China - Fuzhou

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Fuzhou Liaison Office  
Unit 28F, World Trade Plaza  
No. 71 Wusi Road  
Fuzhou 350001, China  
Tel: 86-591-7503506 Fax: 86-591-7503521

#### China - Shanghai

Microchip Technology Consulting (Shanghai)  
Co., Ltd.  
Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

#### China - Shenzhen

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Shenzhen Liaison Office  
Rm. 1315, 13/F, Shenzhen Kerry Centre,  
Renminnan Lu  
Shenzhen 518001, China  
Tel: 86-755-2350361 Fax: 86-755-2366086

#### China - Hong Kong SAR

Microchip Technology Hongkong Ltd.  
Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaugnessey Road  
Bangalore, 560 025, India  
Tel: 91-80-2290061 Fax: 91-80-2290062

### Japan

Microchip Technology Japan K.K.  
Benex S-1 6F  
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Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-6334-8870 Fax: 65-6334-8850

### Taiwan

Microchip Technology Taiwan  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Denmark

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Lautrup høj 1-3  
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#### Germany

Microchip Technology GmbH  
Gustav-Heinemann Ring 125  
D-81739 Munich, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

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Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

#### United Kingdom

Microchip Ltd.  
505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5869 Fax: 44-118 921-5820

05/01/02

