19-3800; Rev 0; 5/08

EVALUATION KIT AVAILABLE

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceiver

General Description

The MAX13170E is a three-driver/three-receiver multiprotocol transceiver that operates from a +5V single supply. The MAX13170E, along with the MAX13172E and the MAX13174E, form a complete software-selectable data terminal equipment (DTE) or data communication equipment (DCE) interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21), and V.35 protocols. The MAX13170E transceivers carry the high-speed clock and data signals, while the MAX13172E carry the control signals. The MAX13170E can be terminated by the MAX13174E software-selectable resistor termination network or by discrete termination networks.

The MAX13170E has an internal charge pump and a proprietary low-dropout transmitter output stage that allows V.11-, V.28-, and V.35-compliant operation from a +5V single supply. The MAX13170E features a no-cable mode that reduces supply current to 0.5µA, and disables all (high-impedance) transmitter and receiver outputs. Short-circuit current limiting and thermal shutdown circuitry protect the receiver and transmitter outputs against excessive power dissipation. The MAX13170E has extended ESD protection for all the transmitter outputs and receivers inputs.

The MAX13170E is available in a 5.3mm x 10.2mm, 28-pin SSOP package and operates over the 0°C to +70°C commercial temperature range.

Features

- ♦ The MAX13170E/MAX13172E/MAX13174E Chipset is a Pin-for-Pin Upgrade to the MXL1544/MAX3175/MXL1543/MXL1543B Chipset
- ♦ Supports RS-232, RS-449, EIA-530, EIA-530A, V.35, V.36, and X.21
- ♦ Software-Selectable Cable Termination Using the MAX13174E
- ♦ Complete DTE or DCE Port with the MAX13172E/MAX13174E
- ♦ Fail-Safe Receivers
- ♦ +5V Single-Supply Operation
- ♦ 0.5µA No-Cable Mode
- ♦ TUV-Certified NET1/NET2 and TBR1/TBR2-Compliant (Pending)
- ♦ Extended ESD Protection for All the Transmitter Outputs and Receivers Inputs to GND
  - ±13kV Using the Human Body Model
  - ±8kV Using the Contact Method Specified in IEC 61000-4-2
  - ±5kV Using the Air-Gap Discharge Method Specified in IEC 61000-4-2

Applications

Data Networking	PCI Cards
CSU and DSU	Telecommunications Equipment
Data Routers	

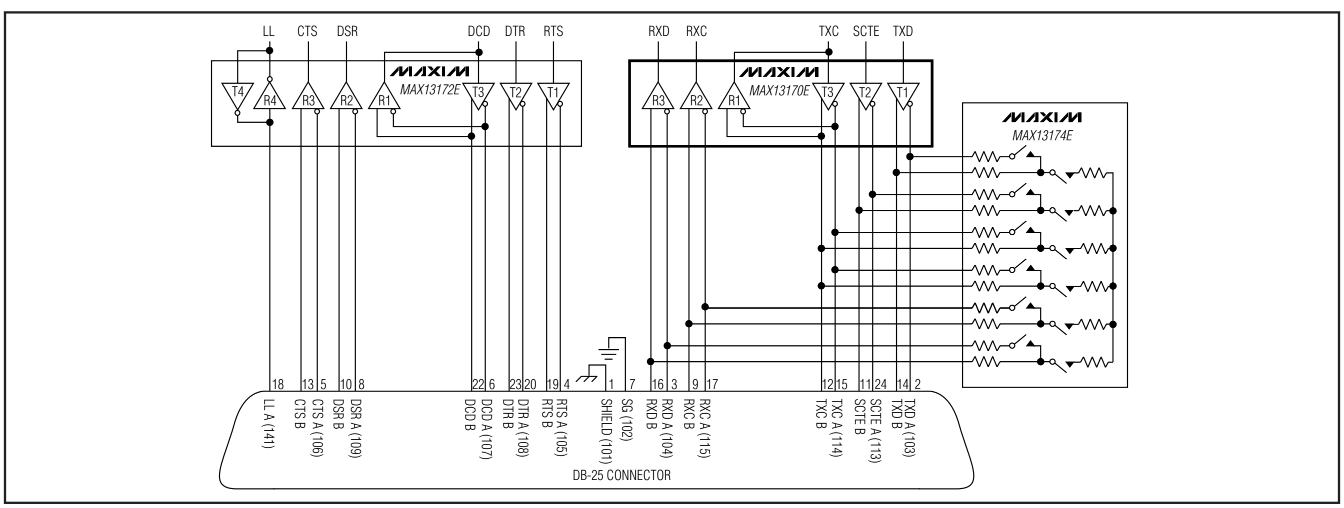
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX13170ECAI+	0°C to +70°C	28 SSOP

+Denotes a lead-free package.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceiver

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

Supply Voltages
- V_{CC} ....-0.3V to +6V

Charge-Pump Output Voltages
- V_{DD} ....-0.3V to +7.1V
- V_{EE} ....+0.3V to -7.1V
- V_{DD} to V_{CC} ....-0.6 to +6V

Logic Input Voltages
- M0, M1, M2, DCE/$\overline{\text{DTE}}$, T_IN ....-0.3V to +6V

Logic Output Voltages
- R_OUT ....-0.3V to (V_{CC} + 0.3V)

Transmitter Outputs
- T_OUT_, T3OUT_/R1IN_ (No Cable Mode or V.28) ....-15V to +15V
- Short-Circuit Duration to GND ....Continuous

Receiver Inputs
- R_IN_T3OUT_/R1IN_ ....-15V to +15V
- R_INA to R_INB, T3OUT/R1INA to T3OUT/R1INB ....-15V to +15V

Continuous Power Dissipation (T_A = +70°C)
- 28-Pin SSOP (derate 9.5mW/°C above +70°C) 762mW

Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
- 28-Pin SSOP ....25°C/W

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
- 28-Pin SSOP ....67°C/W

Operating Temperature Range ....0°C to 70°C
Junction Temperature ....150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Package thermal resistances were obtained using the method described in JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, C_3 = C_4 = C_5 = 4.7μF, C_1 = C_2 = 1μF, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Operating Range	V_{CC}		4.5		5.5	V
V_{CC} Supply Current (DCE Mode) (Digital Inputs = GND or V_{CC}) (Transmitter Outputs Static)	I_{CC}	V.11 mode, no load		15	28	mA
		V.11 mode, full load		133	180	
		V.35 mode, no load		21	38	
		V.35 mode, full load		153	195	
		V.28 mode, no load		16	30	
		V.28 mode, full load		29	40	
		No cable mode		0.5	10	μA
Internal Power Dissipation (DCE Mode)	P_D	V.11 mode, full load		200		mW
		V.35 mode, full load		750		
		V.28 mode, full load		100		
Positive Charge-Pump Output Voltage (Note 3)	V_{DD}	V.28, V.35 modes, no load	6.5	6.9	7.1	V
		V.28, V.35 modes, with load, I_{DD} = 10mA	5.6	6.9		
		V.11 mode	5.15	5.3	5.7	
		V.11 mode, V_{DD} variation, I_{DD} = 0mA to 25mA		0.01		
Negative Charge-Pump Output Voltage	V_{EE}	V.28, V.35 modes, no load		-6.9		V
		V.28, V.35 modes, with load, I_{EE} = 10mA (Note 3)		-6.7	-5.4	
		V.11 mode (Note 3)	-4.84	-4.5	-4.16	
		V.11 mode, V_{EE} variation, I_{EE} = 0mA to 25mA		0.01		
Charge-Pump Enable Time		Time it takes for both V_{DD} and V_{EE} to reach specified range		<1		ms
Thermal Shutdown Protection	THSD			145		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, C_3 = C_4 = C_5 = 4.7µF, C_1 = C_2 = 1µF, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (M0, M1, M2, DCE/$\overline{\text{DTE}}$, T1IN, T2IN, T3IN)						
Input High Voltage	V_{IH}		0.66 x V_{CC}			V
Input Low Voltage	V_{IL}				0.33 x V_{CC}	V
Logic-Input Current	I_{IN}	T1IN, T2IN, T3IN	-1		+1	µA
Pullup Resistor	R_{PUIN}	M0, M1, M2, DCE/$\overline{\text{DTE}}$ to V_{CC}	50	100	170	kΩ
LOGIC OUTPUTS (R1OUT, R2OUT, R3OUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA	0.66 x V_{CC}			V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.33 x V_{CC}	V
Output Pullup Resistor	R_{PUY}	No-cable mode (to V_{CC})		71.4		kΩ
Transmitter Output Leakage Current	I_Z	-0.25V < V_{OUT} < +0.25V, V_{CC} = 0 or no-cable mode		+5	0.2	µA
V.11 TRANSMITTER						
Open-Circuit Differential Output Voltage	V_{ODO}	Open circuit, R = 1.95kΩ, Figure 1	$-V_{CC}$		$+V_{CC}$	V
Loaded Differential Output Voltage (Note 4)	V_{ODL}	R = 50Ω, Figure 1	0.5 x V_{ODO}			V
		R = 50Ω, Figure 1	|2|			
Change in Magnitude of Output Differential Voltage	ΔV_{OD}	R = 50Ω, Figure 1			0.2	V
Common-Mode Output Voltage	V_{OC}	R = 50Ω, Figure 1			3.0	V
Change in Magnitude of Common-Mode Output Voltage	ΔV_{OC}	R = 50Ω, Figure 1			0.2	V
Short-Circuit Current	I_{SC}	V_{OUT} = GND			150	mA
Rise Time	t_R	Figures 2, 6		4.5	10	ns
Fall Time	t_F	Figures 2, 6		6.5	10	ns
Transmitter Input-to-Output Prop Delay	t_{PHL}, t_{PLH}	Figures 2, 6		16	22	ns
Data Skew	$\|t_{PHL}-t_{PLH}\|$	Figures 2, 6 (Note 3)			3	ns
Output-to-Output Skew	t_{SKEWT}	Figures 2, 6 (Notes 3, 5)			2.5	ns
V.11 RECEIVER						
Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +7V	-200		-50	mV
Input Hysteresis	ΔV_{TH}	-7V ≤ V_{CM} ≤ +7V		13		mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	-0.66		+0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	15	30		kΩ
Rise or Fall Time	t_R, t_F	Figures 2, 7		3		ns
Receiver Input-to-Output Delay	t_{PHL}, t_{PLH}	Figures 2, 7			23	ns
Data Skew	$\|t_{PHL}-t_{PLH}\|$	Figures 2, 7 (Note 3)			3	ns
Output-to-Output Skew	t_{SKEWR}	(Notes 3, 5)			2.5	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, $C_3 = C_4 = C_5$ = 4.7µF, $C_1 = C_2$ = 1µF, $T_A = T_{MIN}$ to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V.35 TRANSMITTER							
Differential Output Voltage	V_{OD}	With load, -4V < V_{CM} < +4V, Figure 3		±0.44	±0.55	±0.66	V
Output High Current	I_{OH}	$V_{A,B}$ = 0		-13	-11	-9	mA
Output Low Current	I_{OL}	$V_{A,B}$ = 0		9	11	13	mA
Rise or Fall Time	t_R, t_F	Figures 3, 6			5		ns
Transmitter Input-to-Output Delay	t_{PLH}, t_{PHL}	Figures 3, 6			19	35	ns
Data Skew	$\lvert t_{PLH} - t_{PHL} \rvert$	Figures 3, 6, (Note 3)				3	ns
Output-to-Output Skew	t_{SKEWT}	Figures 3, 6, (Notes 3, 5)				3	ns
V.35 RECEIVER							
Differential Threshold Voltage	V_{TH}	-2V ≤ V_{CM} ≤ +2V		-200		-50	mV
Input Hysteresis	ΔV_{TH}	-2V ≤ V_{CM} ≤ +2V			15		mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V		-0.66		+0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V		15	30		kΩ
Rise or Fall Time	t_R, t_F	Figures 3, 7			3		ns
Receiver Input-to-Output Delay	t_{PHL}, t_{PLH}	Figures 3, 7 (Note 3)				23	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	Figures 3, 7 (Note 3)				3	ns
Output-to-Output Skew	t_{SKEWR}	(Notes 3, 5)				2.5	ns
V.28 TRANSMITTER							
Output Voltage Swing	V_{OD}	Open circuit (output high)				V_{DD}	V
		Open circuit (output low)		V_{EE}			
		R_L = 3kΩ	Output high	5	6.8		
			Output low		-6.8	-5	
Short-Circuit Current	$\lvert I_{SC} \rvert$					85	mA
Output Slew Rate	$SR_{R/F}$	R_L = 3kΩ, C_L = 2500pF, Figures 4, 8		4		30	V/µs
Transmitter Input-to-Output Delay from Low to High	t_{PHL}	R_L = 3kΩ, C_L = 2500pF, Figures 4, 8			1	2	µs
Transmitter Input-to-Output Delay from High to Low	t_{PLH}	R_L = 3kΩ, C_L = 2500pF, Figures 4, 8			1	2	µs
V.28 RECEIVER							
Input Threshold Low	V_{IL}			0.8			V
Input Threshold High	V_{IH}					2	V
Input Hysteresis	V_{HYST}				0.25		V
Input Resistance	R_{IN}	-15V ≤ V_{IN} ≤ +15V		3	5	7	kΩ
Rise or Fall Time	t_R, t_F	Figures 5, 9			3		ns
Receiver Input-to-Output Delay	t_{PHL}, t_{PLH}	Figures 5, 9				150	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, C_3 = C_4 = C_5 = 4.7µF, C_1 = C_2 = 1µF, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C.) (Note 2)

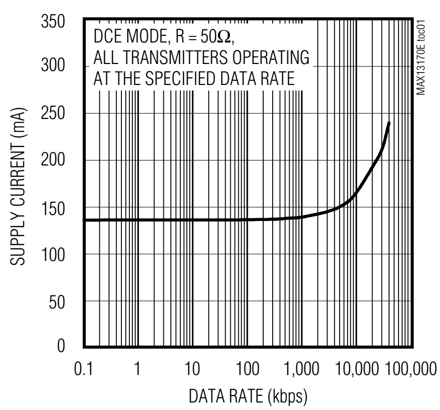
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION (T_OUT_, T_OUT_/R_OUT_, R_IN_ to GND)						
ESD Protection		Contact Discharge IEC61000-4-2		±8		kV
		Air-Gap Discharge IEC61000-4-2		±5		
		Human Body Model		±13		

Note 2: All devices are 100% production tested at T_A = +70°C and are guaranteed by design for T_A = 0°C to +70°C as specified.
Note 3: Guaranteed by design, not production tested.
Note 4: V_{ODL} is guaranteed at both 0.5 x V_{ODO} and l2Vl.
Note 5: Ouput-to-output skews are evaluated as a difference of propagation delays between different channels in the same condtion and for the same polarity (LH or HL).

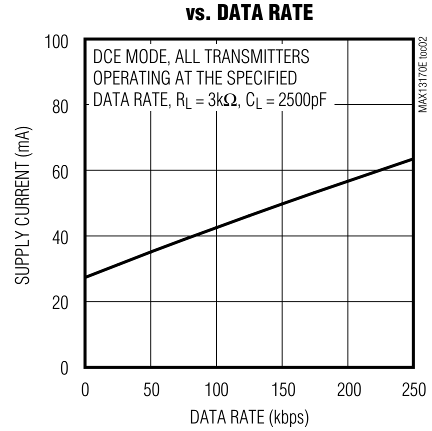
Typical Operating Characteristics

(V_{CC} = +5.0V, C1 = C2 =1µF, C3 = C4 = C5 = 4.7µF, (Figure 10), T_A = T_{MIN} to T_{MAX}, T_A = +25°C, unless otherwise noted.)

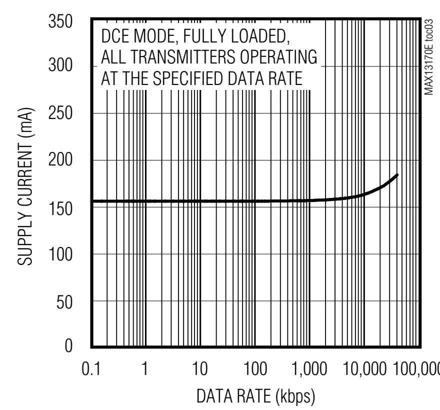
V.11 SUPPLY CURRENT vs. DATA RATE



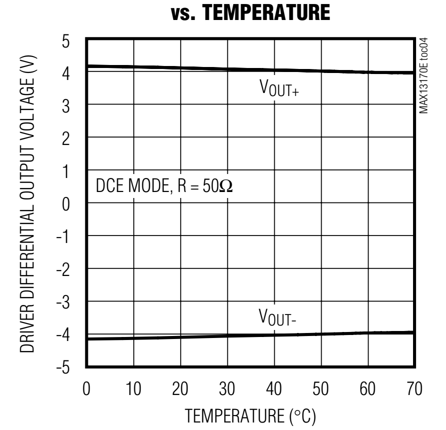
V.28 SUPPLY CURRENT vs. DATA RATE



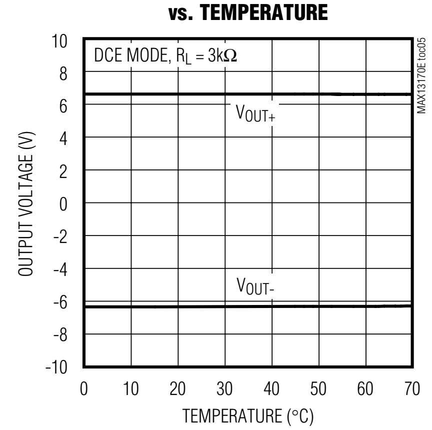
V.35 SUPPLY CURRENT vs. DATA RATE



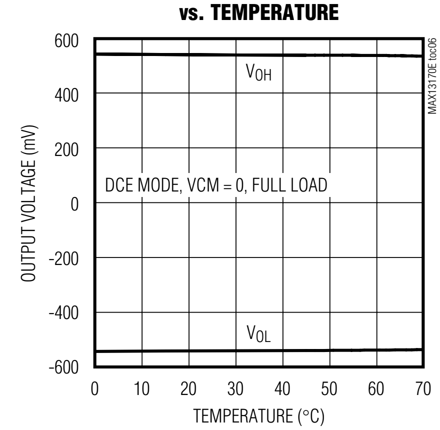
V.11 DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



V.28 OUTPUT VOLTAGE vs. TEMPERATURE



V.35 OUTPUT VOLTAGE vs. TEMPERATURE

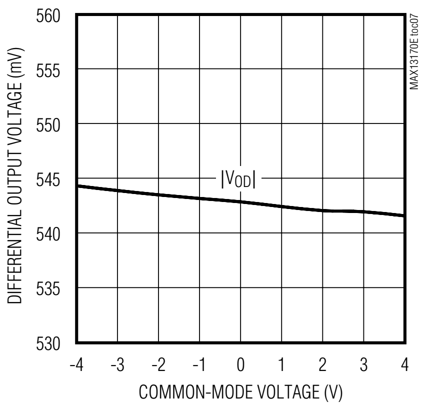


+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceiver

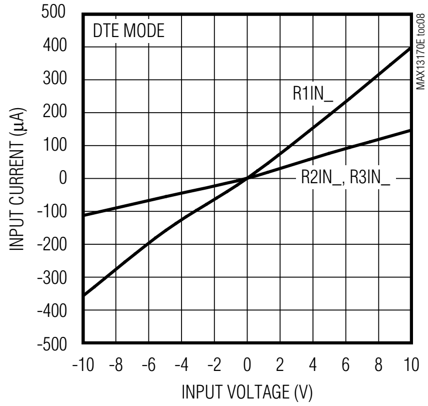
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, C1= C2 = C4 =1µF, C3 = C5 = 4.7µF (Figure 10), T_A = +25°C, unless otherwise noted.)

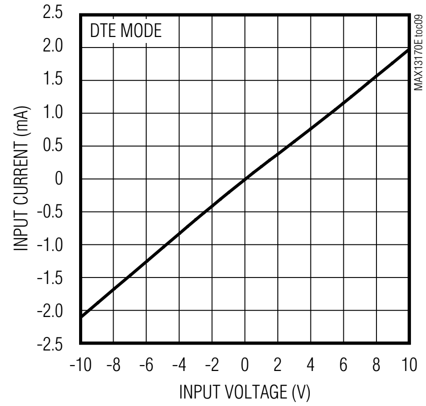
V.35 LOADED DIFFERENTIAL OUTPUT VOLTAGE vs. COMMON-MODE VOLTAGE



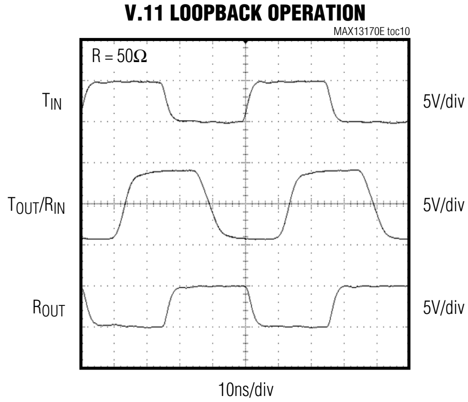
V.11/V.35 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



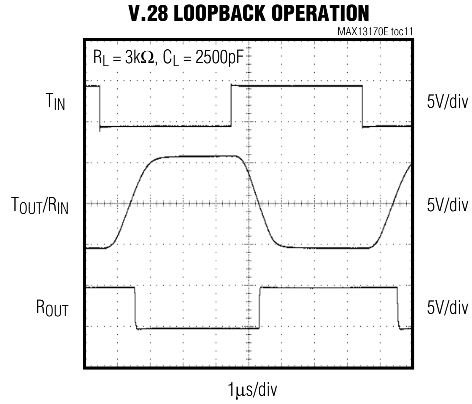
V.28 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



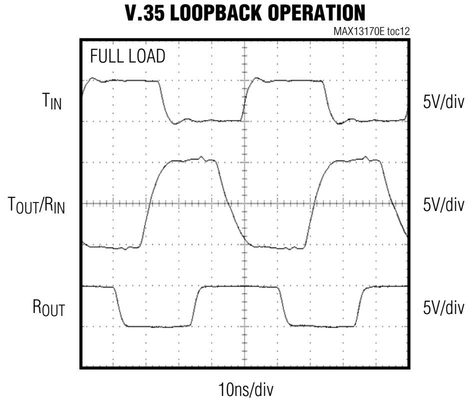
V.11 LOOPBACK OPERATION



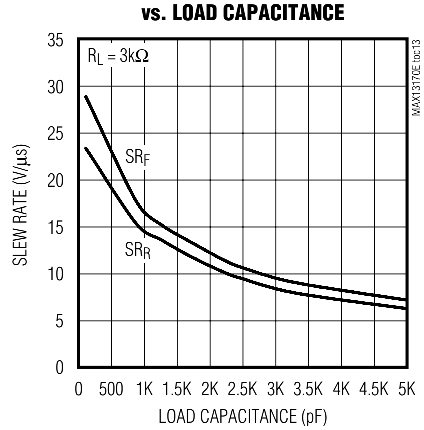
V.28 LOOPBACK OPERATION



V.35 LOOPBACK OPERATION



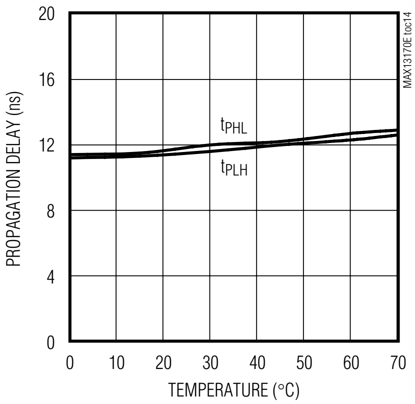
V.28 SLEW RATE vs. LOAD CAPACITANCE



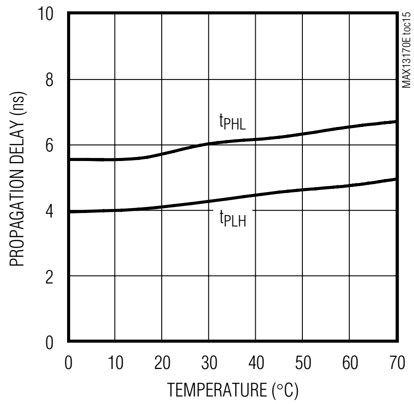
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, C1= C2 = C4 =1μF, C3 = C5 = 4.7μF (Figure 10), T_A = +25°C, unless otherwise noted.)

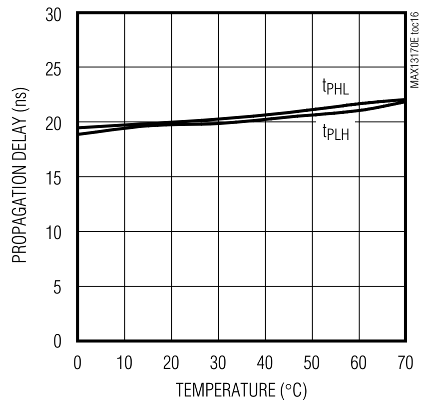
V.11 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE



V.11/V.35 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



V.35 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE



Test Circuits

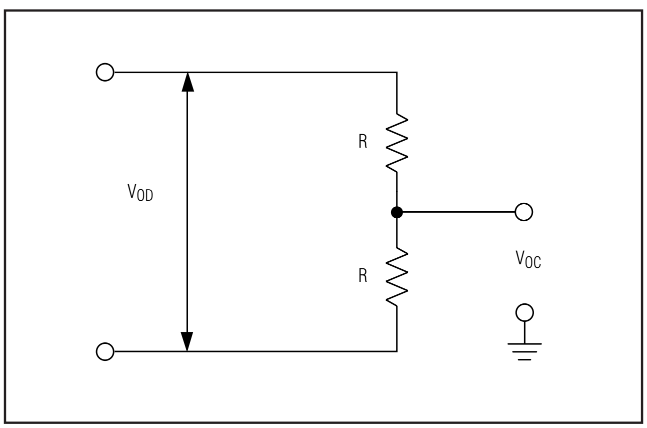


Figure 1. V.11 DC Test Circuit

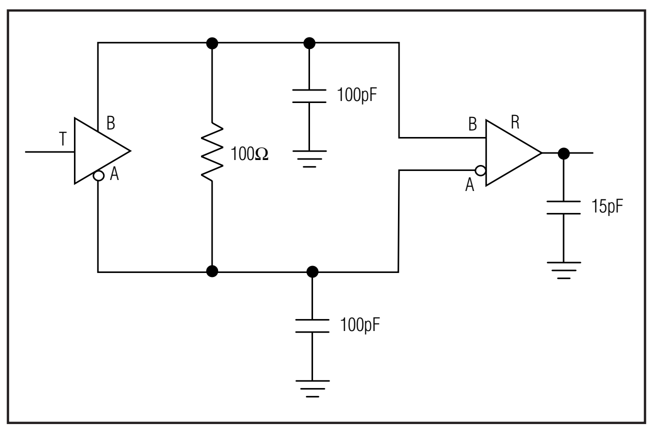


Figure 2. V.11 AC Test Circuit

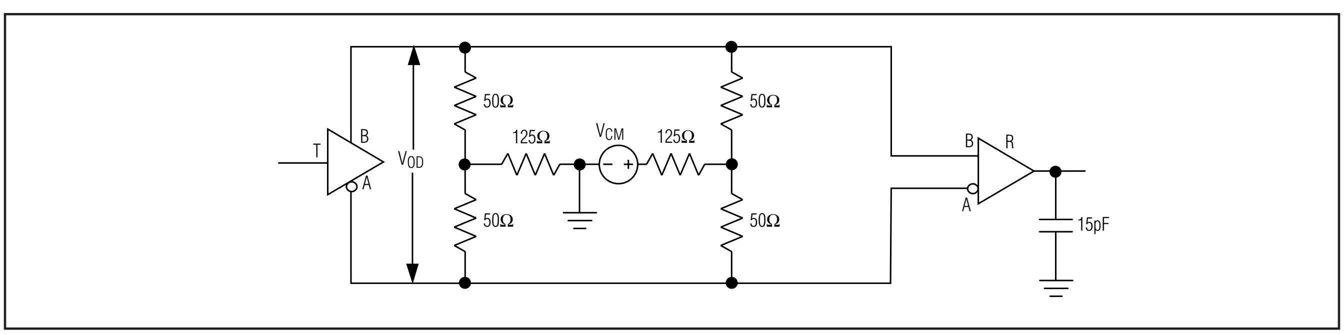


Figure 3. V.35 Transmitter/Receiver Test Circuit

Test Circuits (continued)

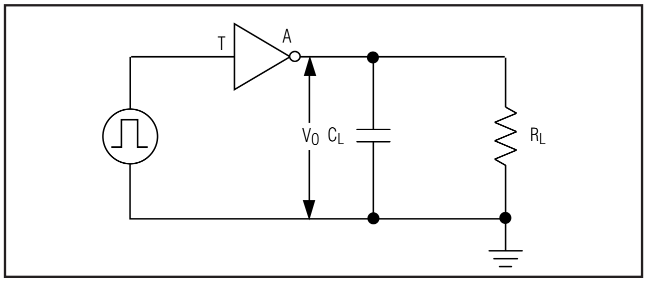


Figure 4. V.28 Transmitter Test Circuit

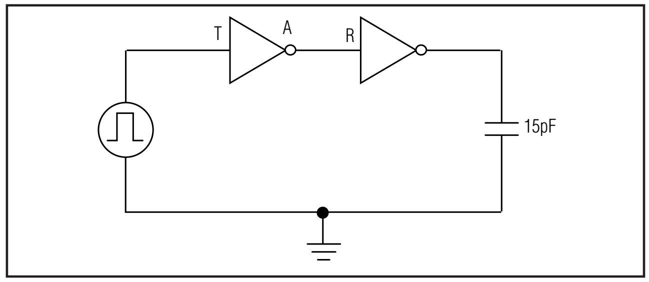


Figure 5. V.28 Receiver Test Circuit

Timing Diagrams

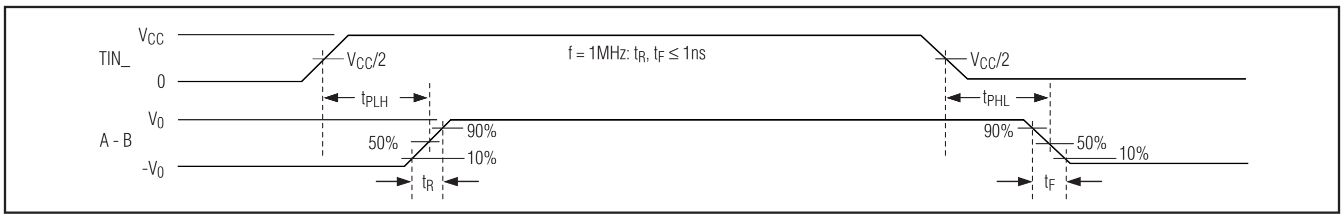


Figure 6. V.11, V.35 Transmitter Propagation Delays

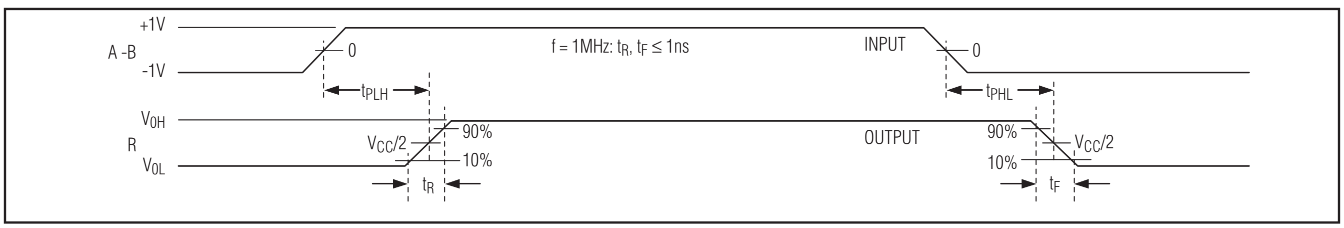


Figure 7. V.11, V.35 Receiver Propagation Delays

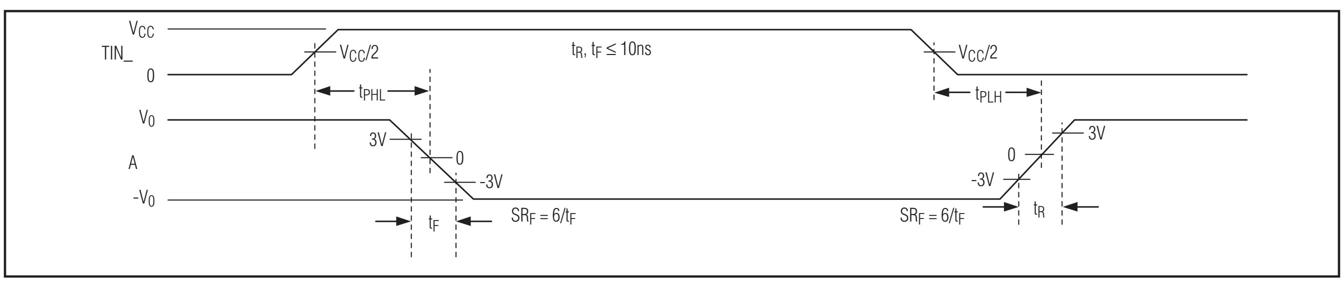


Figure 8. V.28 Transmitter Propagation Delays

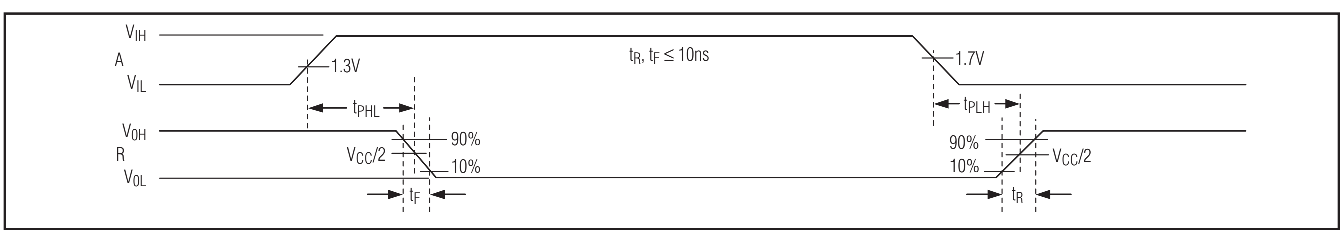


Figure 9. V.28 Receiver Propagation Delays

Pin Description

PIN	NAME	FUNCTION
1	C1-	V_{DD} Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C1+ and C1- as close as possible to the device.
2	C1+	V_{DD} Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C1+ and C1- as close as possible to the device.
3	V_{DD}	Charge-Pump Positive-Supply Output. Connect a 4.7µF ceramic capacitor from V_{DD} to ground as close as possible to the device.
4	V_{CC}	Device Supply Voltage. Bypass V_{CC} with a 4.7µF capacitor to ground as close as possible to the device.
5	T1IN	Transmitter 1 Logic Input
6	T2IN	Transmitter 2 Logic Input
7	T3IN	Transmitter 3 Logic Input
8	R1OUT	Receiver 1 Logic Output. Internally pull up to V_{CC}.
9	R2OUT	Receiver 2 Logic Output. Internally pull up to V_{CC}.
10	R3OUT	Receiver 3 Logic Output. Internally pull up to V_{CC}.
11	M0	Mode Select 0 Input. Internally pull up to V_{CC}.
12	M1	Mode Select 1 Input. Internally pull up to V_{CC}.
13	M2	Mode Select 2 Input. Internally pull up to V_{CC}.
14	DCE/$\overline{\text{DTE}}$	DCE/DTE Mode-Select Input. Internally pull up to V_{CC}.
15	R3INB	Receiver 3 Noninverting Input
16	R3INA	Receiver 3 Inverting Input
17	R2INB	Receiver 2 Noninverting Input
18	R2INA	Receiver 2 Inverting Input
19	T3OUTB/ R1INB	Transmitter 3 Noninverting Output/Receiver 1 Noninverting Input
20	T3OUTA/ R1INA	Transmitter 3 Inverting Output/Receiver 1 Inverting Input
21	T2OUTB	Transmitter 2 Noninverting Output
22	T2OUTA	Transmitter 2 Inverting Output
23	T1OUTB	Transmitter 1 Noninverting Output
24	T1OUTA	Transmitter 1 Inverting Output
25	GND	Ground
26	V_{EE}	Charge-Pump Negative Supply Output. Connect a 4.7µF ceramic capacitor from V_{EE} to ground as close as possible to the device.
27	C2-	V_{EE} Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C2+ and C2- as close as possible to the device.
28	C2+	V_{EE} Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C2+ and C2- as close as possible to the device.

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceiver

Detailed Description

The MAX13170E is a three-driver/three-receiver, multiprotocol transceiver that operates from a single +5V supply. The MAX13170E, along with the MAX13172E and MAX13174E, form a complete software-selectable DTE or DCE interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21), and V.35 protocols. The MAX13170E transceivers carry the high-speed clock and data signals, while the MAX13172E transceivers carry serial-interface control signaling. The MAX13170E can be terminated by the MAX13174E software-selectable resistor termination network or by a discrete termination network. The MAX13170E features a 0.5µA no-cable mode, fail-safe operation, and thermal shutdown circuitry. Thermal shutdown protects the drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the receiver and transmitter outputs into a high-impedance state.

Mode Selection

The state of the mode-select inputs M0, M1, and M2 determines which serial interface protocol is selected (Table 1). The state of the DCE/$\overline{\text{DTE}}$ input determines whether the transceiver is configured as a DTE or DCE serial port. When the DCE/$\overline{\text{DTE}}$ input is logic-high, driver T3 is activated and receiver R1 is disabled. When the DCE/$\overline{\text{DTE}}$ input is logic-low, driver T3 is disabled and receiver R1 is activated (Table 1). M0, M1, M2, and DCE/$\overline{\text{DTE}}$ are internally pulled up to V_{CC} to ensure a logic-high if left unconnected.

No-Cable Mode

The MAX13170E enters no-cable mode when the mode-select inputs are left unconnected or connected high (M0 = M1 = M2 = 1). In this mode, the multiprotocol drivers and receivers are disabled and the supply current drops to 0.5µA. The receivers' outputs enter a high-impedance state in no-cable mode, allowing these output lines to be shared with other receivers' outputs, (the receivers' outputs have internal pullup resistors to pull the outputs high if not driven). Also, in no-cable mode, the transmitter outputs enter a high-impedance state so that these output lines can be shared with other devices.

Dual Charge-Pump Voltage Converter

The MAX13170E internal power supply consists of a regulated dual charge pump that provides positive and negative output voltages from a +5V supply. The charge pump operates in discontinuous mode. If the output voltage is less than the regulated voltage, the charge pump is enabled. If the output voltage exceeds the regulated voltage, the charge pump is disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C5) to generate the V_{DD} and V_{EE} supplies. Figure 10 shows charge-pump connections.

Table 1. Mode Selection

MAX13170E MODE NAME	M2	M1	M0	DCE/$\overline{\text{DTE}}$	T1	T2	T3	R1	R2	R3
Not Used (Default V.11)	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530A	0	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11
X.21	0	1	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.35	1	0	0	0	V.35	V.35	Z	V.35	V.35	V.35
RS-449/V.36	1	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.28/RS-232	1	1	0	0	V.28	V.28	Z	V.28	V.28	V.28
No Cable	1	1	1	0	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530A	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530	0	1	0	1	V.11	V.11	V.11	Z	V.11	V.11
X.21	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.35	1	0	0	1	V.35	V.35	V.35	Z	V.35	V.35
RS-449/V.36	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.28/RS-232	1	1	0	1	V.28	V.28	V.28	Z	V.28	V.28
No Cable	1	1	1	1	Z	Z	Z	Z	Z	Z

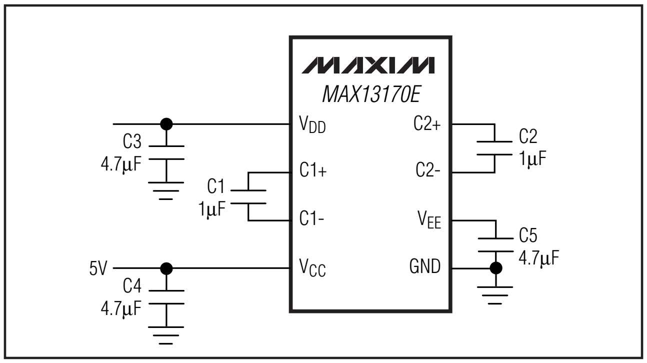


Figure 10. Charge Pump

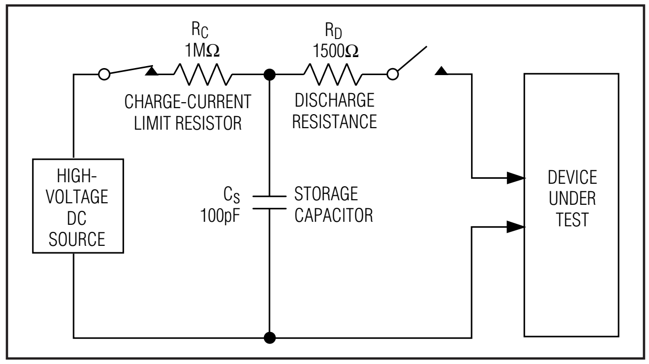


Figure 11a. Human Body ESD Test Model

Fail-Safe Receivers

The MAX13170E guarantees a logic-high receiver output when the receiver inputs are shorted, or when they are connected to a terminated transmission line with all the drivers disabled. This is done by setting the receivers' threshold between -50mV and -200mV in the V.11 and V.35 modes. If the differential receiver input voltage (B - A) is ≥ -50mV, R_OUT is logic-high. If (B - A) is ≤ -200mV, R_OUT is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination. With the receiver thresholds of the MAX13170E, this results in a logic-high with a 50mV minimum noise margin.

ESD Protection

As with all Maxim devices, a minimum of ±2kV-to-GND ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13170E have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±13kV without damage (HBM). The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13170E keeps working without latchup or damage. ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX13170E are characterized for protection to the following limits:

- ±13kV using the Human Body Model
- ±8kV using the Contact Method specified in IEC 61000-4-2
- ±5kV using the Air-Gap Discharge Method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11a shows the Human Body Model, and Figure 11b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

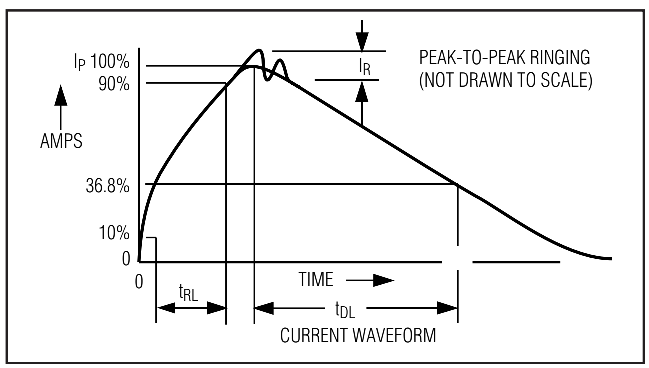


Figure 11b. Human Body Current Waveform

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceiver

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13170E help equipment designs to meet IEC 61000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 11c shows the IEC 61000-4-2 model, and Figure 11d shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

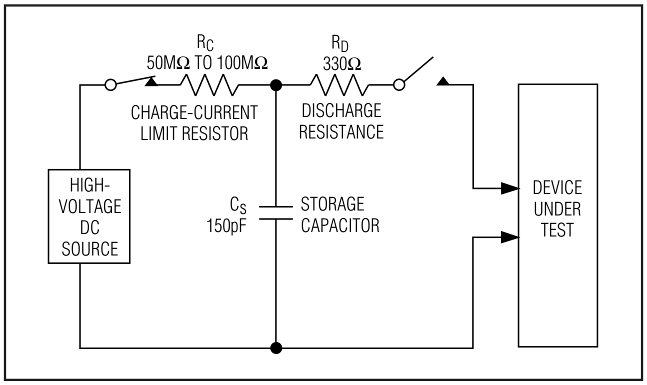


Figure 11c. IEC 61000-4-2 ESD Test Model

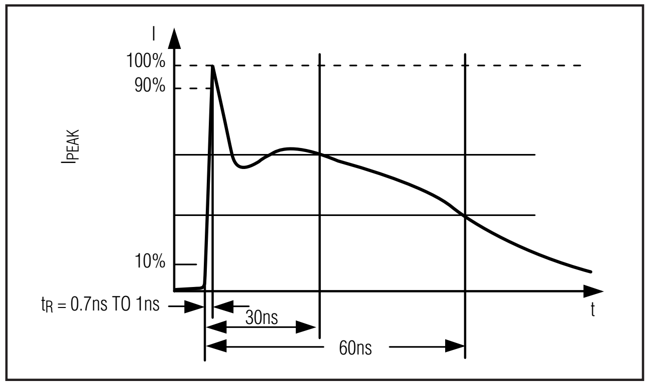


Figure 11d. IEC 61000-4-2 ESD Generator Current Waveform

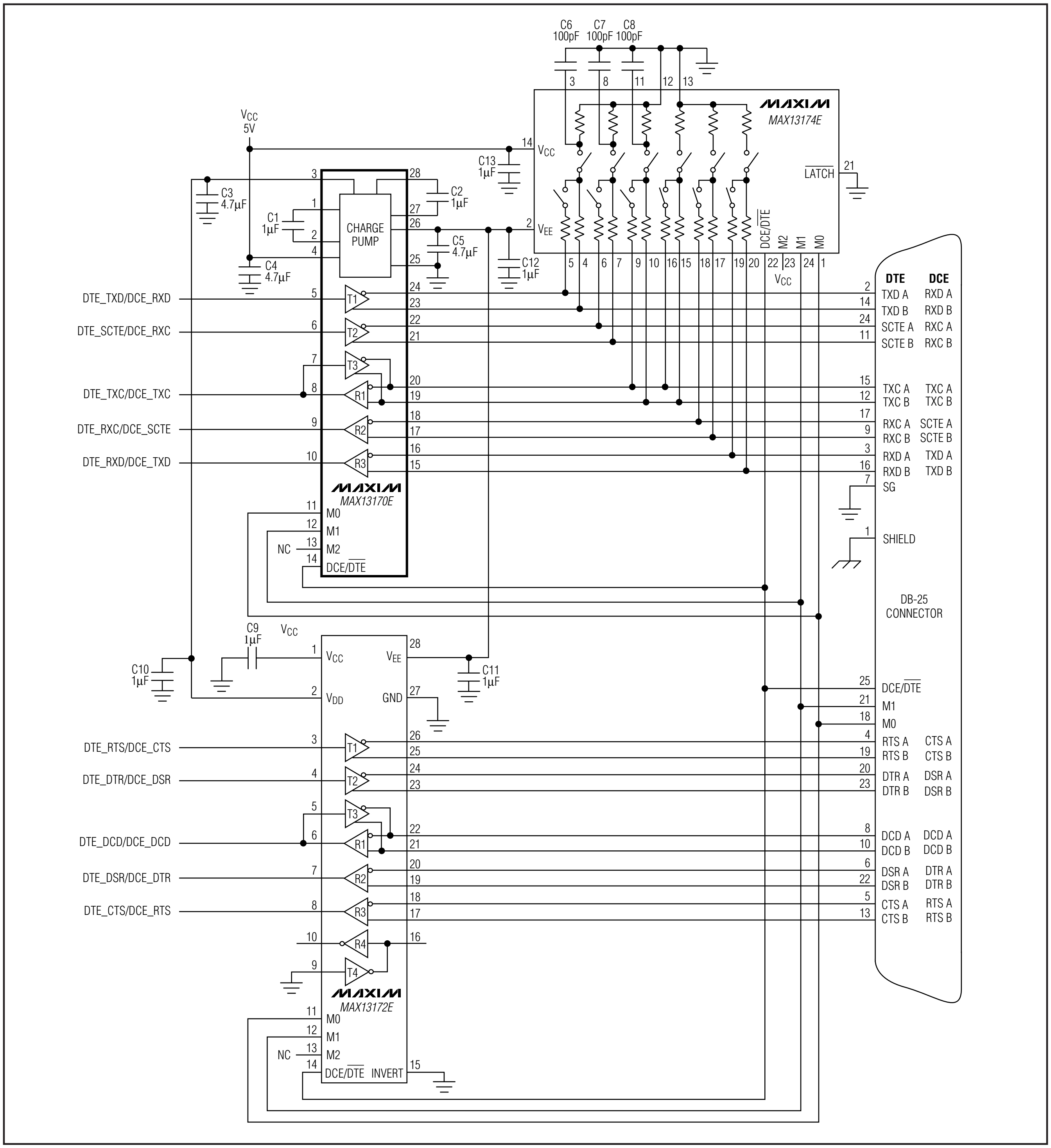


Figure 12. Cable-Selectable Multiprotocol DTE/DCE Port

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceiver

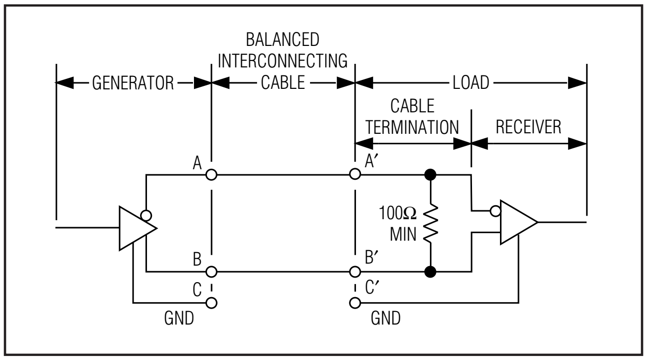


Figure 13. Typical V.11 Interface

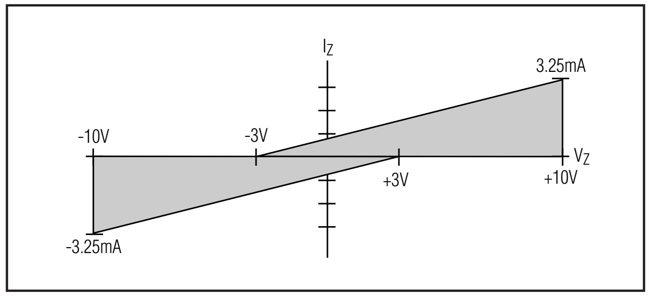


Figure 14. Receiver Input Impedance

Applications Information

Capacitor Selection

The capacitors used for the charge pumps, as well as for supply bypassing, should have a low equivalent series resistance (ESR) and low temperature coefficient. Multilayer ceramic capacitors with an X7R dielectric offer the best combination of performance, size, and cost. The flying capacitors (C1, C2) should have a value of 1µF, while the reservoir capacitors (C3, C5) and the bypass capacitor (C4) should have a minimum value of 4.7µF (Figure 10). To reduce the ripple present on the transmitter outputs, capacitors C3, C4, and C5 can be increased. The values of C1 and C2 should not be increased.

Bypassing

For best performance of the charge pumps, connect C3, C4, and C5 closer the device than C1 and C2.

Cable Termination

The MAX13174E software-selectable resistor network is designed to be used with the MAX13170E. The MAX13174E multiprotocol termination network provides V.11- and V.35-compliant termination, while V.28 receiver termination is internal to the MAX13170E. These cable termination networks provide compatibility with V.11, V.28, and V.35 protocols. Using the MAX13174E termination networks provide the advantage of not having to build expensive termination networks out of resistors and relays, manually changing termination modules, or building custom termination networks.

Cable-Selectable Mode

A cable-selectable multiprotocol interface is shown in Figure 12. The mode control lines M0, M1, and DCE/$\overline{\text{DTE}}$ are wired to the DB-25 connector. To select the serial interface mode, the appropriate combination of M0, M1, and DCE/$\overline{\text{DTE}}$ are grounded within the cable wiring. The control lines that are not grounded are pulled high by the internal pullups on the MAX13170E. The serial interface protocol of the MAX13170E, MAX13172E, and MAX13174E is selected based on the cable that is connected to the DB-25 interface.

V.11 Interface

As shown in Figure 13, the V.11 protocol is a fully balanced differential interface. The V.11 driver generates a minimum of ±2V between nodes A and B when a 100Ω (min) resistance is presented at the load. The V.11 receiver is sensitive to ±200mV differential signals at receiver inputs A' and B'. The V.11 receiver rejects common-mode signals developed across the cable (referenced from C to C') of up to ±7V, allowing for error-free reception in noisy environments. The receiver inputs must comply with the impedance curve shown in Figure 14.

For high-speed data transmission, the V.11 specification recommends terminating the cable at the receiver with a 100Ω resistor. This resistor, although not required, prevents reflections from corrupting transmitted data. In Figure 15, the MAX13174E is used to terminate the V.11 receiver. Internal to the MAX13174E, S1 is closed and S2 is open to present a 100Ω minimum differential resistance. The MAX13170E's internal V.28 termination is disabled by opening S3.

V.35 Interface

Figure 16 shows a fully-balanced, differential standard V.35 interface. The generator and the load must both present a 100Ω ±10Ω differential impedance and a 150Ω ±15Ω common-mode impedance as shown by the resistive T networks in Figure 15. The V.35 driver generates a current output (±11mA, typ) that develops an output voltage of ±550mV across the generator and load termination networks. The V.35 receiver is sensitive to ±200mV differential signals at receiver inputs A' and B'. The V.35 receiver rejects common-mode signals developed across the cable (referenced from C to C') of up to ±4V, allowing for error-free reception in noisy environments.

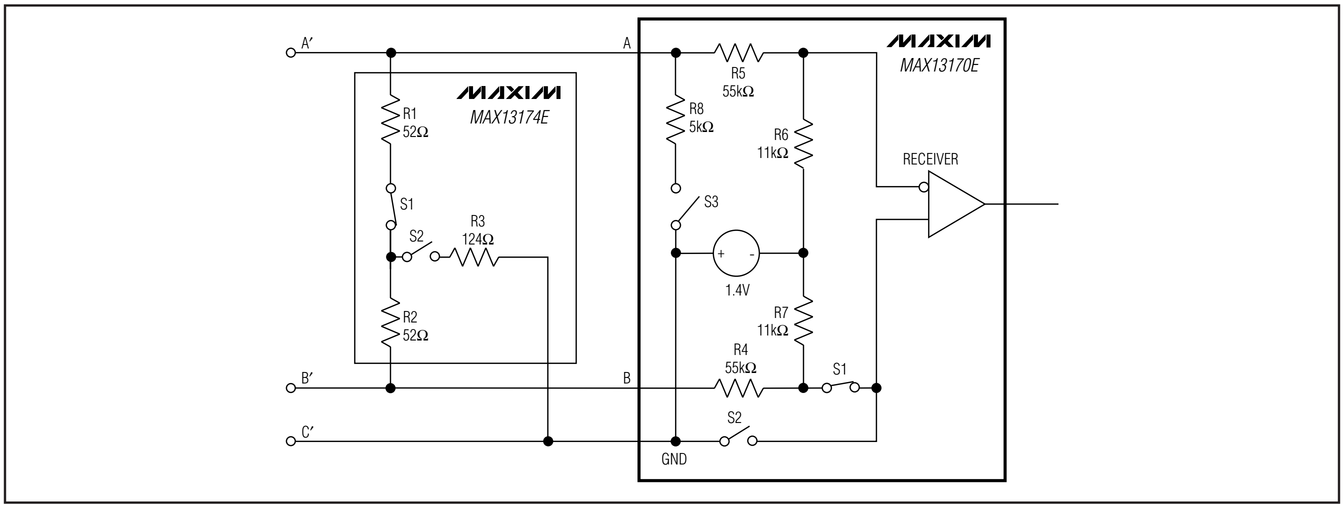


Figure 15. V.11 Termination and Internal Resistance Networks

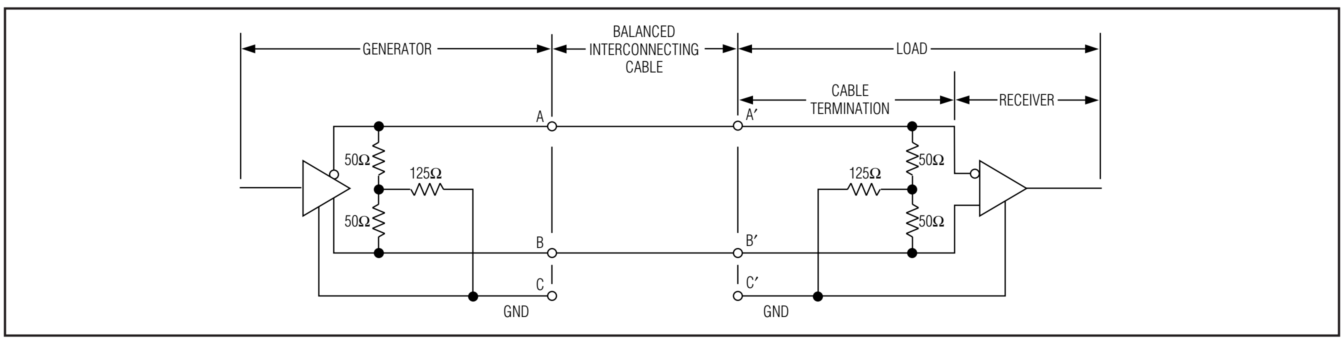


Figure 16. Typical V.35 Interface

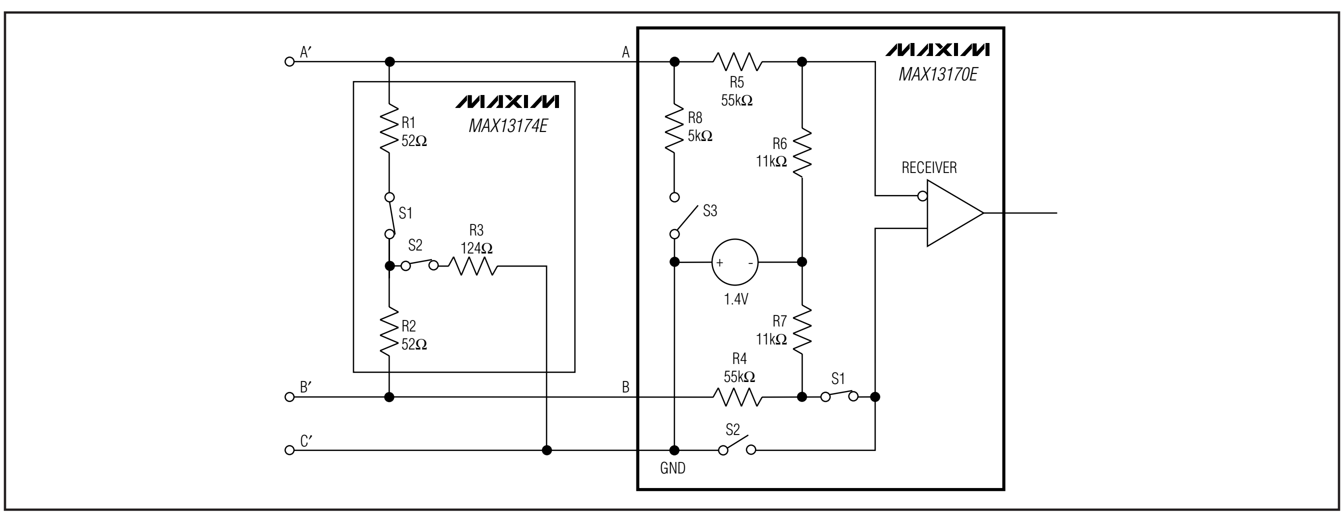


Figure 17. V.35 Termination and Internal Resistance Networks

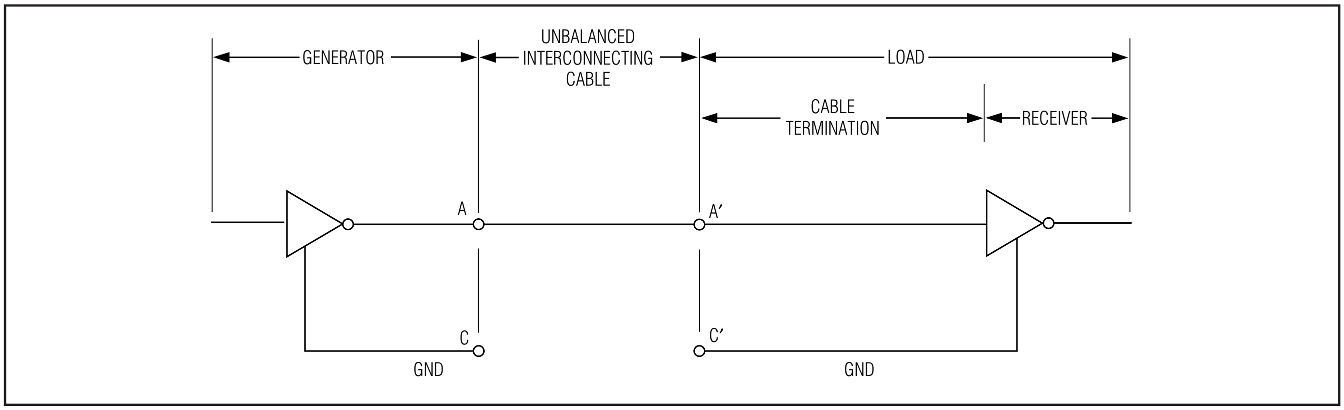


Figure 18. Typical V.28 Interface

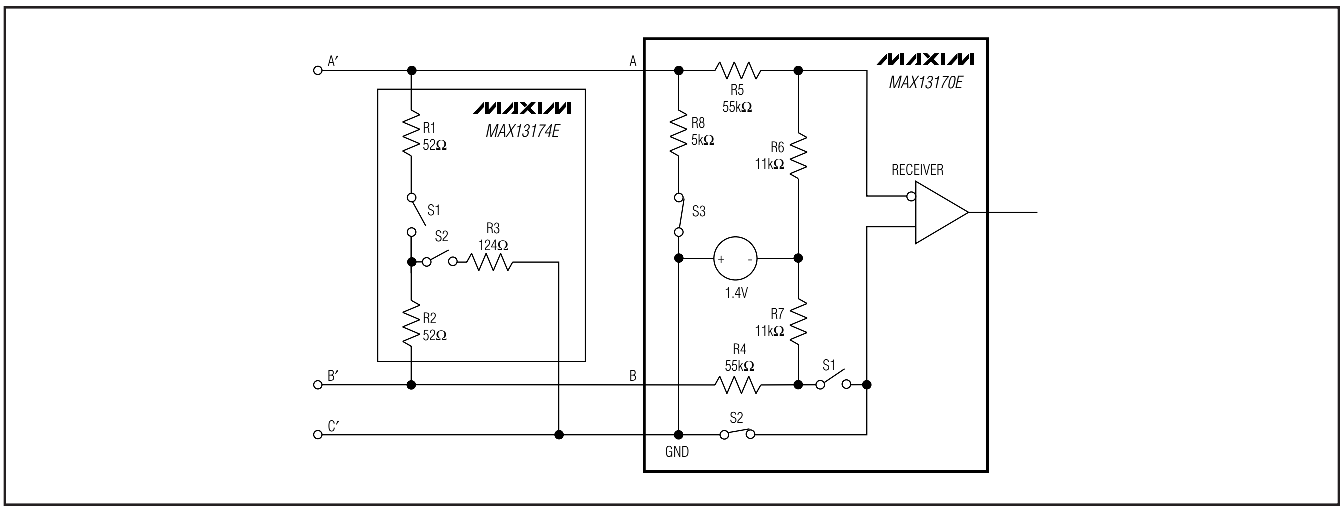


Figure 19. V.28 Termination and Internal Resistance Networks

In Figure 17, the MAX13174E is used to implement the resistive T network that is needed to properly terminate the V.35 driver and receiver. Internal to the MAX13174E, S1 and S2 are closed to connect the T-network resistors to the circuit. The V.28 termination resistor (internal to the MAX13170E) is disabled by opening S3 to avoid interference with the T-network impedance.

V.28 Interface

The V.28 interface is an unbalanced single-ended interface (Figure 18). The V.28 driver generates a minimum of ±5V across a 3kΩ load impedance between A' and C'. The V.28 receiver has a single-ended input. To aid in rejecting system noise, the MAX13170E's V.28 receiver has a typical hysteresis of 0.05V.

Figure 19 shows the MAX13174E's termination network disabled by opening S1 and S2. The MAX13170E's internal 5kΩ V.28 termination is enabled by closing S3.

DTE vs. DCE Operation

Figure 20 shows a DCE or DTE controller-selectable interface. DCE/$\overline{\text{DTE}}$ (pin 14) switches the port's mode of operation. See Table 1.

This application requires only one DB-25 connector, but separate cables for DCE or DTE signal routing. See Figure 20 for complete signal routing in DCE and DTE modes.

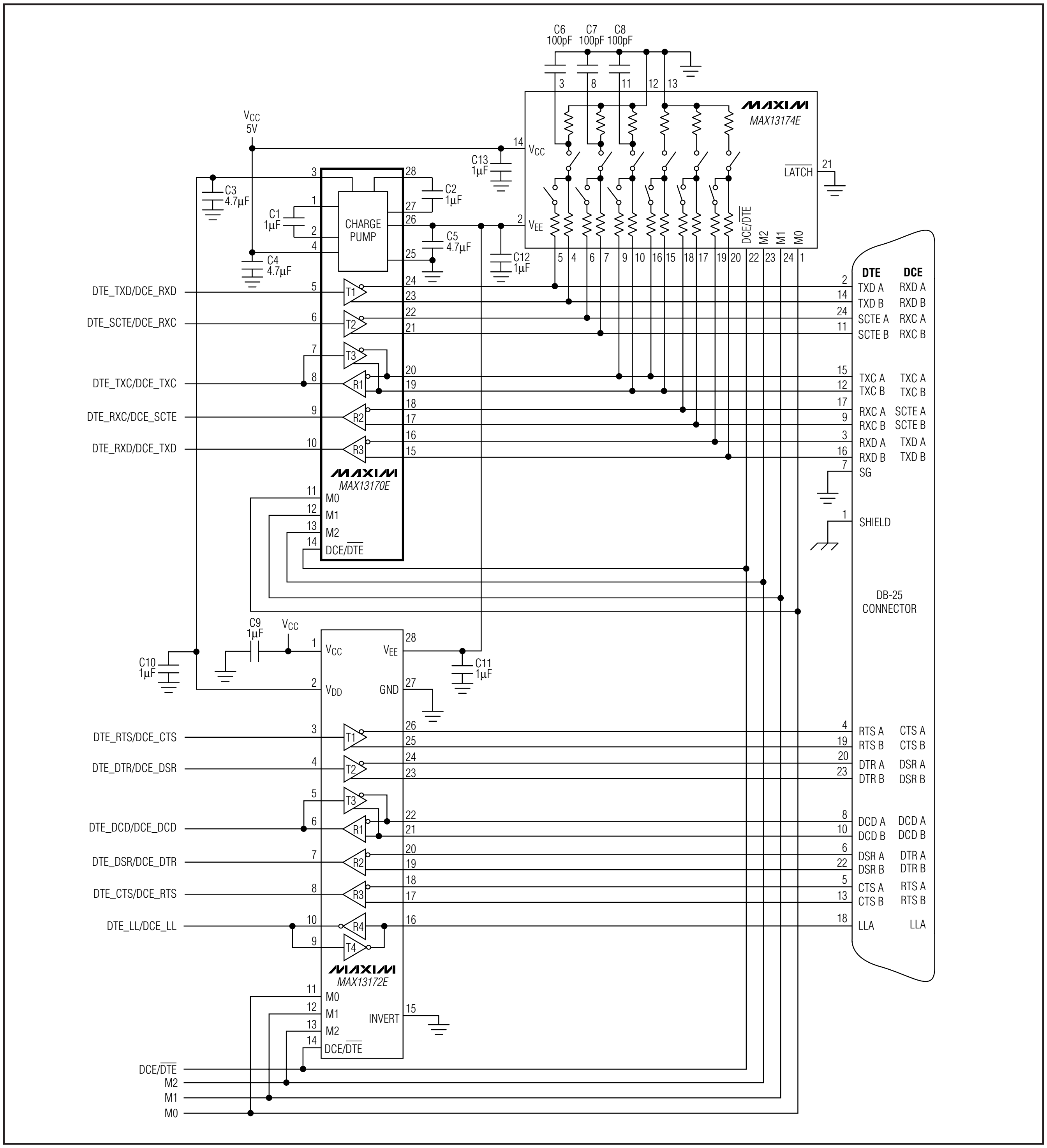


Figure 20. Multiprotocol DCE/DTE Port

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceiver

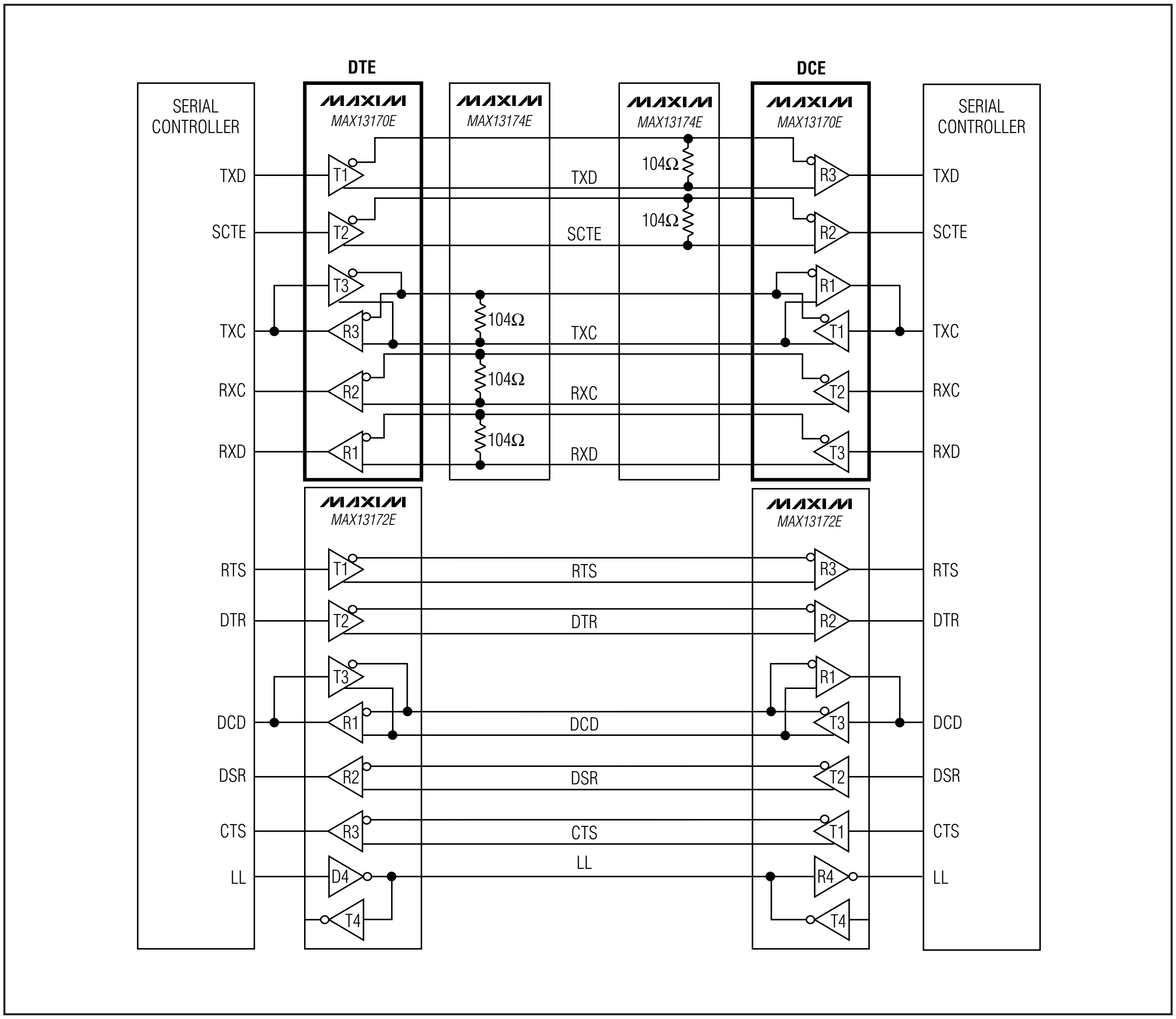


Figure 21. DCE-to-DTE X.21 Interface

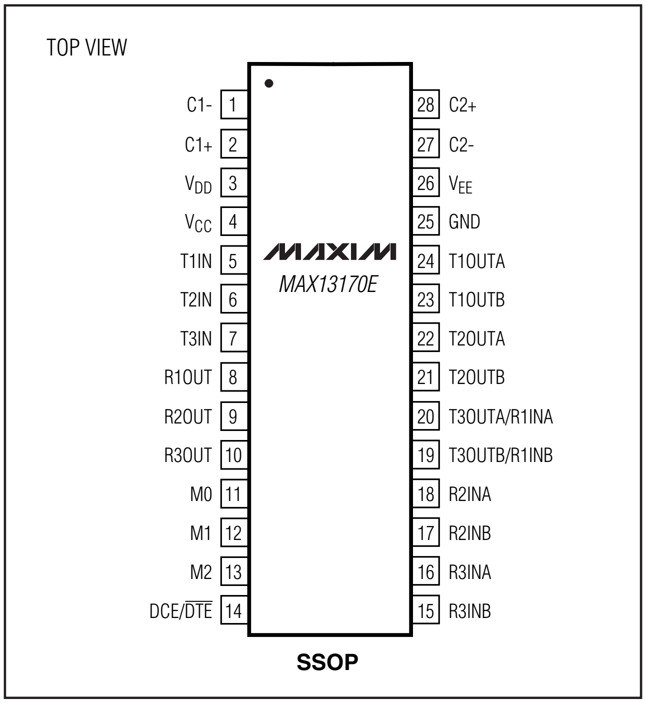
Complete Multiprotocol X.21 Interface

A complete DTE-to-DCE interface operating in X.21 mode is shown in Figure 21. The MAX13170E is used to generate the clock and data signals, and the MAX13172E generates the control signals and local loopback (LL). The MAX13174E is used to terminate the clock and data signals to support the V.11 protocol for cable termination. The control signals do not need external termination.

Compliance Testing

A European Standard EN 45001 test report is pending for the MAX13170E/MAX13172E/MAX13174E chipset. A copy of the test report will be available from Maxim upon completion.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 2619

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 SSOP	A28-2	21-0056

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