



## QUICK START PROCEDURE

Demonstration circuit 1856B-B is an easy way to evaluate the performance of the LTM4649EY. Please refer to Figure 1 for test setup connections and follow the procedure below.

1. With power off, place the jumpers in the following positions for a typical 1.8V<sub>OUT</sub> application:

JP8	JP7	JP9	JP2
TRACK/SS	RUN	MODE	V <sub>OUT</sub> Select
SS	ON	CCM	1.8V

2. Before connecting input supply, load and meters, preset the input voltage supply to be between 4.5V to 16V. Preset the load current to 0A.
3. With power off, connect the load, input voltage supply and meters as shown in Figure 1.
4. Turn on input power supply. The output voltage meter should display the selected output voltage  $\pm 2\%$ .

5. Once the proper output voltage is established, adjust the load current within the 0A to 10A range and observe the load regulation, efficiency, and other parameters. Output voltage ripple should be measured at J6 with a BNC cable and oscilloscope.
6. To observe increased light load efficiency place the mode pin jumper (JP9) in the Burst Mode<sup>®</sup> operation position. To observe increased light load efficiency with a reduced output ripple as compared to Burst Mode operation, place the mode pin jumper in the pulse-skipping position.
7. For optional load transient testing apply an adjustable positive pulse signal between IOSTEP CLK and GND pins. The pulse amplitude sets the load step current amplitude. The pulse width should be short ( $< 1\text{ms}$ ) and pulse duty cycle should be low ( $< 15\%$ ) to limit the thermal stress on the load transient circuit. The load step current can be monitored with a BNC connected to J5 (10mV/A).

**QUICK START PROCEDURE**

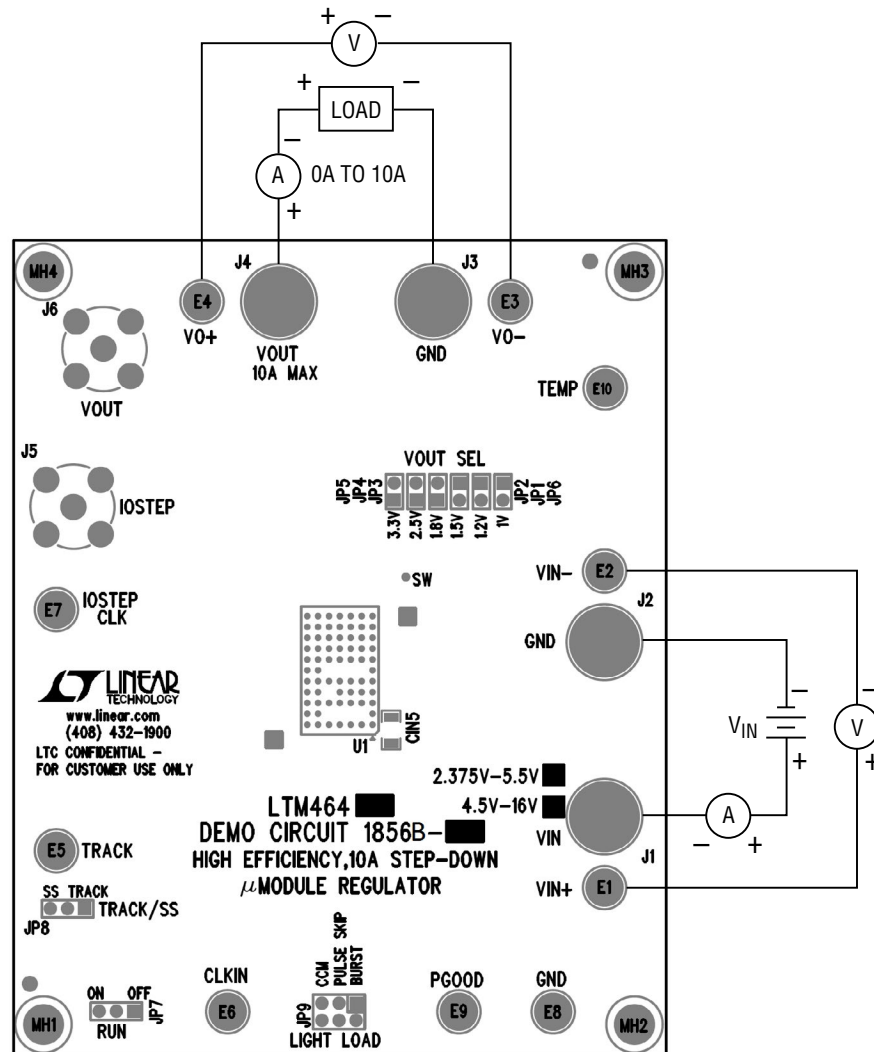


Figure 1. Test Setup of DC1856B-B

## QUICK START PROCEDURE

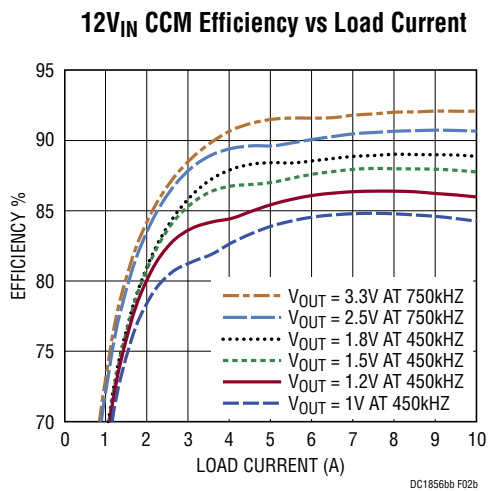
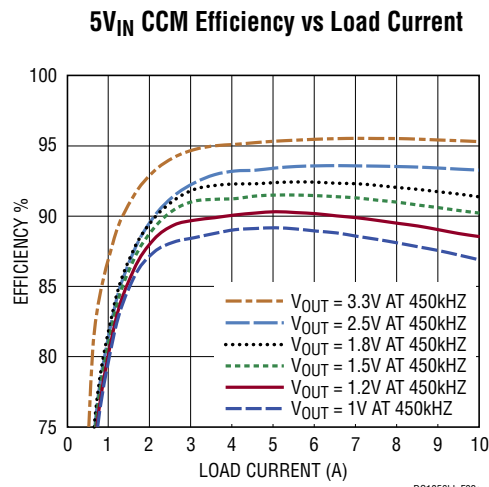
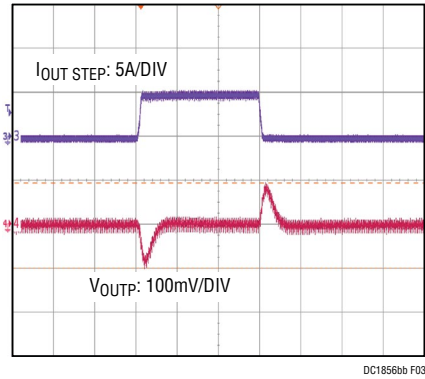


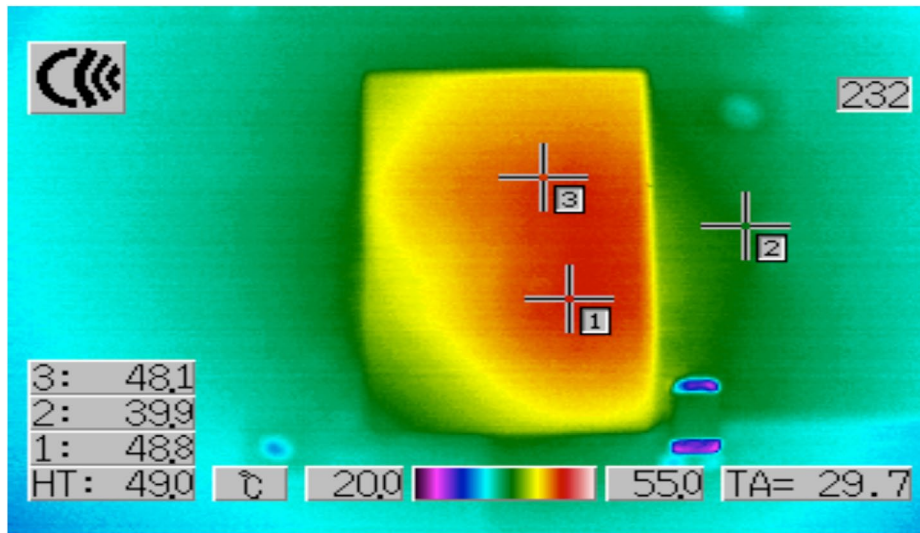
Figure 2. Measured Supply Efficiency at 5V<sub>IN</sub> and 12V<sub>IN</sub>

**QUICK START PROCEDURE**



$V_{IN}$ (V)	$V_{OUT}$ (V)	$C_{OUT}$ CERAMIC
12	1.5	2 × 220 $\mu$ F/4V Ceramic

**Figure 3. Measured Load Transient Response (5A to 10A Load Step)**



$V_{IN}$ (V)	$V_{OUT}$ (V)	$I_{OUT}$ (A)	AIRFLOW	AMBIENT (°C)
1.2	1.5	10	Natural Convection	29.7

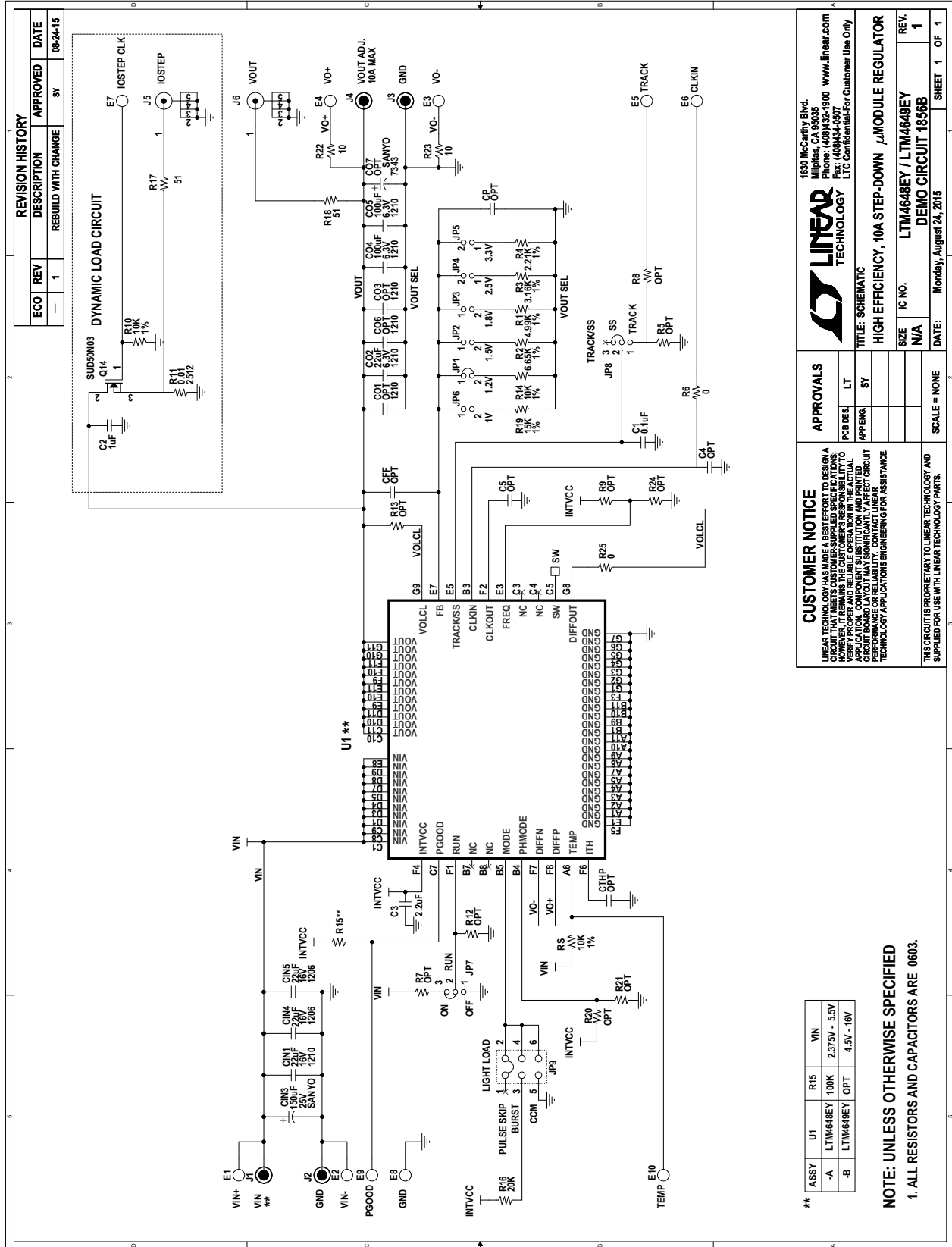
**Figure 4. Measured Thermal Capture**

# DEMO MANUAL DC1856B-B

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
<b>Required Circuit Components</b>				
1	2	C04, C05	CAP, 100µF, 20%, 6.3V, X5R, 1210	AVX, 12106D107MAT2A
2	1	C02	CAP, 22µF, 20%, 6.3V, X5R, 1210	AVX, 12106D226MAT2A
3	1	CIN1	CAP, 22µF, 20%, 16V, X7R, 1210	MURATA, GRM32ER71C226KE18L
4	1	CIN3	CAP, 150µF, 10%, 25V, OS-CON	SUN ELECT, 25HVH150MT
5	2	CIN4, CIN5	CAP, 22µF, 20%, 16V, X5R, 1206	TAIYO YUDEN, EMK316BJ226ML-T
6	2	R22, R23	RES, 10Ω, 5%, 1/10W, 0603	VISHAY, CRCW060310R0JNEA
7	1	R19	RES, 15kΩ, 1%, 1/10W, 0603	VISHAY, CRCW060315K0FKEA
8	1	C1	CAP, 0.1µF, 20%, 25V, X7R, 0603	AVX, 06033C104MAT2A
9	1	C3	CAP, 2.2µF, 20%, 10V, X5R, 0603	TAIYO YUDEN, LMK107BJ225MA-T
10	1	U1	IC, POWER MODULE	LINEAR TECHNOLOGY, LTM4649EY
<b>Additional Demo Board Circuit Components</b>				
1	0	C07	CAP, OPTION, 7343	OPTION
2	0	C01, C03, C06	CAP, OPTION, 1210	OPTION
3	1	C2	CAP, 1µF, 20%, 10V, X5R, 0603	TAIYO YUDEN, LMK107BJ105MA-T
4	0	C4, C5, CTHP, CP, CFF	CAP, OPTION, 0603	OPTION
5	1	R11	RES, 0.01Ω, 5%, 1W, 2512	PANASONIC, ERJ-M1WSF10MU
6	3	R10, R14, RS	RES, 10kΩ, 1%, 1/10W, 0603	VISHAY, CRCW060310K0FKEA
7	1	R16	RES, 20kΩ, 5%, 1/10W, 0603	VISHAY, CRCW060320K0JNEA
8	2	R17, R18	RES, 51Ω, 5%, 1/10W, 0603	VISHAY, CRCW060351R0JNEA
9	1	R15	RES, OPTION, 0603	OPTION
10	1	R1	RES, 4.99kΩ, 1%, 1/10W, 0603	VISHAY, CRCW06034K99FKEA
11	1	R2	RES, 6.65kΩ, 1%, 1/10W, 0603	VISHAY, CRCW06036K65FKEA
12	1	R3	RES, 3.16kΩ, 1%, 1/10W, 0603	VISHAY, CRCW06033K16FKEA
13	1	R4	RES, 2.21kΩ, 1%, 1/10W, 0603	VISHAY, CRCW06032K21FKEA
14	0	R5, R7, R8, R9, R12, R13, R20, R21, R24	RES, OPTION, 0603	OPTION
15	2	R6, R25	RES, 0Ω, JUMPER, 0603	VISHAY, CRCW06030000Z0EA
16	1	Q14	XSTR, MOSFET, N-CHANNEL, 30V	VISHAY, SUD50N04-8M8P-4GE3
<b>Hardware</b>				
1	10	E1 TO E10	TESTPOINT, TURRET 0.094"	MILL MAX, 2501-2-00-80-00-00-07-0
2	6	JP1, JP2, JP3, JP4, JP5, JP6	HEADER, 2PIN, 2mm	SULLIN, NRPN021PAEN-RC
3	2	JP7, JP8	HEADER, 3PIN, 2mm	SULLIN, NRPN031PAEN-RC
4	1	JP9	HEADER, 3X2 2mm	SULLIN, NRPN032PAEN-RC
5	4	J1, J2, J3, J4	JACK, BANANA	KEYSTONE, 575-4
6	2	J5, J6	CONN, BNC, 5 PINS	CONNEX, 112404
7	4	XJP1, XJP7, XJP8, XJP9	SHUNT, 2mm	SAMTEC, 2SN-BK-G
8	4		STANDOFF, SNAP ON	KEYSTONE_8834

**SCHEMATIC DIAGRAM**



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**TITLE: SCHEMATIC**  
**HIGH EFFICIENCY, 10A STEP-DOWN MODULE REGULATOR**

SIZE: N/A  
 IC NO.: LTM4648EY / LTM4648EY  
 REV.: 1

DATE: Monday, August 24, 2015  
 SHEET 1 OF 1

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**APPROVALS**  
 PCB DES: LT  
 APP'G: SY

SCALE = NONE

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

**NOTE: UNLESS OTHERWISE SPECIFIED**  
 1. ALL RESISTORS AND CAPACITORS ARE 0603.



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# DEMO MANUAL DC1856B-B

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