ALPHA & OMEGA SEMICONDUCTOR

# AOT5N100/AOTF5N100

## 1000V,4A N-Channel MOSFET

### General Description

The AOT5N100 & AOTF5N100 are fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications.By providing low $R_{DS(on)}$, $C_{iss}$ and $C_{rss}$ along with guaranteed avalanche capability this parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number: AOT5N100L & AOTF5N100L

### Product Summary

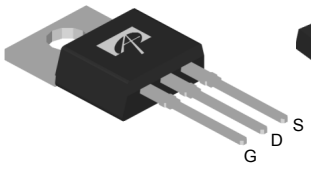
| | |
|---|---|
| $V_{DS}$ | 1100@150℃ |
| $I_D$ (at $V_{GS}$=10V) | 4A |
| $R_{DS(ON)}$ (at $V_{GS}$=10V) | < 4.2Ω |

100% UIS Tested
100% $R_g$ Tested

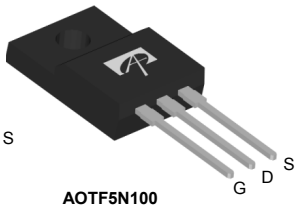
RoHS Compliant

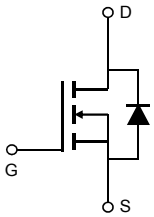
Top View

TO-220 AOT5N100




TO-220F AOTF5N100




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | AOT5N100 | AOTF5N100 | Units |
|---|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 1000 | | V |
| Gate-Source Voltage | | $V_{GS}$ | ±30 | | V |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | 4 | 4* | A |
| | $T_C$=100°C | | 2.5 | 2.5* | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 15 | | |
| Avalanche Current [C] | | $I_{AR}$ | 2.8 | | A |
| Repetitive avalanche energy [C] | | $E_{AR}$ | 117 | | mJ |
| Single pulsed avalanche energy [G] | | $E_{AS}$ | 235 | | mJ |
| Peak diode recovery dv/dt | | dv/dt | 5 | | V/ns |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 195 | 42 | W |
| | Derate above 25°C | | 1.6 | 0.3 | W/ °C |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | | °C |
| Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds | | $T_L$ | 300 | | °C |

**Thermal Characteristics**

| Parameter | Symbol | AOT5N100 | AOTF5N100 | Units |
|---|---|---|---|---|
| Maximum Junction-to-Ambient [A,D] | $R_{\theta JA}$ | 65 | 65 | °C/W |
| Maximum Case-to-sink [A] | $R_{\theta CS}$ | 0.5 | -- | °C/W |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 0.64 | 3 | °C/W |

* Drain current limited by maximum junction temperature.

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V, $T_J$=25°C | 1000 | | | V |
| | | $I_D$=250µA, $V_{GS}$=0V, $T_J$=150°C | | 1100 | | |
| $BV_{DSS}$ /ΔTJ | Breakdown Voltage Temperature Coefficient | $I_D$=250µA, $V_{GS}$=0V | | 1.04 | | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=1000V, $V_{GS}$=0V | | | 1 | µA |
| | | $V_{DS}$=800V, $T_J$=125°C | | | 10 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±30V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=5V, $I_D$=250µA | 3.3 | 3.9 | 4.5 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=2.5A | | 3.5 | 4.2 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=40V, $I_D$=2.5A | | 5 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.73 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 4 | A |
| $I_{SM}$ | Maximum Body-Diode Pulsed Current | | | | 15 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=25V, f=1MHz | 750 | 950 | 1150 | pF |
| $C_{oss}$ | Output Capacitance | | 40 | 62 | 85 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 3.5 | 6 | 9 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 2 | 4.3 | 6.5 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=800V, $I_D$=5A | 15 | 19 | 23 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 4.6 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 6.5 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=500V, $I_D$=5A, $R_G$=25Ω | | 27 | | ns |
| $t_r$ | Turn-On Rise Time | | | 40 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 50 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 33 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=5A,dI/dt=100A/µs,$V_{DS}$=100V | 350 | 450 | 550 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=5A,dI/dt=100A/µs,$V_{DS}$=100V | 4.2 | 5.5 | 6.8 | µC |

A. The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A$=25° C.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C, Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. L=60mH, $I_{AS}$=2.8A, $V_{DD}$=150V, $R_G$=25Ω, Starting $T_J$=25° C

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

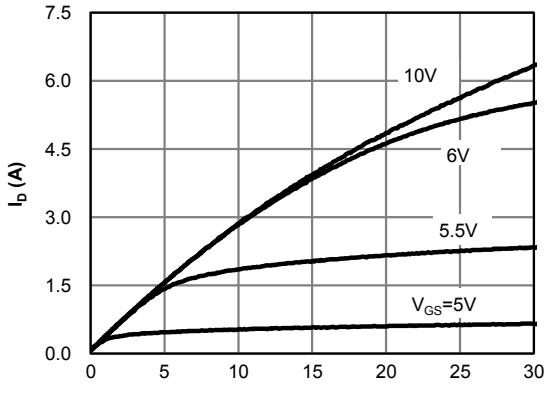



Fig 1: On-Region Characteristics

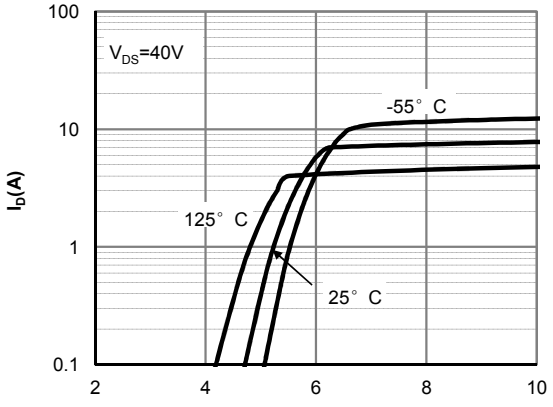



Figure 2: Transfer Characteristics

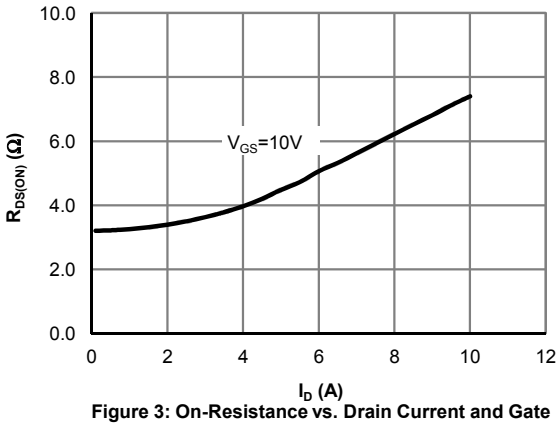



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

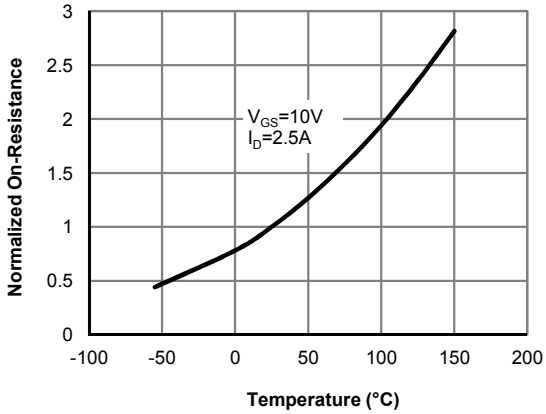



Figure 4: On-Resistance vs. Junction Temperature

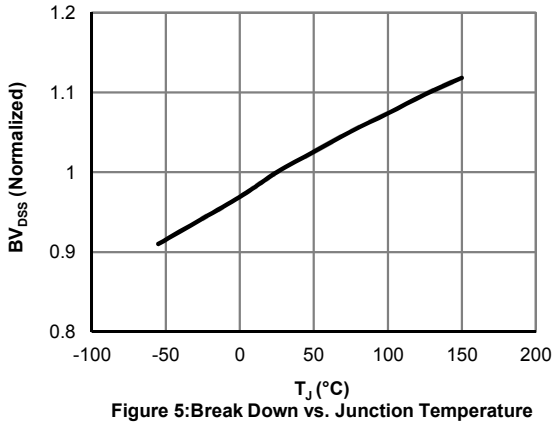



Figure 5:Break Down vs. Junction Temperature

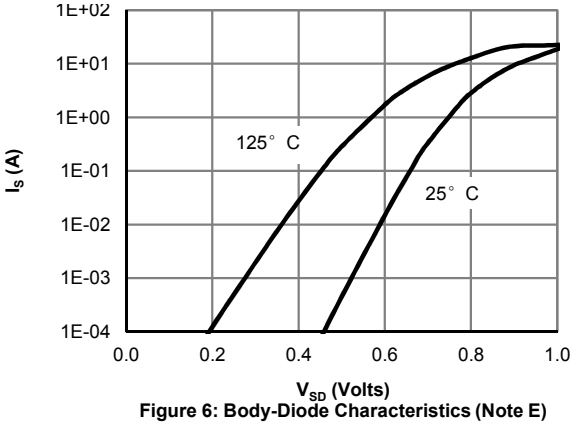



Figure 6: Body-Diode Characteristics (Note E)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

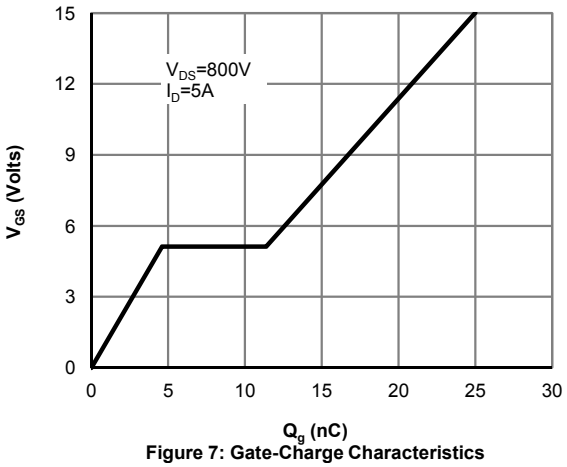



**Figure 7: Gate-Charge Characteristics**

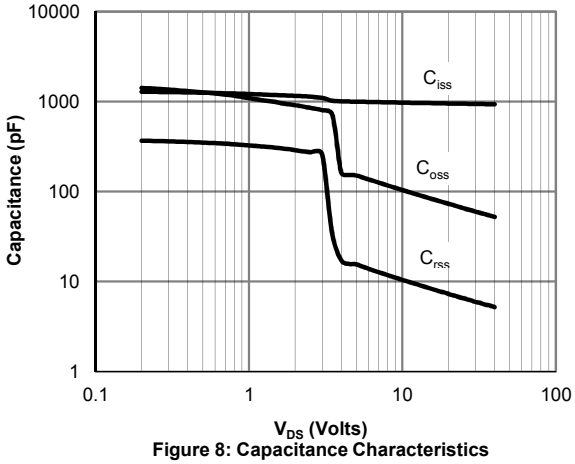



**Figure 8: Capacitance Characteristics**

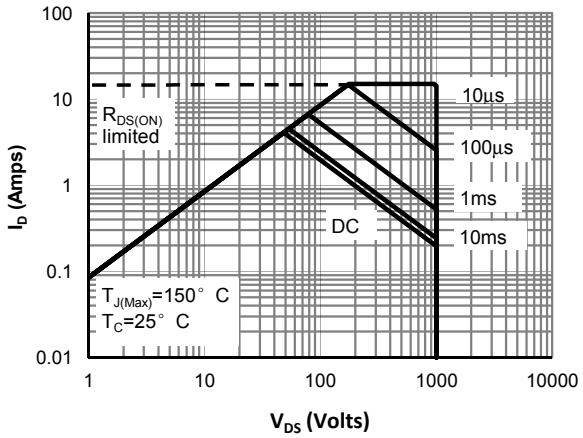



**Figure 9: Maximum Forward Biased Safe Operating Area for AOT5N100 (Note F)**

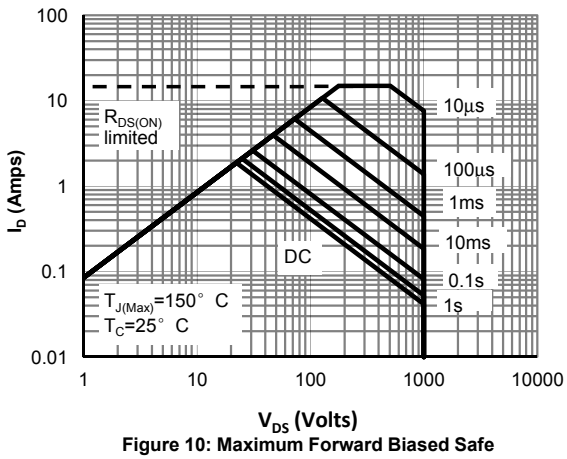



**Figure 10: Maximum Forward Biased Safe Operating Area for AOTF5N100 (Note F)**

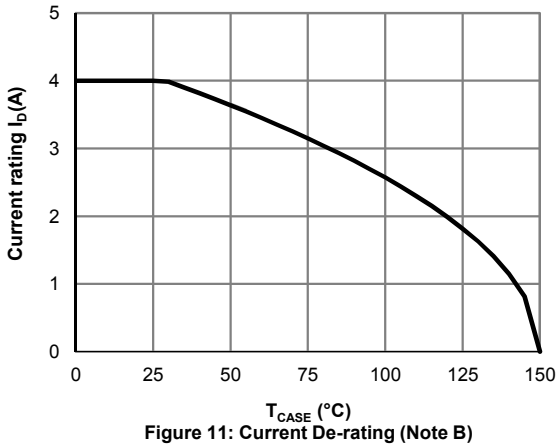



**Figure 11: Current De-rating (Note B)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

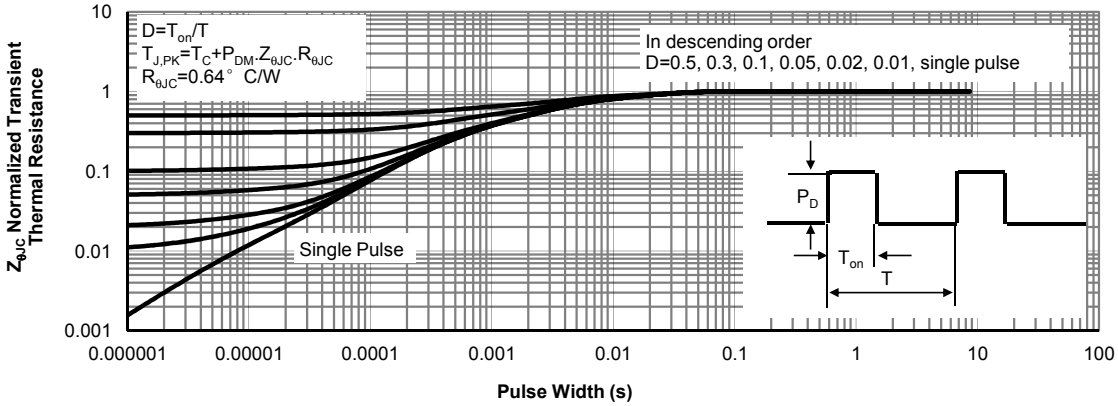



**Figure 12: Normalized Maximum Transient Thermal Impedance for AOT5N100 (Note F)**

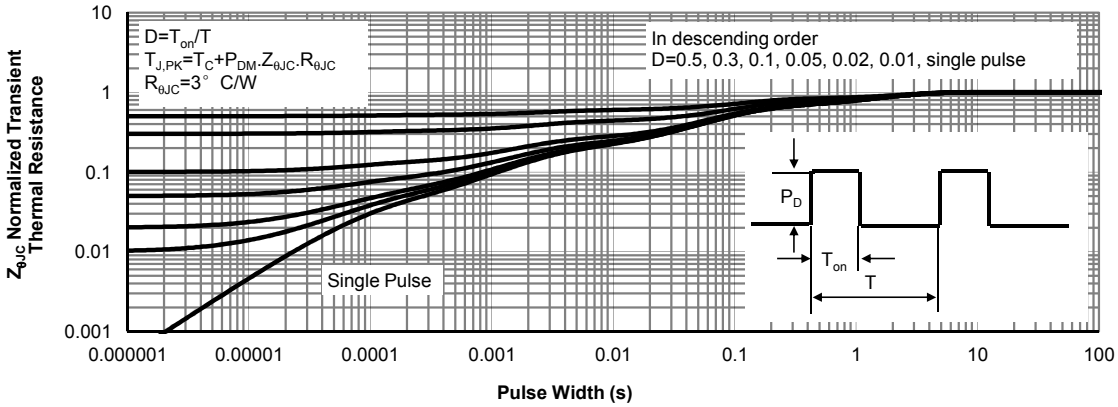
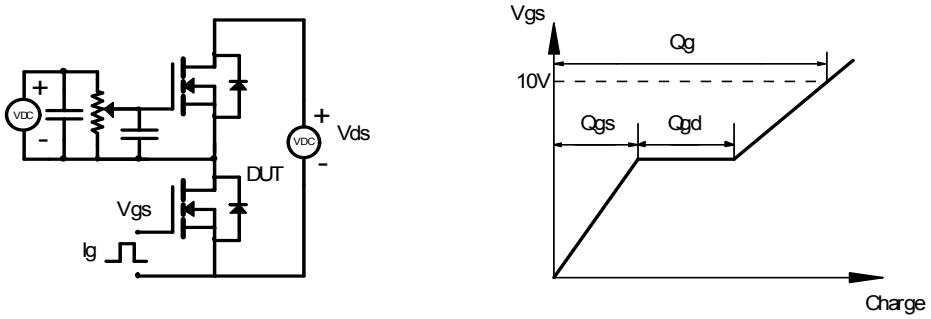
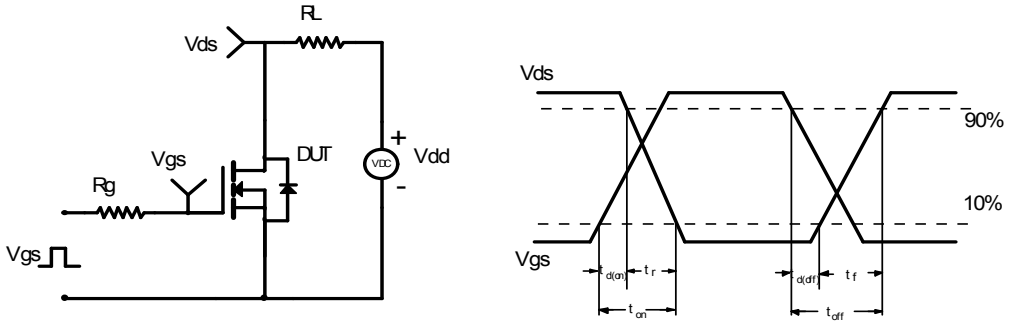



**Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF5N100 (Note F)**

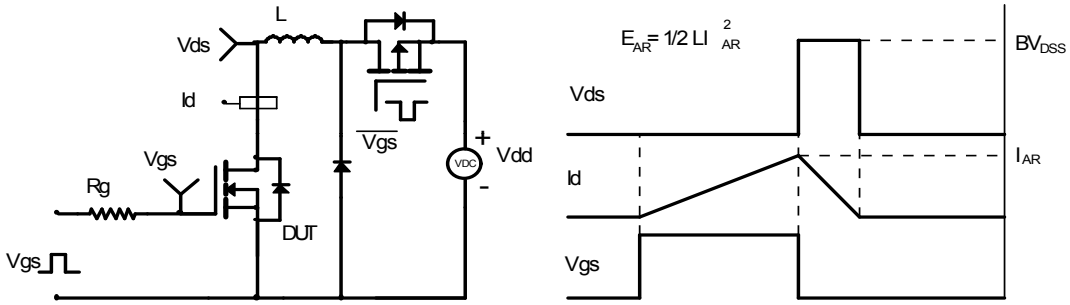
## Gate Charge Test Circuit & Waveform




## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms