

DATA SHEET

**TDA1562Q; TDA1562ST;
TDA1562SD**

**70 W high efficiency power
amplifier with diagnostic facility**

Preliminary specification
Supersedes data of 1998 Apr 07

2003 Feb 12

70 W high efficiency power amplifier with diagnostic facility

TDA1562Q; TDA1562ST;
TDA1562SD

FEATURES

- Very high output power, operating from a single low supply voltage
- Low power dissipation, when used for music signals
- Switches to low output power at too high case temperatures
- Few external components
- Fixed gain
- Differential inputs with high common mode rejection
- Mode select pin (on, mute and standby)
- Status I/O pin (class-H, class-B and fast mute)
- All switching levels with hysteresis
- Diagnostic pin with information about:
 - Dynamic Distortion Detector (DDD)
 - Any short-circuit at outputs
 - Open load detector
 - Temperature protection.
- No switch-on or switch-off plops

- Fast mute on supply voltage drops
- Quick start option (e.g. car-telephony/navigation)
- Low (Δ) offset voltage at the outputs
- Load dump protection
- Short-circuit safe to ground, supply voltage and across the load
- Low power dissipation in any short-circuit condition
- Protected against electrostatic discharge
- Thermally protected
- Flexible leads.

GENERAL DESCRIPTION

The TDA1562 is a monolithic integrated 70 W/4 Ω Bridge-Tied Load (BTL) class-H high efficiency power amplifier in a 17 lead DIL-bent-SIL plastic power package.

The device can be used for car audio systems (e.g. car radios and boosters) as well as mains fed applications (e.g. midi/mini audio combinations and TV sound).

QUICK REFERENCE DATA

$V_P = 14.4$ V; $R_L = 4$ Ω ; $R_S = 0$ Ω ; $f = 1$ kHz; $T_{amb} = 25$ $^{\circ}$ C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	operating; note 1	8	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_q	quiescent current	on and mute; $R_L =$ open circuit	–	110	150	mA
I_{stb}	standby current	standby	–	3	50	μ A
$ V_{OO} $	output offset voltage	on and mute	–	–	100	mV
$ \Delta V_{OO} $	delta output offset voltage	on \leftrightarrow mute	–	–	30	mV
G_v	voltage gain		25	26	27	dB
$ Z_{i(dif)} $	differential input impedance		90	150	–	k Ω
P_o	output power	THD = 0.5%	45	55	–	W
		THD = 10%	60	70	–	W
THD	total harmonic distortion	$P_o = 1$ W	–	0.03	–	%
		$P_o = 20$ W	–	0.06	–	%
		DDD active	–	2.1	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	on and mute	55	63	–	dB
CMRR	common mode rejection ratio	on	56	80	–	dB
ISRR	input signal rejection ratio	mute	80	100	–	dB
$V_{n(o)}$	noise output voltage	on	–	100	150	μV

Note

- When operating at $V_P > 16\text{ V}$, the output power must be limited to 85 W at THD = 10% (or minimum load is 6 Ω).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1562Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1
TDA1562Q/S10	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 7.7 mm)	SOT243-3
TDA1562ST	RDBS17P	plastic rectangular-DIL-bent-SIL power package; 17 leads (row spacing 2.54 mm)	SOT577-2
TDA1562SD	RDBS17P	plastic rectangular-DIL-bent-SIL (reverse bent) power package; 17 leads (row spacing 2.54 mm)	SOT668-2

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BLOCK DIAGRAM

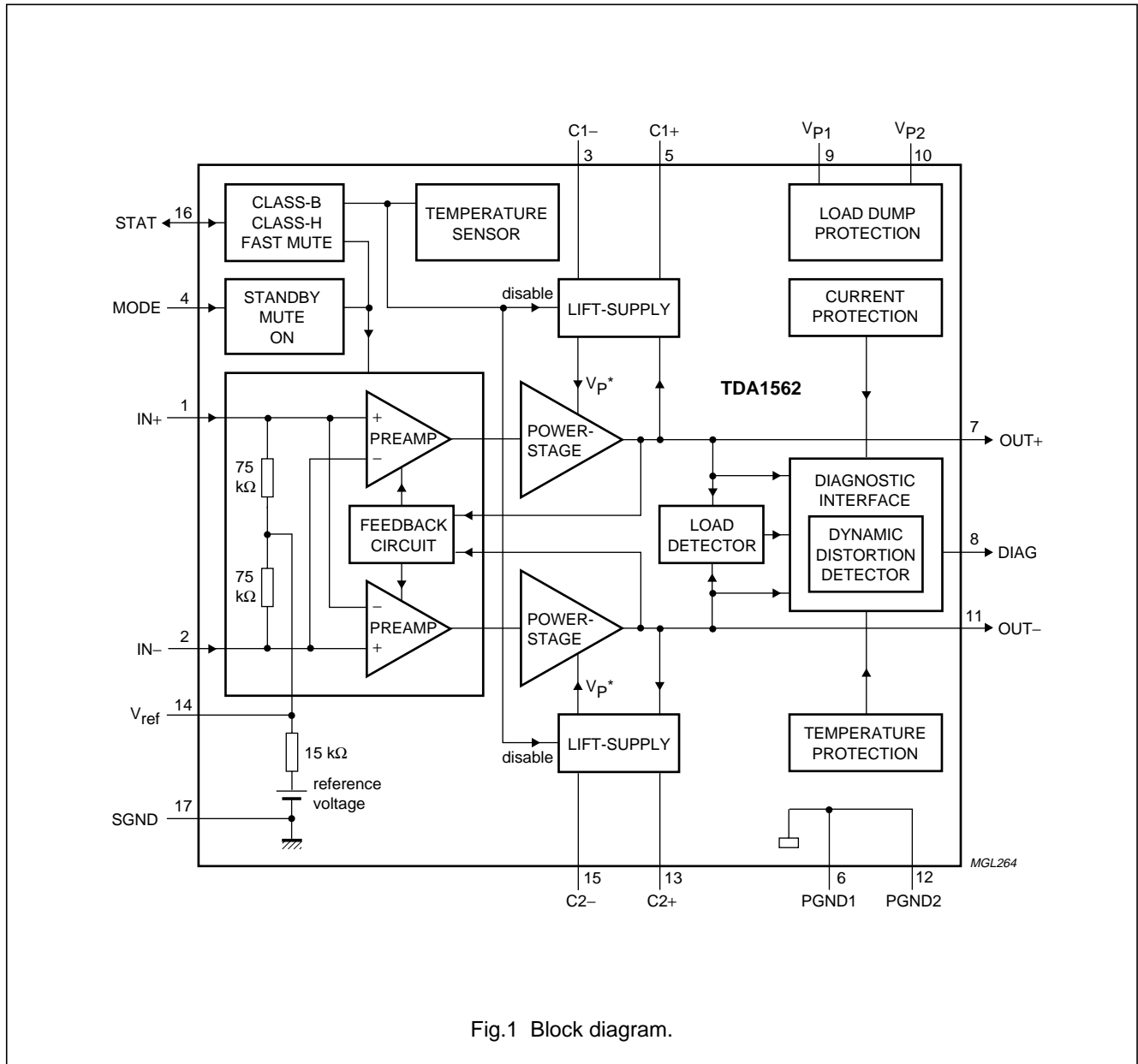


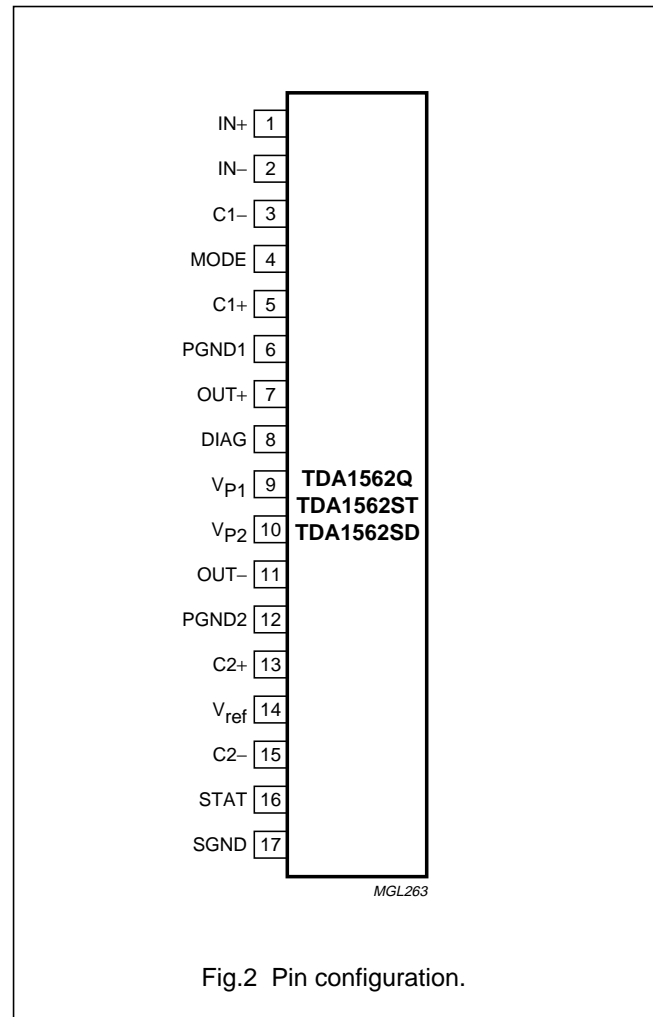
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
IN+	1	signal input (positive)
IN-	2	signal input (negative)
C1-	3	negative terminal of lift electrolytic capacitor 1
MODE	4	mode select input
C1+	5	positive terminal of lift electrolytic capacitor 1
PGND1	6	power ground 1
OUT+	7	positive output
DIAG	8	diagnostic output (open-collector)
V _{P1}	9	supply voltage 1
V _{P2}	10	supply voltage 2
OUT-	11	negative output
PGND2	12	power ground 2
C2+	13	positive terminal of lift electrolytic capacitor 2
V _{ref}	14	internal reference voltage
C2-	15	negative terminal of lift electrolytic capacitor 2
STAT	16	status I/O
SGND	17	signal ground



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FUNCTIONAL DESCRIPTION

The TDA1562 contains a mono class-H BTL output power amplifier. At low output power, up to 18 W, the device operates as a normal BTL amplifier. When a larger output voltage swing is required, the internal supply voltage is lifted by means of the external electrolytic capacitors. Due to this momentarily higher supply voltage the obtainable output power is 70 W.

In normal use, when the output is driven with music-like signals, the high output power is only needed during a small percentage of time. Under the assumption that a music signal has a normal (Gaussian) amplitude distribution, the reduction in dissipation is about 50% when compared to a class-B output amplifier with the same output power. The heatsink should be designed for use with music signals. If the case temperature exceeds 120 °C the device will switch back from class-H to class-B operation. The high power supply voltage is then disabled and the output power is limited to 20 W.

When the supply voltage drops below the minimum operating level, the amplifier will be muted immediately.

Mode select input (pin MODE)

This pin has 3 modes:

1. LOW for standby: the complete circuit is switched off, the supply current is very low
2. MID for mute: the circuit is switched on, but the input signal is suppressed
3. HIGH for on: normal operation, the input signal is amplified by 26 dB.

When the circuit is switched from mute to on or vice versa the actual switching takes place at a zero crossing of the input signal. The circuit contains a quick start option, i.e. when it is switched directly from standby to on, the amplifier is fully operational within 50 ms (important for applications like car telephony and car navigation).

Status I/O (pin STAT)

INPUT

This input has 3 possibilities:

1. LOW for fast mute: the circuit remains switched on, but the input signal is suppressed
2. MID for class-B: the circuit operates as class-B amplifier, the high power supply voltage is disabled, independent of the case temperature
3. HIGH for class-H: the circuit operates as class-H amplifier, the high power supply voltage is enabled, independent of the case temperature.

When the circuit is switched from fast mute to class-B/H or vice versa the switching is immediately carried out. When the circuit is switched from class-B to class-H or vice versa the actual switching takes place at a zero crossing of the input signal.

OUTPUT

This output has 3 possibilities:

1. LOW for mute: acknowledge of muted amplifier
2. MID for class-B: the circuit operates as class-B amplifier, the high power supply voltage is disabled, caused by the case temperature $T_c > 120\text{ °C}$
3. HIGH for class-H: the circuit operates as class-H amplifier, the high power supply voltage is enabled, because the case temperature $T_c < 120\text{ °C}$.

When the circuit is switched from class-B to class-H or vice versa the actual switching takes place at a zero crossing of the input signal.

The status I/O pins of maximum 8 devices may be tied together for synchronizing purposes.

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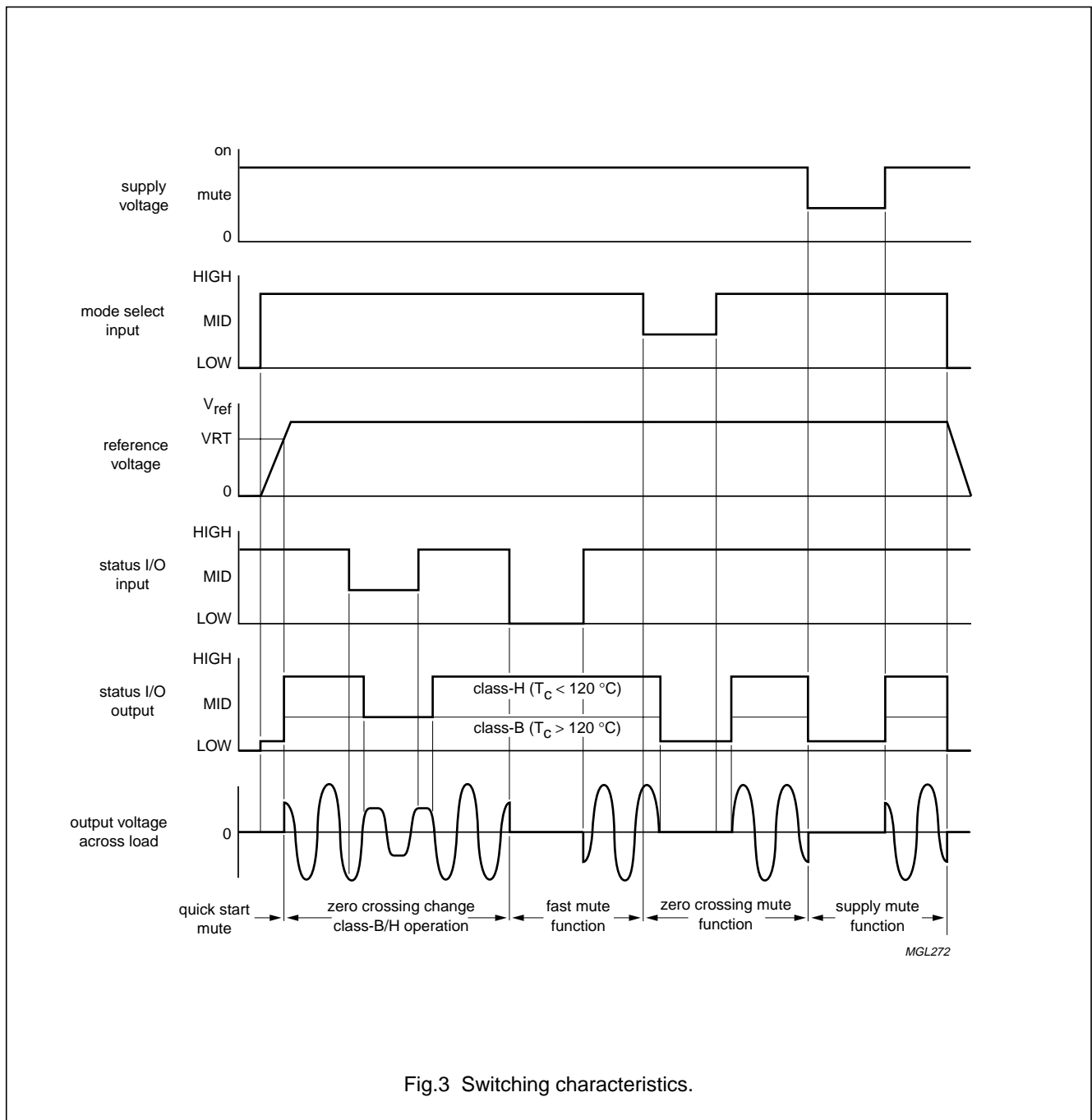


Fig.3 Switching characteristics.

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Diagnostic output (pin DIAG)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of the output stages, the DDD becomes active. This information can be used to drive a sound processor or DC-volume control to attenuate the input signal and so limit the distortion.

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at the outputs to ground or to the supply voltage, the output stages are switched off. They will be switched on again approximately 20 ms after removing the short-circuit. During this short-circuit condition the diagnostic output is continuously LOW.

When a short-circuit occurs across the load, the output stages are switched off during approximately 20 ms. After that time is checked during approximately 50 μ s whether the short-circuit is still present. During this short-circuit condition the diagnostic output is LOW for 20 ms and HIGH for 50 μ s. The power dissipation in any short-circuit condition is very low.

TEMPERATURE DETECTION

Just before the temperature protection becomes active the diagnostic output becomes continuously LOW.

LOAD DETECTION

Directly after the circuit is switched from standby to mute or on, a built-in detection circuit checks whether a load is present. The results of this check can be detected at the diagnostic output, by switching the mode select input in the mute mode.

Since the diagnostic output is an open-collector output, more devices can be connected.

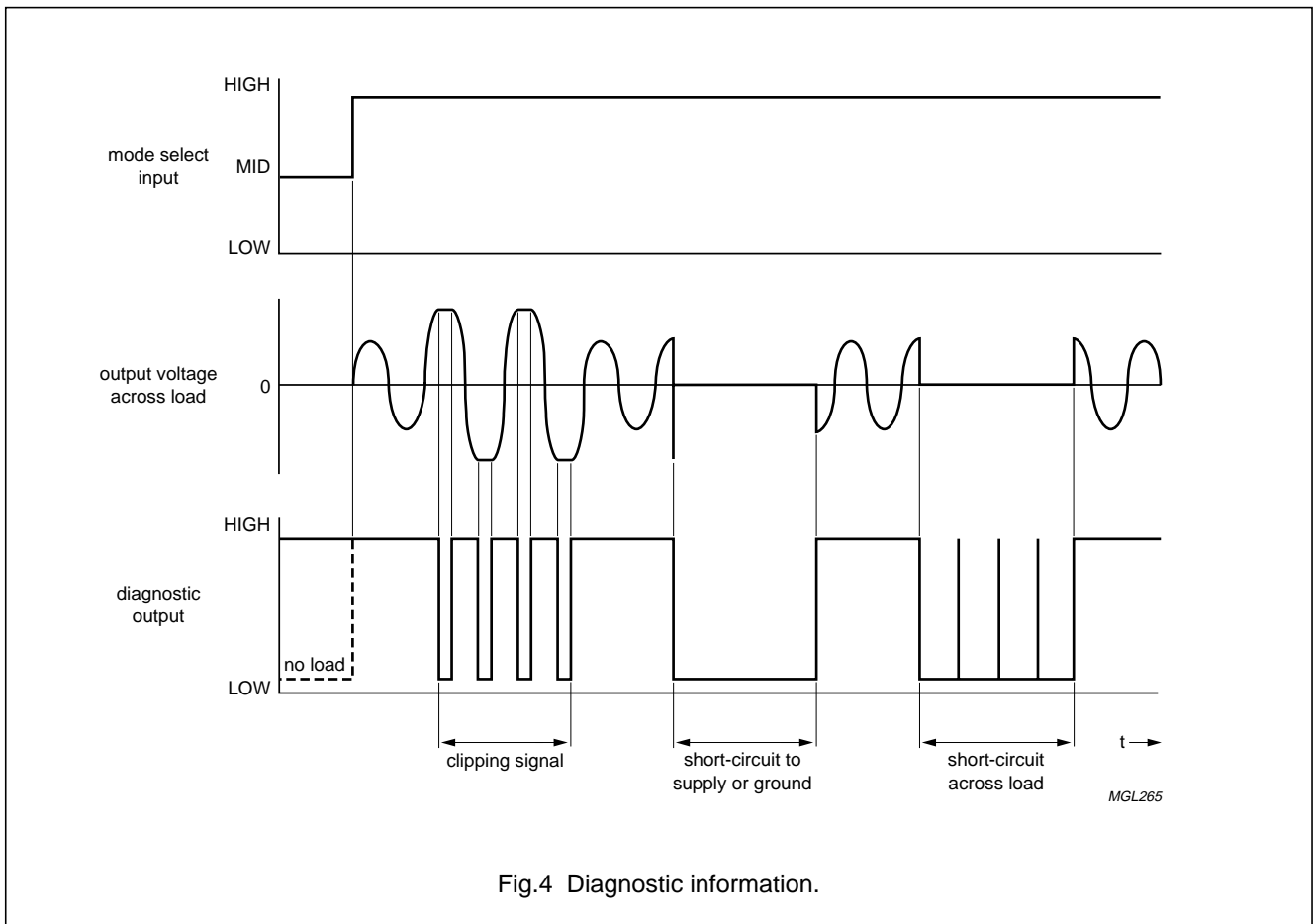


Fig.4 Diagnostic information.

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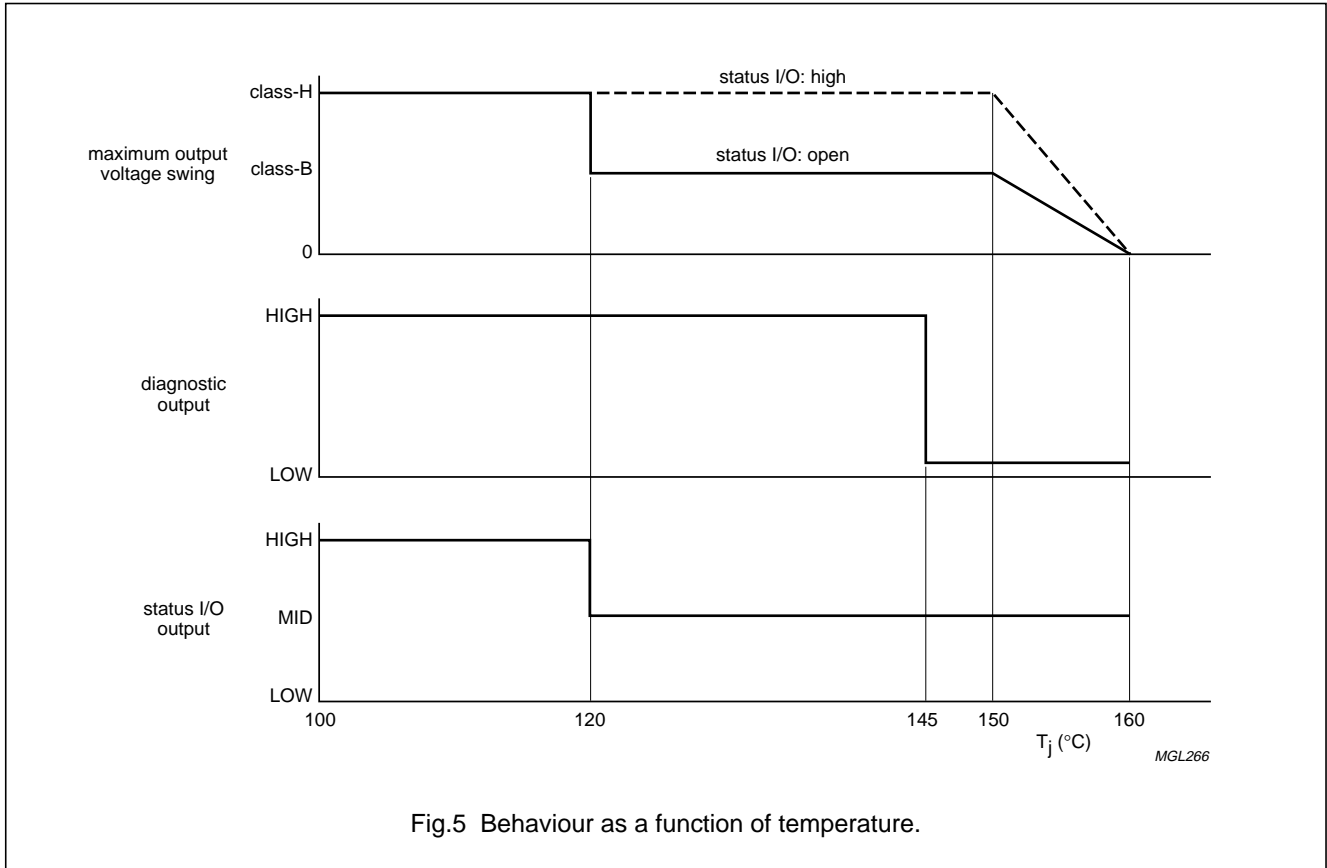


Fig.5 Behaviour as a function of temperature.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating; note 1	–	18	V
		non-operating	–	30	V
		load dump; $t_r > 2.5$ ms; $t = 50$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	10	A
I_{ORM}	repetitive peak output current		–	8	A
V_{sc}	short-circuit safe voltage		–	18	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	–	°C
T_j	junction temperature	note 2	–	150	°C
P_{tot}	total power dissipation		–	60	W

Notes

- When operating at $V_P > 16$ V, the output power must be limited to 85 W at THD = 10% (or minimum load is 6 Ω).
- T_j is a theoretical temperature which is based on a simplified representation of the thermal behaviour of the device. $T_j = T_c + P \times R_{th(j-c)}$, where $R_{th(j-c)}$ is a fixed value to be used for the calculation of T_j . The rating for T_j limits the allowable combinations of power dissipation P and case temperature T_c (in accordance with IEC 60747-1).

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QUALITY SPECIFICATION

Quality in accordance with "SNW-FQ-611D", if this type is used as an audio amplifier.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

DC CHARACTERISTICS

$V_P = 14.4$ V; $R_L = 4$ Ω ; $T_{amb} = 25$ °C; measurements in accordance with Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies V_{P1} and V_{P2}						
V_P	supply voltage		8	14.4	18	V
$V_{P(th+)}$	supply threshold voltage	mute \rightarrow on	7	–	9	V
$V_{P(th-)}$	supply threshold voltage	on \rightarrow mute	7	–	9	V
$V_{P(H1)}$	hysteresis $ (V_{th+} - V_{th-}) $		–	200	–	mV
I_q	quiescent current	on and mute; $R_L =$ open circuit	–	110	150	mA
I_{stb}	standby current	standby	–	3	50	μ A
Amplifier outputs OUT+ and OUT–						
V_O	output voltage	on and mute	–	6.5	–	V
$ V_{OO} $	output offset voltage	on and mute	–	–	100	mV
$ \Delta V_{OO} $	delta output offset voltage	on \leftrightarrow mute	–	–	30	mV
Mode select input MODE						
V_I	input voltage		0	–	V_P	V
I_I	input current	$V_{MODE} = 14.4$ V	–	15	20	μ A
V_{th1+}	threshold voltage 1+	standby \rightarrow mute	1	–	2.2	V
V_{th1-}	threshold voltage 1–	mute \rightarrow standby	0.9	–	2	V
V_{msH1}	hysteresis $ (V_{th1+} - V_{th1-}) $		–	200	–	mV
V_{th2+}	threshold voltage 2+	mute \rightarrow on	3.3	–	4.2	V
V_{th2-}	threshold voltage 2–	on \rightarrow mute	3.3	–	4	V
V_{msH2}	hysteresis $ (V_{th2+} - V_{th2-}) $		–	200	–	mV
Status I/O STAT						
PIN STAT AS INPUT						
V_{st}	input voltage		0	–	V_P	V
$I_{st(H)}$	HIGH-level input current	$V_{STAT} = 14.4$ V	–	3.5	4.5	mA
$I_{st(L)}$	LOW-level input current	$V_{STAT} = 0$ V	–	–350	–400	μ A
V_{th1+}	threshold voltage 1+	fast mute \rightarrow class-B	–	–	2	V
V_{th1-}	threshold voltage 1–	class-B \rightarrow fast mute	1	–	–	V
V_{stH1}	hysteresis $ (V_{th1+} - V_{th1-}) $		–	200	–	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{th2+}	threshold voltage 2+	class-B → class-H	–	–	4.2	V
V_{th2-}	threshold voltage 2–	class-H → class-B	3.3	–	–	V
V_{stH2}	hysteresis $ (V_{th2+} - V_{th1-}) $		–	200	–	mV
PIN STAT AS OUTPUT						
$I_{st(mute)}$	mute acknowledge sink current		2.2	–	–	mA
$V_{st(mute)}$	mute acknowledge output voltage	$I_{st} = 2.2 \text{ mA}$	–	–	0.5	V
$I_{st(clB)}$	class-B operation output current		15	–	–	μA
$V_{st(clB)}$	class-B operation output voltage	$I_{st} = 15 \mu\text{A}$	2.0	–	3.0	V
$I_{st(clH)}$	class-H operation source current		–140	–	–	μA
$V_{st(clH)}$	class-H operation output voltage	$I_{st} = -140 \mu\text{A}$	$V_P - 2.5$	–	–	V
$T_{c(th)}$	threshold case temperature sensor		–	120	–	$^{\circ}\text{C}$
Diagnostic output DIAG						
V_{DIAG}	output voltage	active LOW	–	–	0.6	V
R_L	load resistance for open load detection		100	–	–	Ω
$T_{j(th)}$	threshold junction temperature sensor		–	145	–	$^{\circ}\text{C}$

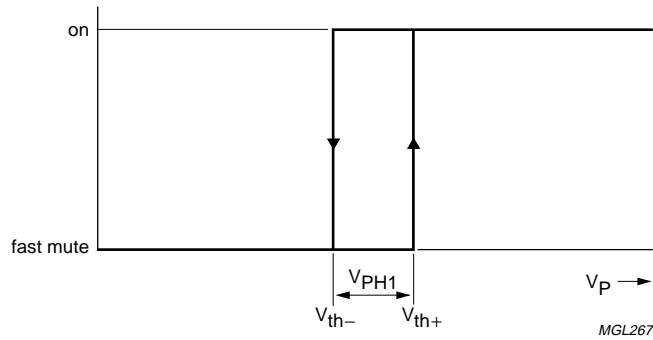
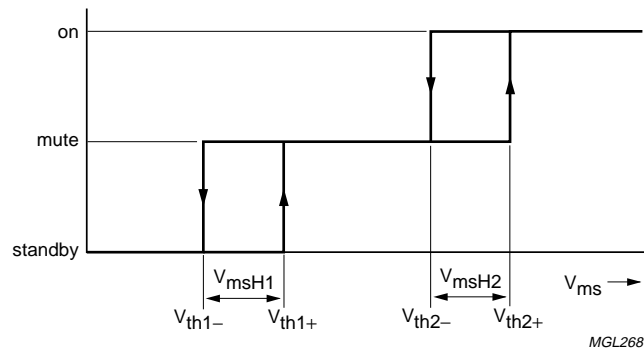


Fig.6 Supply voltage transfer characteristic.

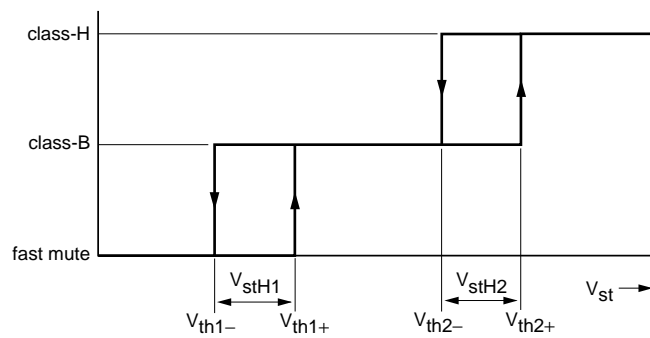
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MGL268

Fig.7 Mode select transfer characteristic.



MGL269

Fig.8 Status I/O transfer characteristic.

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AC CHARACTERISTICS

$V_P = 14.4\text{ V}$; $R_L = 4\ \Omega$; $R_S = 0\ \Omega$; $f = 1\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; measurements in accordance with Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	class-B; THD = 10%	16	19	–	W
		class-H; THD = 10%	60	70	–	W
		class-H; THD = 0.5%	45	55	–	W
$f_{ro(h)(P)}$	high frequency power roll-off	P_o (–1 dB); THD = 0.5%; note 1	–	20	–	kHz
THD	total harmonic distortion	$P_o = 1\text{ W}$	–	0.03	–	%
		$P_o = 20\text{ W}$	–	0.06	–	%
		DDD active	–	2.1	–	%
G_v	voltage gain		25	26	27	dB
$f_{ro(h)(G)}$	high frequency gain roll-off	G_v (–1 dB); note 2	20	–	–	kHz
$ Z_{i(dif)} $	differential input impedance		90	150	210	k Ω
SVRR	supply voltage ripple rejection	on and mute; note 3	55	63	–	dB
		standby; note 3	–	90	–	dB
CMRR	common mode rejection ratio	on; note 4	56	80	–	dB
ISRR	input signal rejection ratio	mute; note 5	80	100	–	dB
$V_{n(o)}$	noise output voltage	on; note 6	–	100	150	μV
		mute; notes 6 and 7	–	60	–	μV

Notes

- The low frequency power roll-off is determined by the value of the electrolytic lift capacitors.
- The low frequency gain roll-off is determined by the value of the input coupling capacitors.
- Supply voltage ripple rejection is measured across R_L ; ripple voltage $V_{ripple(max)} = 2\text{ V}$ (p-p).
- Common mode rejection ratio is measured across R_L ; common mode voltage $V_{cm(max)} = 2\text{ V}$ (p-p).
CMMR (dB) = differential gain (G_v) + common mode attenuation (α_{cm}). Test set-up according to Fig.10; mismatch of input coupling capacitors excluded.
- Input signal rejection ratio is measured across R_L ; input voltage $V_{i(max)} = 2\text{ V}$ (p-p). ISSR (dB) = differential gain (G_v) + mute attenuation (α_m).
- Noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz.
- Noise output voltage is independent of source impedance R_S .

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TEST AND APPLICATION INFORMATION

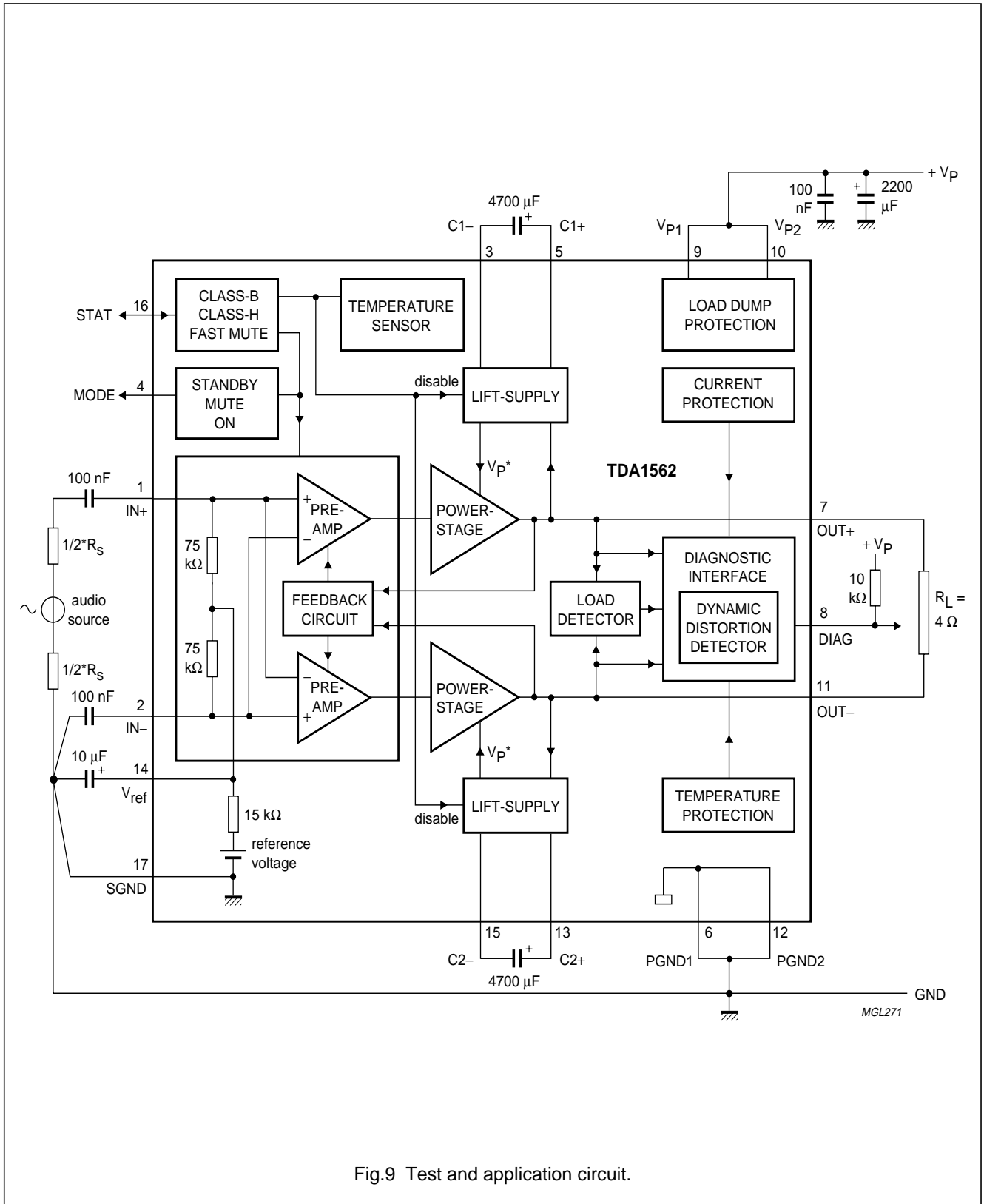


Fig.9 Test and application circuit.

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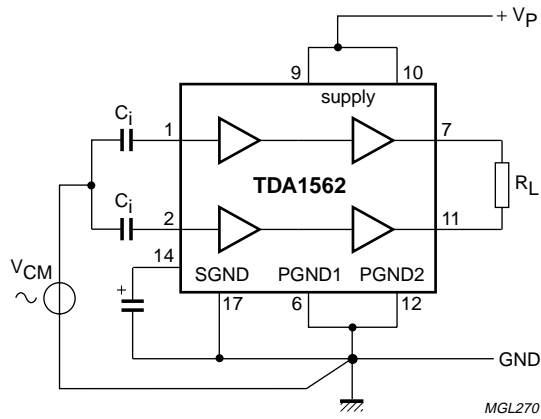


Fig.10 CMRR test set-up.

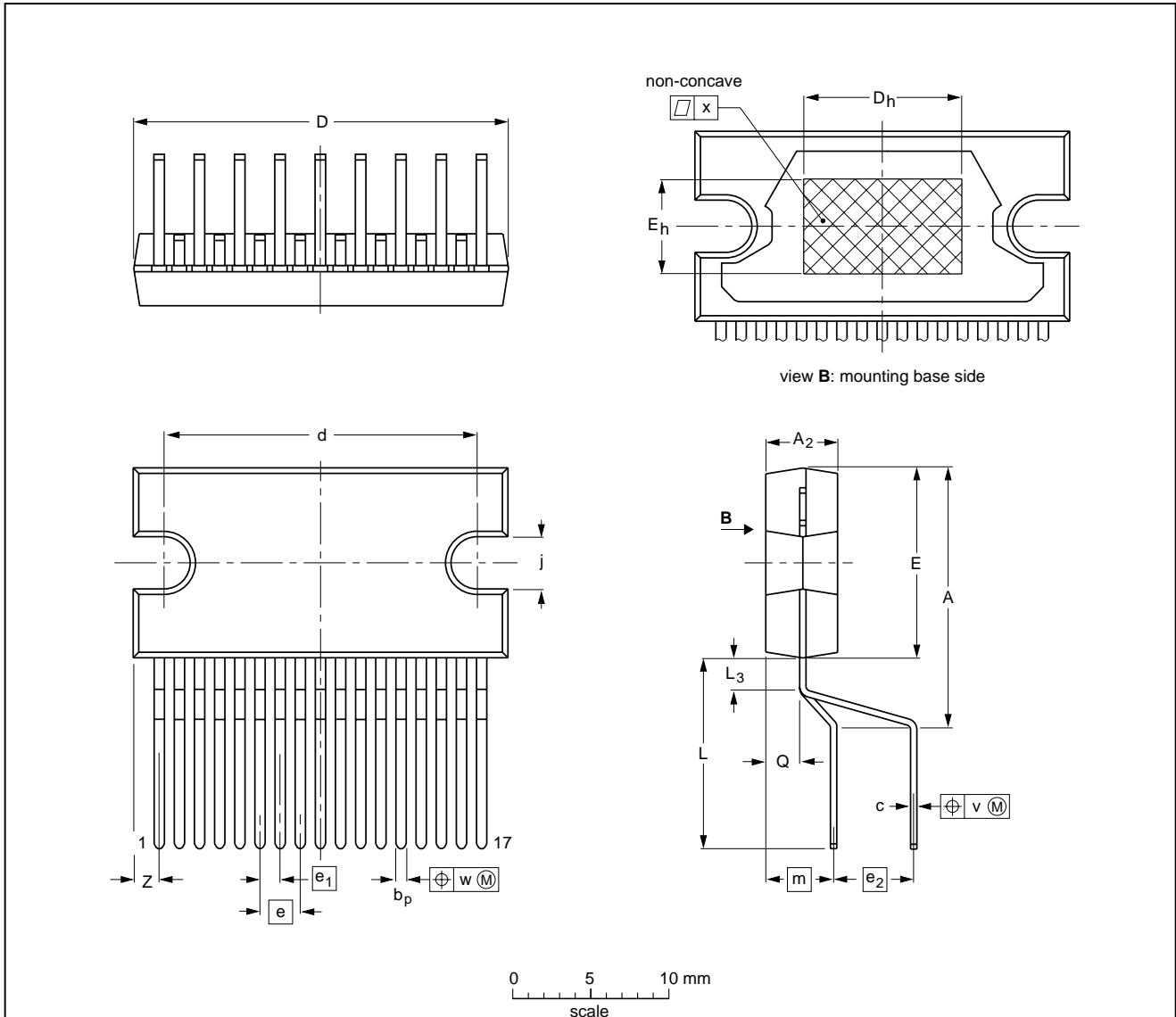
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PACKAGE OUTLINES

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	z ⁽¹⁾
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

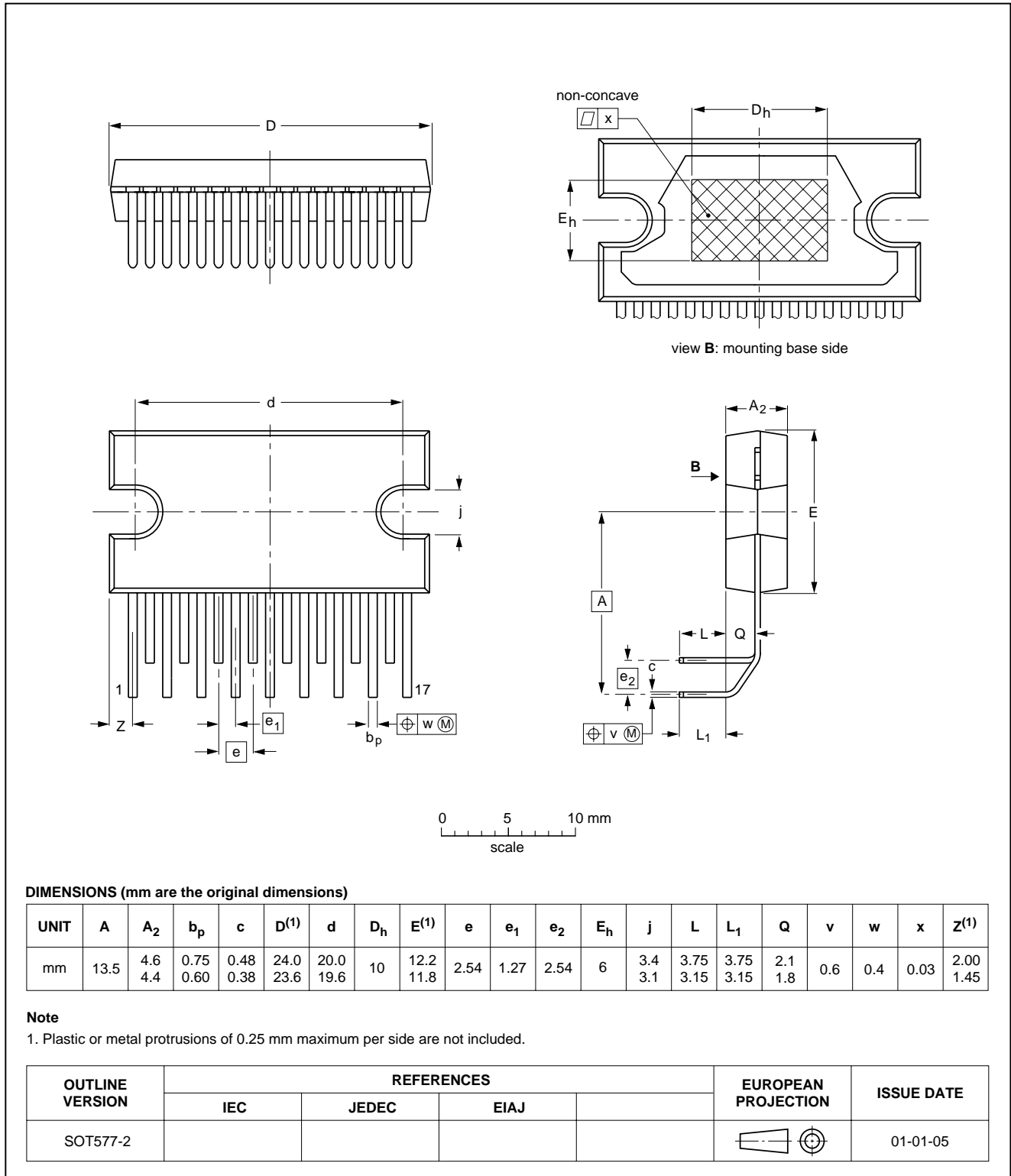
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						97-12-16 99-12-17

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RDBS17P: plastic rectangular-DIL-bent-SIL power package; 17 leads
(row spacing 2.54 mm)

SOT577-2

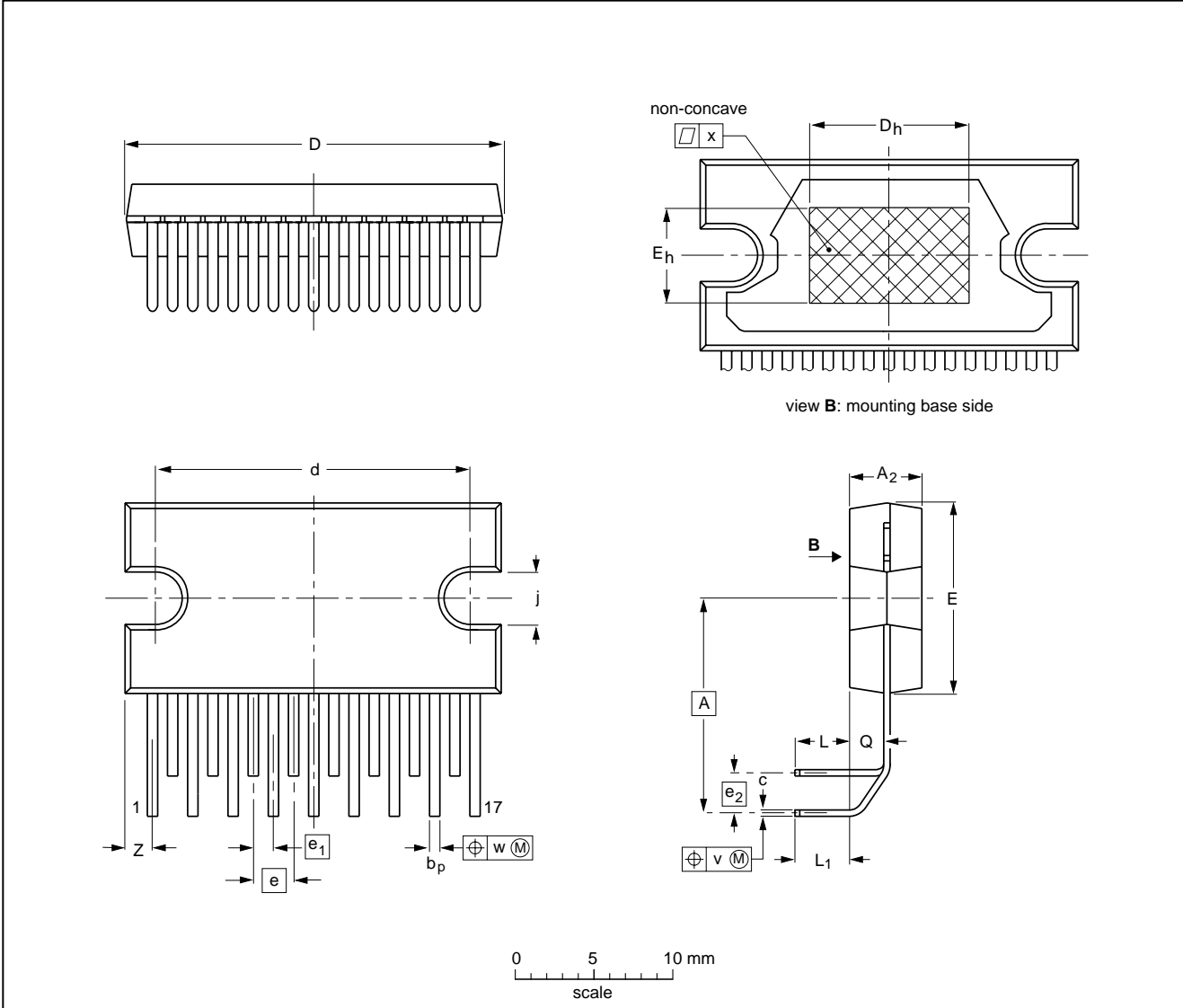


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RDBS17P: plastic rectangular-DIL-bent-SIL power package; 17 leads
(row spacing 2.54 mm)

SOT577-2



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₁	Q	v	w	x	z ⁽¹⁾
mm	13.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	2.54	6	3.4 3.1	3.75 3.15	3.75 3.15	2.1 1.8	0.6	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

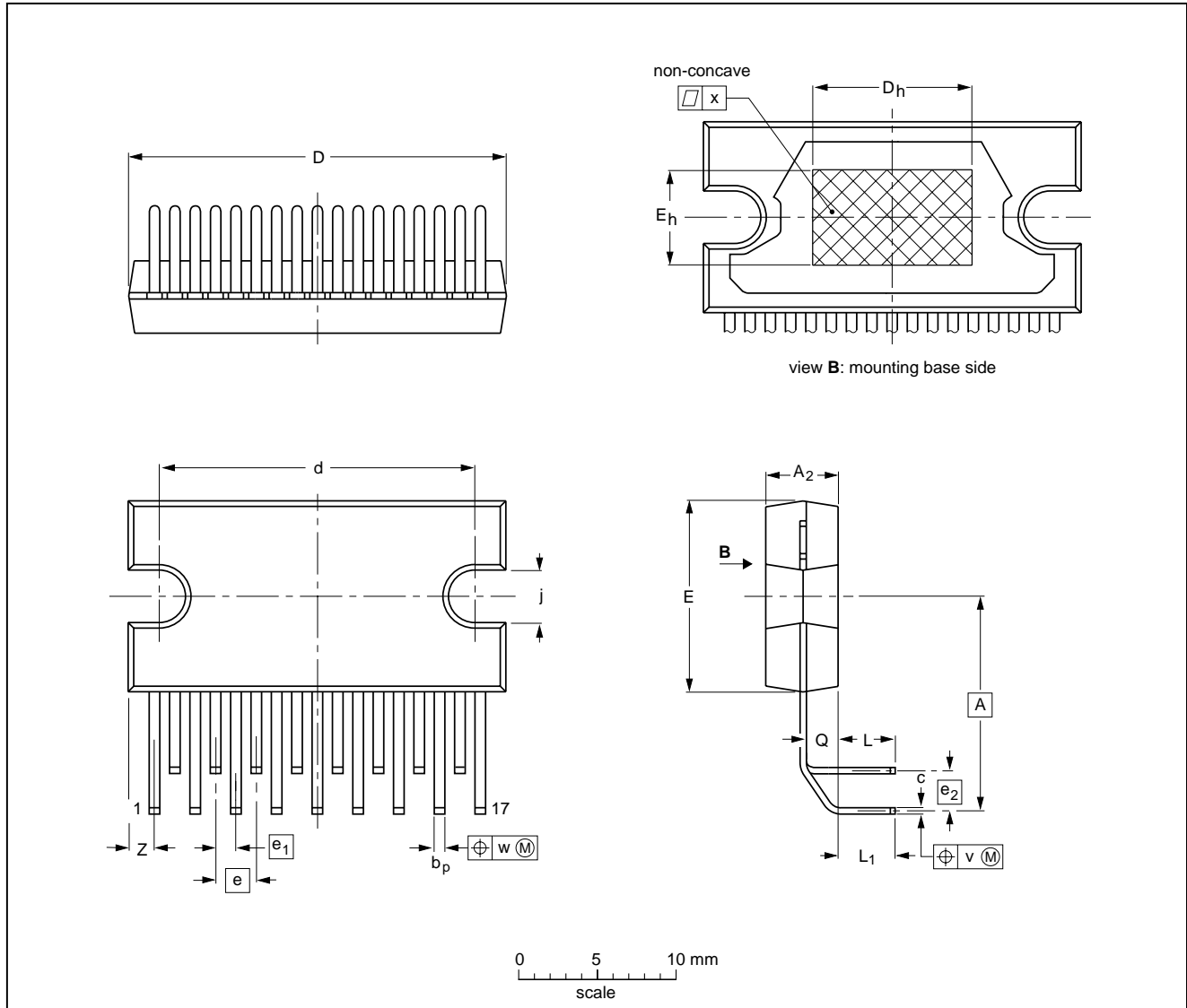
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SOT577-2						01-01-05

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RDBS17P: plastic rectangular-DIL-bent-SIL (reverse bent) power package; 17 leads
(row spacing 2.54 mm)

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DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₁	Q	v	w	x	Z ⁽¹⁾
mm	13.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	2.54	6	3.4 3.1	3.75 3.15	3.75 3.15	2.1 1.9	0.6	0.4	0.03	2.00 1.45

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT668-2						01-01-05

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SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable ⁽¹⁾

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

70 W high efficiency power amplifier with diagnostic facility

TDA1562Q; TDA1562ST;
TDA1562SD

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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NOTES

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