ISL6566EVAL1: Voltage Regulator Down Solutions for Intel and AMD Designs

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Introduction

The Intel and AMD families of microprocessors continue to increase in size with the addition of their next generation microprocessors. These new processors are the most advanced Intel and AMD have developed, requiring advanced power management solutions that have strict requirements for core voltage, transient response, and peak current demands. Responding to the increasing needs of these new processors, Intersil introduces the ISL6566 controller to enable the next generation of power management solutions.

Intersil ISL6566

With the integration of a controller and drivers into one IC, the ISL6566 controller is an all-in-one multi-phase power management solution. This single IC is tailored to accommodate both Intel and AMD's next generation microprocessor specifications with integrated high efficient single-phase drivers capable of handling the stresses of high current loads. The ISL6566EVAL1 uses this IC to form a highly integrated solution for Intel and AMD's high current, high slew-rate applications.

The ISL6566 regulates core voltage, balances channel currents, and provides protective features for one to three synchronous buck converter channels. The controller uses a 6-bit DAC giving the user a digital interface to select the output voltage, which is precisely regulated to ±0.5% accuracy using differential remote voltage sensing. The DAC can be setup to read VRM9, VRM10, or AMD Hammer VID codes, allowing the controller to regulate power of any of the three families of microprocessors. The ISL6566 also has MOSFET Rds(on) current sensing to balance the channel currents and Inductor DCR current sensing to give the user control of the output voltage over load current. Other features of the controller include overcurrent, overvoltage, and undervoltage protection, internal overtemperature protection, programmable output voltage offset, and dynamic VID circuitry.

Integrated into the ISL6566 are three high efficient MOSFET drivers, each capable of driving multiple N-channel power MOSFETs. With a 3A sink current capability, fast rise and fall times, and short dead times, these integrated drivers can drive up to three upper and three lower MOSFETs efficiently, pushing load currents as high as 40A per phase. With the addition of adaptive shoot through technology, the integrated drivers allow the ISL6566 controller to create a full power management solution. For further details on the ISL6566, consult the data sheet [1].

The Intersil multi-phase family controller and driver portfolio continues to expand with new selections to better fit our customers' needs. Refer to our web site for updated information: **www.intersil.com**.

ISL6566 VRD Reference Design

The evaluation kit consists of the ISL6566EVAL1 evaluation board, the ISL6566 datasheet, and this application note. The evaluation board is designed to meet the output voltage and current specifications shown in Table 1, with the VID DIP switches (U3 or U4) set to 100101 (1.400V).

TABLE 1. ISL6566EVAL1 DESIGN PARAMETERS

PARAMETER	MAX	TYPICAL	MIN
No Load VCORE Regulation	1.400V	1.380V	1.360V
VCORE Tolerance	+20mV		-20mV
Load Line Slope		1.0mΩ	
Continuous Load Current	5A		
Load Current Step	95A		
Load Current Transient	100A/µs		

The evaluation board provides convenient test points, two types of power supply connectors, a dynamic VID test circuit, and an on-board transient load generator to facilitate the evaluation process. An on board LED is present to indicate the status of the PGOOD signal. The board is configured for down conversion from 12V to the DAC setting.

The printed circuit board is implemented in 4-layer, 1-ounce copper. Layout plots and part lists are provided at the end of the application note for this design.

Quick Start Evaluation

The ISL6566EVAL1 is designed for quick evaluation after following only a few simple steps. All that is required is a single ATX power supply. To begin evaluating the ISL6566EVAL1 follow the steps below.

1. Before doing anything to the evaluation board, make sure the "Enable" switch (S1) and the "Transient Load Generator" switch (S2) are both in the OFF position.
2. Using an ATX power supply, connect the 20-pin main power supply header to the "ATX POWER" connector (J11) on the board. Next connect the 4-pin 12V header to the "ATX12V" connector (J9) on the board.
3. Set the "Static VID" DIP switch (U3) and the "Dynamic VID" DIP switch (U4) to 100101 (VID4 to VID12.5 respectively). Move the "VID Select" switch (S6) to the STATIC position.
4. Move the "Enable" switch (S1) to the ON position to begin regulation.

After step 4, the ISL6566EVAL1 should be regulating the output voltage, at the “VCORE+” and “GND” test points (J5), within the “No Load VCORE Regulation” parameters in Table 1. The “PGOOD Indicator” LED (D1) should be green to indicate the regulator is operating correctly.

ISL6566EVAL1 Board Features

Input Power Connections

The ISL6566EVAL1 includes two different methods for powering up the board. The first method allows for the use of an ATX power supply. The 20-pin header, J11, allows for the connection of the main ATX power connector, while the 4-pin header, J9, connects the 12V AUX power. It is very important that both connections are secure and the S1 and S2 switches are in the OFF position before switching on the ATX supply.

The second method of powering the ISL6566EVAL1 board is with bench-top power supplies. Three female-banana jacks are provided for connection of bench-top supplies. Connect the +5V terminal to J6, +12V terminal to J7, and the common ground to terminal J8. Voltage sequencing is not required when powering the evaluation board.

Once power is applied to the board, the PGOOD LED indicator will begin to illuminate red. With S1 in the OFF position, the ENABLE input of the ISL6566 is held low and the startup sequence is inhibited.

Output Power Connections

The ISL6566EVAL1 output can be exercised using either resistive or electronic loads. Copper alloy terminal lugs provide connection points for loading. Tie the positive load connection to VCORE, terminals J1 and J2, and the negative to ground, terminals J3 and J4. A shielded scope probe test point, J5, allows for inspection of the output voltage, VCORE.

VID Setup

The Static and Dynamic VID DIP switches would be preset to 100101 (1.400V). If another output voltage level is desired, refer to pages 11 to 13 of the ISL6566 data sheet for the complete DAC table and change the VID switches accordingly. **Note that changing the VID states will change the dynamics of the load generator**

The ISL6566EVAL1 board has two options for VID selection, a Static VID mode and a Dynamic VID mode. When in static VID mode, the VID code, set by the “Static VID” DIP switch (U3), will not change during operation. If the dynamic VID mode is chosen, the regulator will start up with the VID code dictated by the “Dynamic VID” DIP switch (U4). This VID code can then be changed during the operation of the regulator to test the dynamic VID circuitry of the ISL6566. Toggling the “VID Select” switch (S6) will change between the two modes (static and dynamic) of operation.

No matter what VID mode is being used (static or dynamic), all three different DAC tables of the ISL6566 can be accessed using the ISL6566EVAL1. The resistor R2 sets the condition of the VRM10 pin. If this resistor is left open (default), then the VRM10 pin is open and VRM10 DAC codes can be used. If a 0Ω resistor is used for R2, the VRM10 pin is grounded and VRM9 and AMD Hammer DAC codes can be accessed. To use VRM9 codes, set VID12.5 on the “Dynamic VID” and “Static VID” DIP switches to the “1” position. To use AMD Hammer DAC codes, set VID12.5 to the “0” position. In VRM9 and AMD Hammer DAC modes, use only VID4 to VID0 on the DIP switches to select the preferred DAC code.

PVCC Power Options

One unique feature of the ISL6566 is the variable gate drive bias for the integrated drivers. The gate drive voltage for the internal drivers can be any voltage from +5V to +12V by simply connecting the desired voltage to the PVCC1, 2 and 3 pins of the controller. To accommodate the flexibility of the drivers, the ISL6566EVAL1 has been designed to support a multitude of options for the PVCC voltage.

Switching between the different PVCC voltages available on the evaluation board is as simple as populating and depopulating certain resistors. The eval board has three on board voltages available: +5V, +12V, and +8V (from an onboard linear regulator). Refer to Table 2 for what resistors to populate for each voltage option.

TABLE 2. GATE DRIVE VOLTAGE OPTIONS AND RESISTOR SETTINGS

UGATE VOLTAGE	LGATE VOLTAGE	R48	R68	R71	R72
12.0V	12.0V	OPEN	OPEN	OPEN	0Ω
8.0V	8.0V	OPEN	OPEN	0Ω	OPEN
5.0V	5.0V	0Ω	OPEN	OPEN	OPEN
12.0V	5.0V	0Ω	0Ω	OPEN	OPEN

Enabling the Controller

In order to enable the controller, the board must be powered, a VID code must be set, and the PVCC voltage must be set. If these steps have been properly followed, the regulator is enabled by toggling the “ENABLE” switch (S1) to the ON position. When S1 is switched, the voltage on the EN pin of the ISL6566 will rise above the ENLL threshold of 0.66V and the controller will begin its digital soft start sequence. The output voltage ramps up to the programmed VID setting, at which time the PGOOD indicator will switch from red to green.

On-Board Load Transient Generator

Most bench-top electronic loads are not capable of producing the current slew rates required to emulate modern microprocessors. For this reason, a discrete transient load generator is provided on the evaluation board, see Figure 1.

The generator produces a load pulse of 225µs in duration with a period of 27ms. The pulse magnitude is approximately 95A with rise and fall slew rates of approximately 100A/µs as configured. The short load current pulse and long duty cycle is required to limit the power dissipation in the load resistors (R38-R42) and MOSFETs (Q20, Q21). To engage the load generator simply place switch S2, in the “ON” position.

If the DAC code is changed from 100101(1.400V), the transient generator dynamics must be adjusted relative to the new output voltage level. Place a scope probe in J10 to measure the voltage across the load resistors and the dV/dt across them as well. Adjust the load resistors, R38-R40, to achieve the correct load current level. Change resistors R34-R37 to increase or decrease the dV/dt as required to match the desired dI/dt profile.

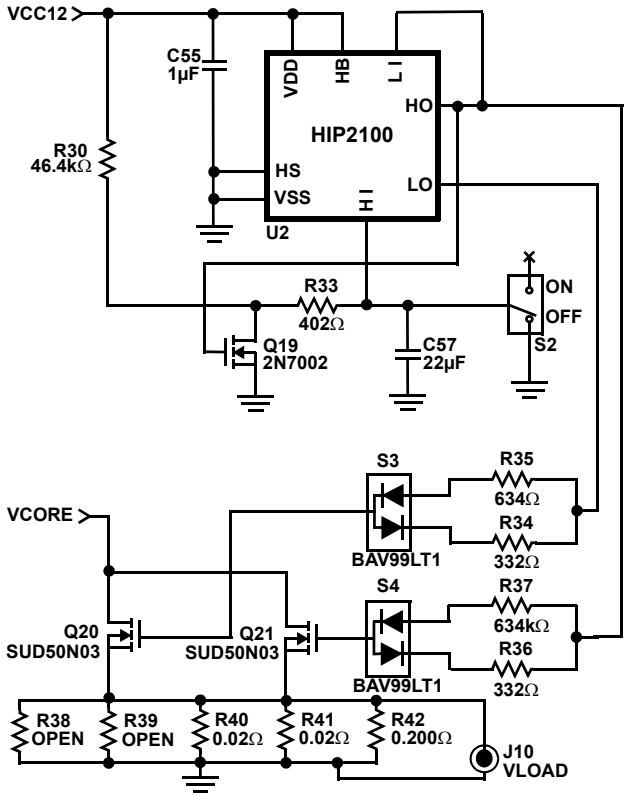


FIGURE 1. LOAD TRANSIENT GENERATOR

Inductor DCR Static Current Sense Points

A unique feature of the ISL6566EVAL1 is the ability to measure the voltage drop across the DCR of each channel’s inductor by multimeter. This is accomplished with the use of a capacitor and resistor series circuit which is placed in parallel across each inductor as illustrated in Figure 2. When current, I_L, flows through the inductor, the voltage crop developed across the DCR will be sensed by the R-C circuit, and an equivalent voltage will be developed across the capacitor C.

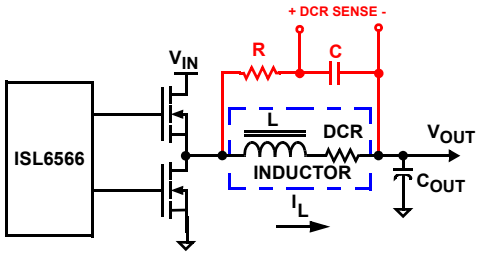


FIGURE 2. DCR STATIC CURRENT SENSE CIRCUIT

In order to not affect the rest of the regulator, the time constant of this R-C circuit is very large, so it can only be used to measure static current, and not transient currents. To calculate the current through each inductor measure the voltage across the “DCR SENSE” points on the ISL6566EVAL1 and then divide that number by the DCR of the inductor. This should give you an accurate reading of the current through each channel during static loads.

Dynamic VID-on-the-Fly Circuitry

Since the ISL6566 supports three different types of DAC encoding (VRM9, VRM10, and AMD Hammer), the ISL6566EVAL1 is able to test the dynamic VID-on-the-Fly circuitry of the IC for each DAC mode of operation. The evaluation board accomplishes this by offering two options for performing the VID-on-the-fly change. Before any VID change is made, the desired starting VID should be set on the “Dynamic VID” DIP switch (U4), and the “VID Select” switch (S6) should be set to the DYNAMIC setting.

The first option available to simulate a dynamic VID-on-the-fly transition should be used if the ISL6566 is operating in VRM10 mode, as described in *VID Setup*. During normal operation, pressing the DYNAMIC SWITCH (S5) button begins the VID transition. An on-board circuit is designed to transition the VID code 450mV below the “Dynamic VID” DIP switch code in 12.5mV steps that occur every 5µs. This simulates the method an Intel VRM10 processor would use to change the VID, allowing the processor to control the VID change.

The second option available to simulate a dynamic VID-on-the-fly transition should be used if the ISL6566 is operating in VRM9 or AMD Hammer mode. The starting VID code should already be set on the “Dynamic VID” DIP switch. Set the ending VID code on the “Static VID” DIP switch. To transition between the two VID codes simply toggle the “VID Select” switch from the DYNAMIC position to the STATIC position. Doing so will immediately change the VID code that is read to the ISL6566, and the IC will be begin slewing the DAC 12.5mV every phase cycle. To switch back to the beginning VID code, simply toggle the “VID Select” switch back to the DYNAMIC position.

Modifying the ISL6566EVAL1 Design

Current Balance Resistors

The ISL6566 uses lower MOSFET Rds(on) current sensing to measure the current through each channel and balance them accordingly. If the lower MOSFETs on the ISL6566EVAL1 are changed, the current balance resistors, R18-R20, should also be changed to adjust for the change in Rds(on). Refer to page 21 in the ISL6566 datasheet to choose new current sense resistors. R18 adjusts the current in channel 1, R20 adjusts the currents in channel 2, and R19 adjusts the current in channel 3. These resistors can also be changed to adjust for any current imbalance due to layout, which is also explained on page 21 of the ISL6566 datasheet.

Load Line (Droop) Regulation

To create an output voltage change proportional to the total current in all the active channels (droop), the ISL6566 uses an inductor DCR sensing R-C network. This network, shown in Figure 3, is designed not only to precisely control the load line of the regulator, but also to thermally compensate for any changes in DCR that may scew the loan line as a result of increases in temperature.

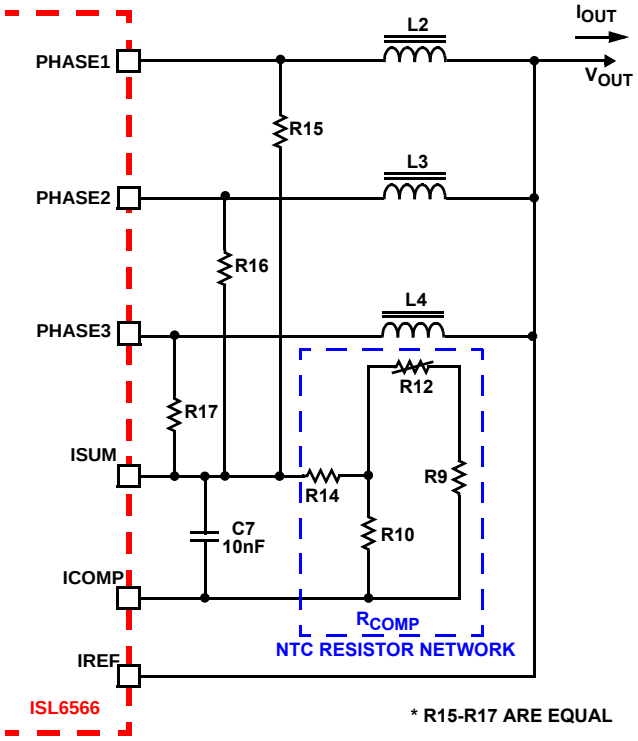


FIGURE 3. DCR SENSING CONFIGURATION

This sensing technique works off the principle that if the R-C time constant of C7 * Rcomp (the NTC resistor network) is equal to the L/DCR time constant of the inductor, the load line impedance will be equal to Rcomp*DCR/R15 (R15-R17 are equal).

If the load line impedance needs to be changed, all that is required is adjusting the values of R15-R17 as explained on page 22 of the ISL6566 datasheet. If the Inductor is changed though, the resistance of the NTC resistor network must first be adjusted so that the new L/DCR time constant is precisely matched.

The NTC resistor network consists of 3 resistors (R9, R10, and R14) and a single NTC thermistor (R12), which is placed close the output inductors. This network is designed to compensate for any change in DCR that occurs due to temperature, and keep the time constant of the R-C network equal to that of the inductor L/DCR time constant. To design this network properly, a design spreadsheet can be obtained from Intersil entitled “NTC Design Spreadsheet for ISL6566.xls”. If a NTC resistor network is not desired, refer to page 21 and 22 of the ISL6566 datasheet to design the entire R-C sense network.

Overcurrent Protection Level

The ISL6566 utilizes a single resistor to set the maximum current level for the IC’s overcurrent protection circuitry. Please refer to page 19 of the ISL6566 datasheet, and adjust resistor R11 accordingly to set the desired overcurrent trip level.

Output Voltage Offset

The ISL6566 allows a designer to accurately offset the output voltage both negatively and positively. All that is required is a single resistor between the OFS and VCC pins, or the OFS pin and GND. The ISL6566EVAL1 has both of these resistor options available on the board. To positively offset the output voltage populate resistor R5. To negatively offset the output voltage populate resistor R7. Please refer to pages 12 and 13 of the ISL6566 datasheet to accurately calculate these resistor values.

Switching Frequency

The switching frequency of the ISL6566 can be adjusted anywhere from 80kHz to 1.5MHz per phase. To change the switching frequency refer to page 24 of the ISL6566 datasheet and adjust the value of frequency set resistor, R13, accordingly.

MOSFET Gate Drive Voltage (PVCC)

The gate drive bias voltage of the integrated drivers in the ISL6566 can be any voltage between +5V and +12V. This bias voltage is set by connecting the desired voltage to the PVCC pins of the IC. Please refer to the *PVCC Power Options* section to set the desired gate drive voltage.

Number of Active Phases

The ISL6566 has the option of 1, 2, or 3-phase operation. The ISL6566EVAL1 is designed to change the number of active phases by simply populating or depopulating one or

two resistors, R45 and R46. Refer to Table 3 for which resistors to populate for 1,2, or 3-phase operation.

TABLE 3. SETTINGS FOR NUMBER OF ACTIVE PHASES

# OF ACTIVE PHASES	R45	R46
3	0Ω	0Ω
2	0Ω	OPEN
1	OPEN	OPEN

ISL6566 VRD Performance

Soft-Start Interval

The typical start-up waveforms for the ISL6566EVAL1 are shown in Figure 4. The waveforms represented in this image show the soft-start sequence of the regulator starting into a 100A load with the DAC set to 1.40V. Before the soft-start interval begins, VCC and PVCC are above POR and the DAC is set to 100101. With these two conditions met, throwing the ENABLE switch into the ON position causes the voltage on the ENLL pin to rise above the ISL6566's enable threshold, beginning the soft-start sequence. For a fixed time of 1ms, VCORE does not move due to the manner in which soft-start is implemented within the controller. After this delay, VCORE begins to ramp linearly toward the DAC voltage. With the converter running at 250kHz, this ramp takes approximately 6.5ms, during which time the input current, ICC12, also ramps slowly due to the controlled building of the output voltage.

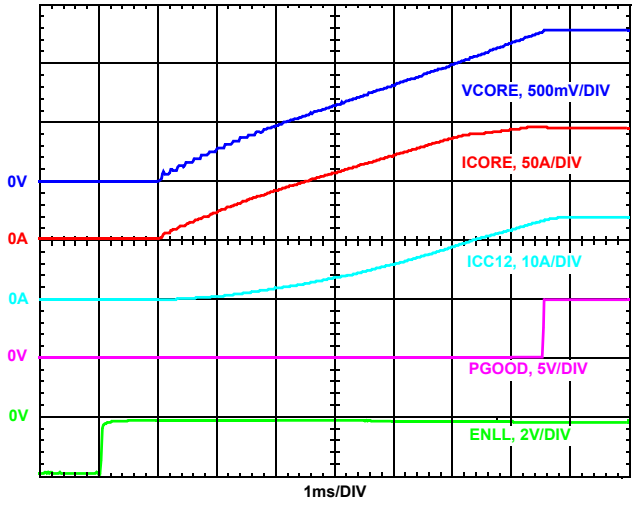


FIGURE 4. SOFT-START INTERVAL WAVEFORMS

Once VCORE reaches the DAC set point, the internal pull-down on the PGOOD pin is released. This allows a resistor from PGOOD to VCC to pull PGOOD high and the PGOOD LED indicator changes from red to green.

Transient Response

The ISL6566EVAL1 design parameters require the regulator to support a 95A maximum load step to a 5A continuous load. This load step will have a maximum slew rate of approximately 100A/µs on both the rising and falling edges. The on-board load transient generator is designed to provide the specified load step, simulating the actual conditions seen at the CPU socket on a motherboard.

During the transient, the core voltage is required to be regulated with a load line of 1mΩ and a tolerance of ±20mV around this load line. In order to meet these design parameters the controller VID is programmed to the maximum no load voltage of 1.400V (100101). An 88.7kΩ resistor (R7) is placed between the OFS and VCC pins create a negative 20mV offset, regulating VCORE to the typical no load voltage of 1.380V specified in Table 1.

The leading edge transient response of the ISL6566EVAL1, which meets the design specifications of Table 1, is shown in Figure 5. In order to obtain the load current waveform shown, a bench-top load is providing a constant 5A, while the on-board transient generator is pulsing a 95A step for 225µs. When the load step occurs, the output capacitors provide the initial output current, causing VCORE to drop suddenly due to the ESR and ESL voltage drops in the capacitors. The controller immediately responds to this drop by increasing the PWM duty cycles to as much as 66%. The duty cycles then decrease to stabilize VCORE and the built in load line regulation holds the output voltage at the programmed level of 1.280V.

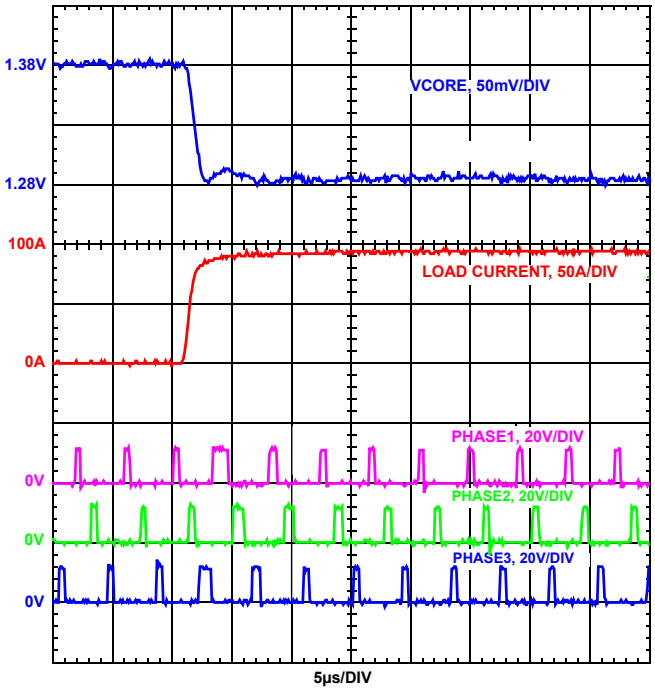


FIGURE 5. RISING EDGE TRANSIENT RESPONSE

At the end of the 225µs load pulse, the load current returns to 5A. The transient response to this falling edge of the load is shown in Figure 4. When the falling load step occurs, the output capacitors must absorb the inductor current which can not fall at the same rate of the load step. This causes VCORE to rise suddenly due to the ESR and ESL voltage

drops in the capacitors. The controller immediately responds to this rise by decreasing the PWM duty cycles to zero, and then increasing them accordingly to regulate VCORE to the programmed 1.375V level.

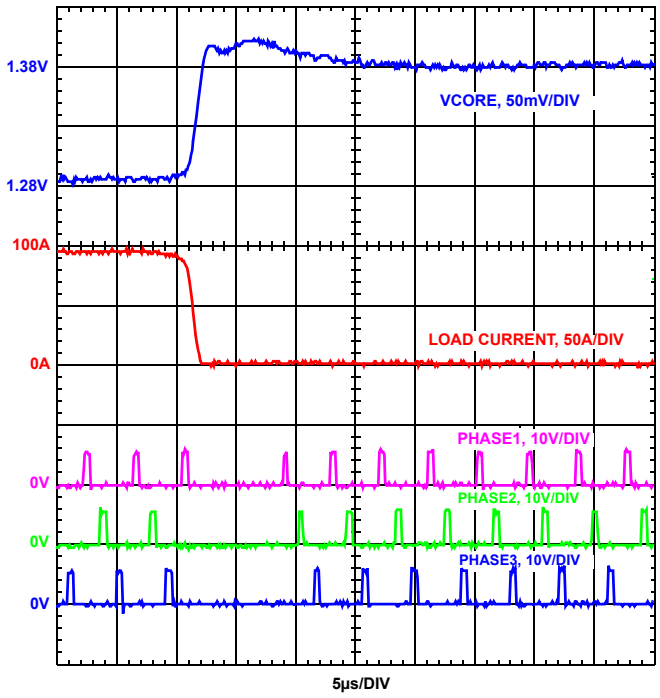


FIGURE 6. FALLING EDGE TRANSIENT RESPONSE

Overcurrent Protection

The ISL6566 is designed to stop all regulation and protect the CPU if an overcurrent event occurs. This is done by continuously monitoring the total output current and comparing it to an overcurrent trip level set by the OCSET resistor, R11. If the output current ever exceeds the trip level, the ISL6566 immediately turns the upper and lower

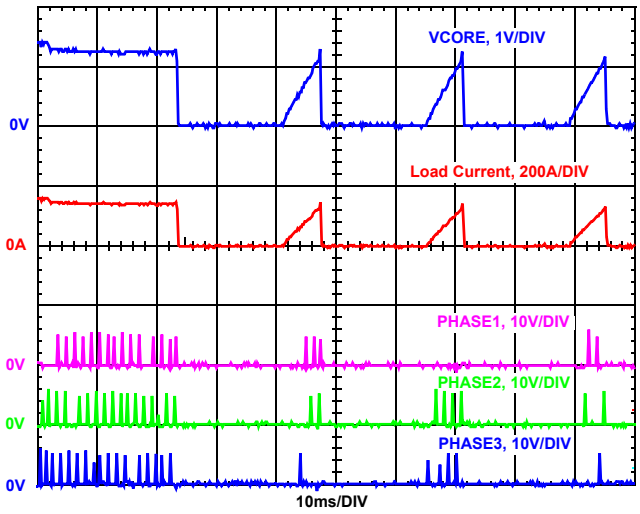


FIGURE 7. OVERCURRENT PROTECTION

MOSFETs off, causing VCORE to fall to 0V. The controller holds the UGATE and LGATE signals in this state for a period of 4096 switching cycles, which at 250kHz is 16.4ms. The controller then re-initializes the soft-start cycle. If the load that caused the overcurrent trip remains, another overcurrent trip will occur before the soft-start cycle completes. The controller will continue to try to cycle soft-start indefinitely until the load current is reduced, or the controller is disabled. This operation is shown in Figure 7.

Pre-POR Overvoltage Protection

Prior to PVCC and VCC exceeding their POR levels, the ISL6566 is designed to protect the load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the input power supply current limits itself and cuts off. In Figure 8, an artificial per-POR overvoltage event has been created by shorting the positive 12V input plane to the PHASE plane. This same 12V input is connected to PVCC pins of the ISL6566. Figure 8 illustrates how the controller protects the load from a high output voltage spike, when the 12V input turns on, by tying LGATE to PHASE.

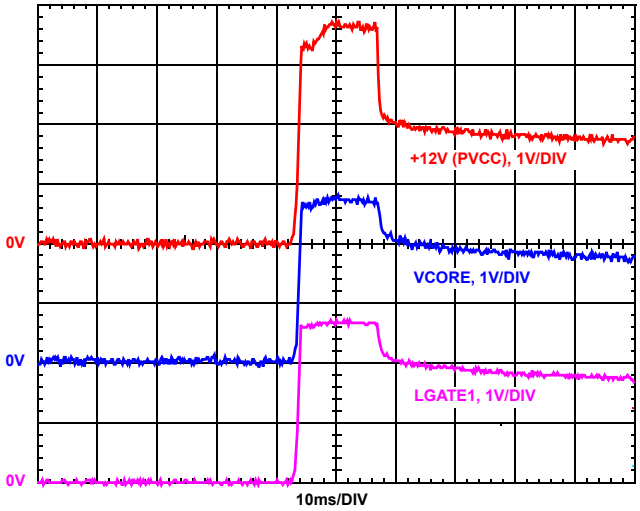


FIGURE 8. PRE-POR OVERVOLTAGE PROTECTION

Overvoltage Protection

To protect from an overvoltage event during normal operation, the ISL6566 continually monitors the output voltage. If the output voltage exceeds a specific limit (set internally), the controller commands the LGATE signals high, turning on the lower MOSFETs to keep the output voltage below a level that might cause damage to the CPU. As shown in the overvoltage event in Figure 9, turning on the lower MOSFETs not only keeps the output voltage from rising, it also sinks a large amount of current, causing the input voltage to the power stage to drop. If this causes the input power supply voltage to fall below the POR level of the ISL6566, as seen at the end of the waveform in Figure 9, the controller responds by using the pre-POR overvoltage protection explained in the previous section. This allows the

ISL6566 always keep the output load safe from high voltage spikes during an entire overvoltage event.

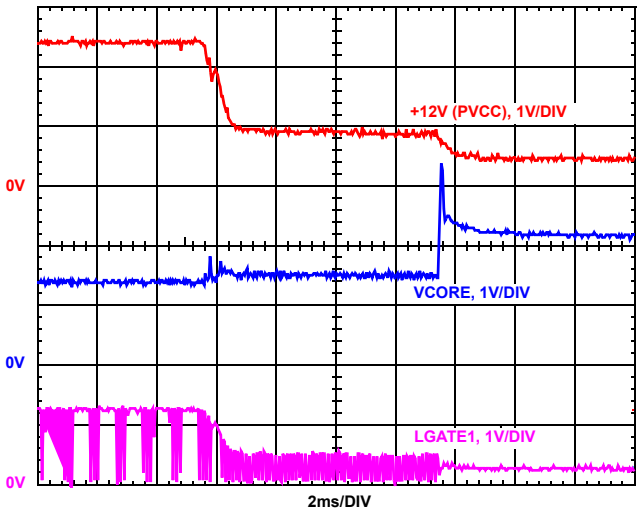


FIGURE 9. PRE-POR OVERVOLTAGE PROTECTION

VID on the Fly

To simulate a VID transition, the ISL6566EVAL1 has on-board dynamic VID circuitry which is described in the *Dynamic VID-on-the-Fly Circuitry* section. Since the ISL6566 handles VID transitions differently, depending on whether the controller is operating in the VRM10, VRM9, or AMD modes of operation, waveforms for each type of transition are illustrated below.

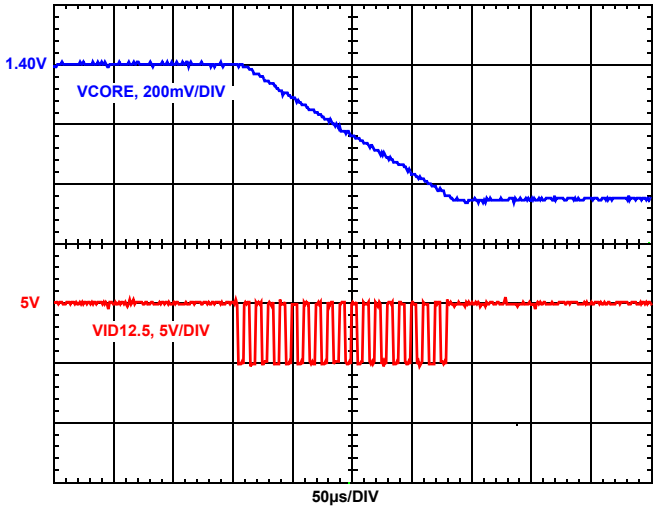


FIGURE 10. VRM10 VID-ON-THE-FLY TRANSITION FROM 1.40V TO 0.950V

Figure 10 shows a VRM10 VID transition from 1.40V (100101) to 0.950V(001011). This transition begins with the DYNAMIC SWITCH signal switching from 5V to 0V, which triggers the on-board circuitry to externally change the VID code once every 5µs. Every time the VID code changes, the VID12.5 signal transitions between 0V and 5V. During the VID transition the controller smoothly moving from one code to the next until the final code of 0.9500V is reached.

Pressing the DYNAMIC SELECT switch again returns the VID code to the original setting of 1.40V, as Figure 11 illustrates. This transition is handled smoothly by the ISL6566 with no overshoot as the final code is reached.

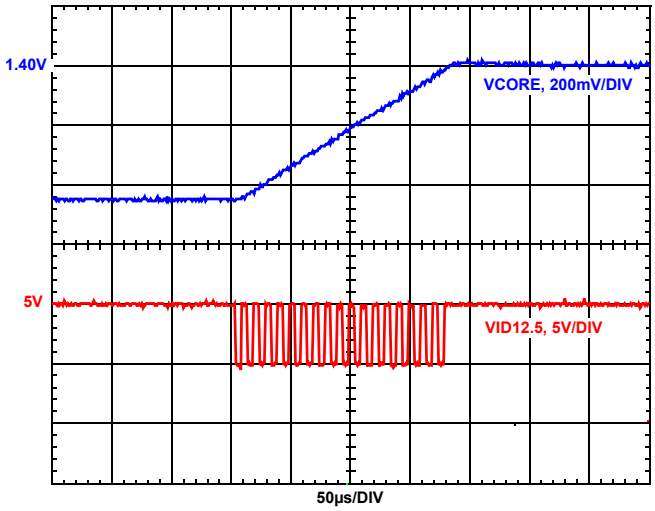


FIGURE 11. VRM10 VID-ON-THE-FLY TRANSITION FROM 0.950V TO 1.40V

Figure 12 and 13 both show dynamic VID transitions when the controller is operating in the VRM9 or AMD Hammer mode. These modes of operation are similar because once the VID code changes, the ISL6566 begins slewing the DAC 12.5mV every phase cycle until the new DAC voltage is reached. Figure 12 illustrates a VID transition from 1.500V(01110) to 1.125V(11101), which begins when the VID0 signal transitions from 0V to 5V. In Figure 13, the VID code returns to 1.500V and the output voltage rises smoothly to this original voltage.

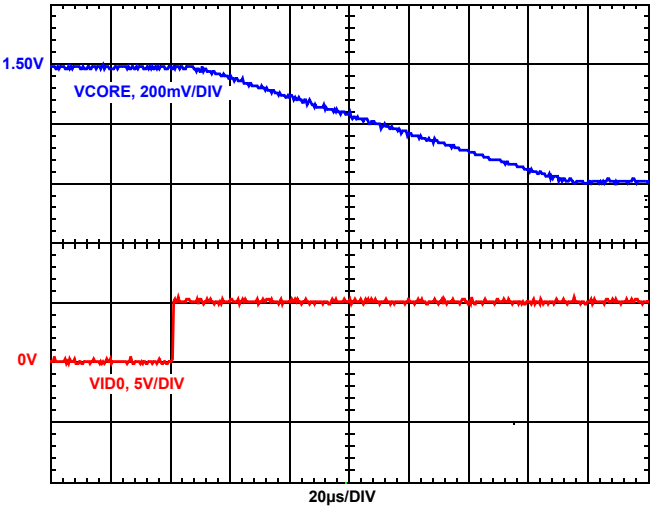


FIGURE 12. VRM9 / AMD HAMMER VID-ON-THE-FLY TRANSITION FROM 1.500V TO 1.125V

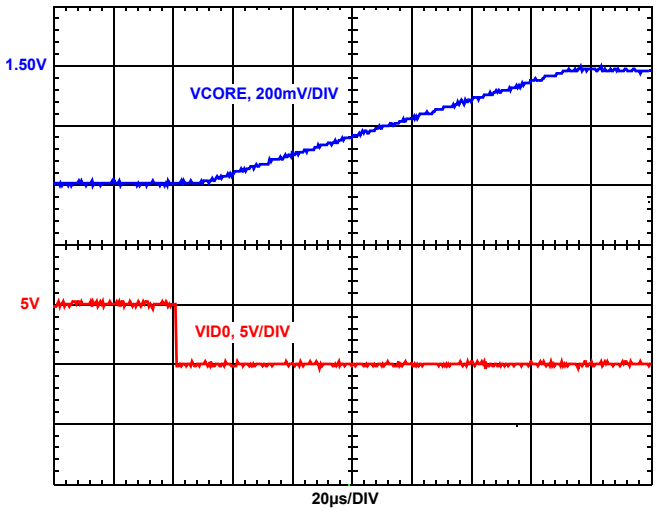


FIGURE 13. VRM9 / AMD HAMMER VID-ON-THE-FLY TRANSITION FROM 1.125V TO 1.500V

Efficiency

The efficiency of the ISL6566EVAL1 board, loaded from 5A to 100A, is plotted in Figure 14. Measurements were performed at room temperature and taken at thermal equilibrium with **300LFM OF AIR FLOW**. The efficiency peaks just below 88% at 40A and then levels off steadily to approximately 81% at 100A. The use of air flow is recommended for high power microprocessor designs, with 300LFM as the mean. The addition of air flow keeps the components cooler and raises the overall efficiency across the load range.

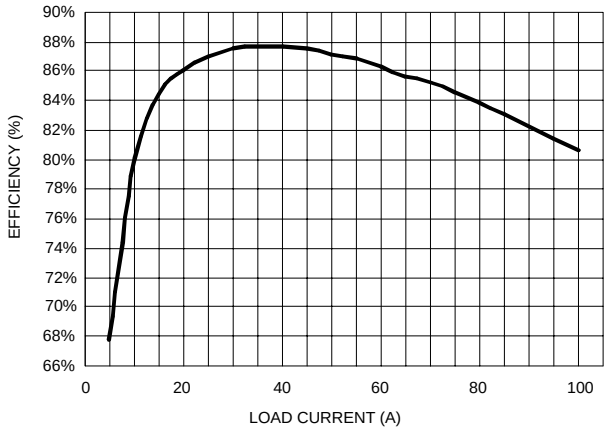


FIGURE 14. EFFICIENCY vs LOAD CURRENT

Thermal Performance

Table 2 shows the laboratory measured upper and lower MOSFET, inductor, and controller temperatures at 100A of load current. The measurements were performed at room temperature (25 °C) and taken at thermal equilibrium with **300LFM OF AIR FLOW**.

TABLE 4. THERMAL DATA AT 100A LOAD

COMPONENT	PHASE 1	PHASE 2	PHASE 3
Upper MOSFETs	78°C	79°C	84°C
Lower MOSFETs	85°C	90°C	94°C
Inductor	57°C	64°C	68°C
ISL6566	83°C	83°C	83°C

Summary

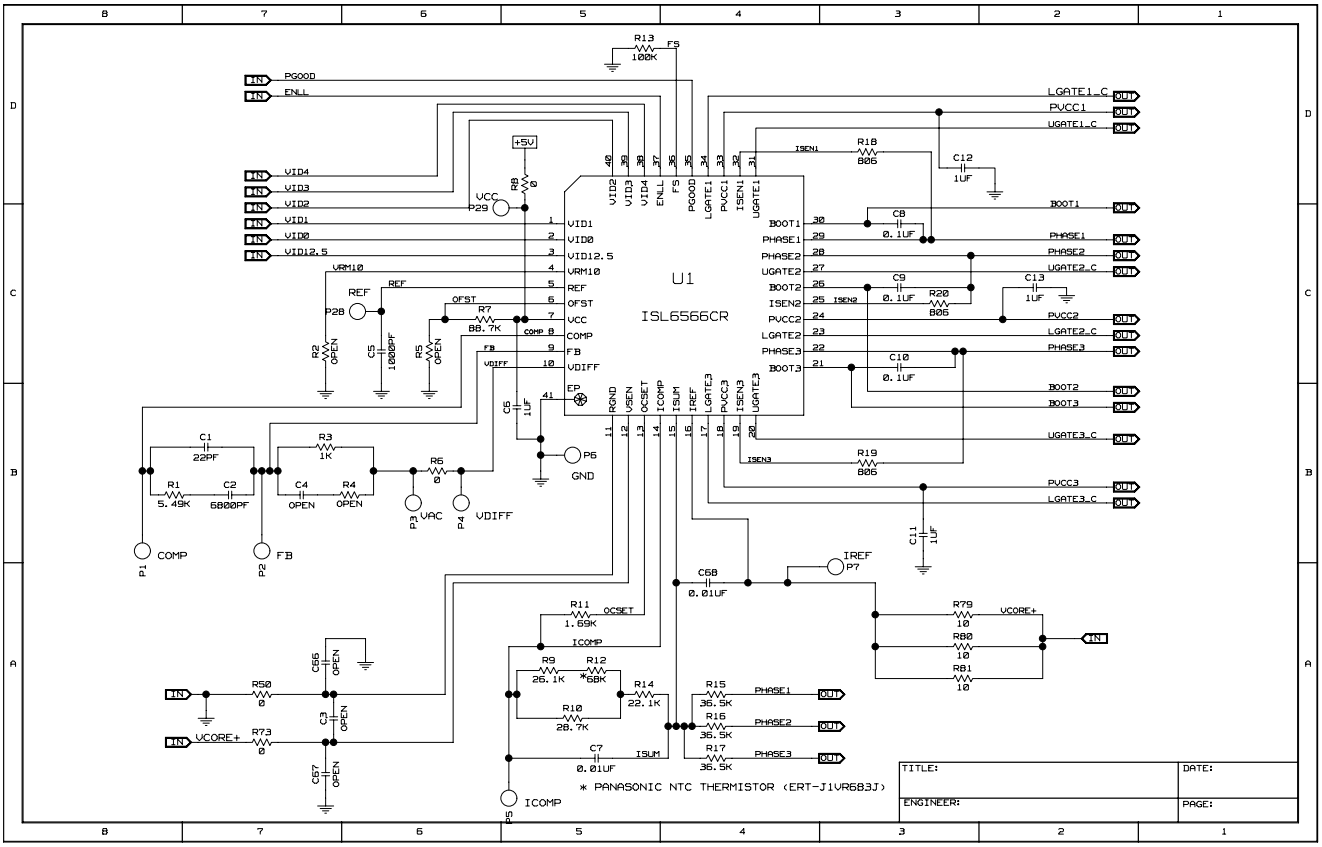
The ISL6566EVAL1 is an adaptable evaluation tool which showcases the performance of the ISL6566 integrated controller. Designed to meet the performance requirements of Intel's and AMD's next generation designs, the board allows the user the flexibility to configure the board for current as well as future microprocessor offerings. The following pages provide a board schematic, bill of materials and layout drawings to support implementation of this solution.

References

Intersil documents are available on the web at www.intersil.com.

[1] ISL6566 Data Sheet, Intersil Corporation, File No. FN9178

Schematic


U1
ISL6566CR
PGOOD
ENLL
VID4
VID3
VID2
VID1
VID0
VID12.5
VRM10
REF
OFST
VCC
COMP
FB
VDIFF
EP
PGND
VSEN
OCSET
ICOMP
ISUM
IREF
LGATE3
PVCC3
ISEN3
UGATE3
LGATE1
PVCC1
ISEN1
UGATE1
BOOT1
PHASE1
PHASE2
UGATE2
BOOT2
ISEN2
PVCC2
LGATE2
PHASE3
BOOT3
+5V
VCC
FS
R13 100K
R8 0
R7 88.7K
R2 OPEN
C5 1000PF
R5 OPEN
C1 22PF
R1 5.49K
C2 6800PF
R3 1K
C4 OPEN
R4 OPEN
R6 0
C6 1UF
C8 0.1UF
C9 0.1UF
C10 0.1UF
C11 1UF
C12 1UF
C13 1UF
R18 806
R20 806
R19 806
C68 0.01UF
R11 1.69K
R9 26.1K
R12 *68K
R14 22.1K
R10 28.7K
C7 0.01UF
R15 36.5K
R16 36.5K
R17 36.5K
R79 10
R80 10
R81 10
VCORE+
R50 0
R73 0
C66 OPEN
C3 OPEN
C67 OPEN
P1 COMP
P2 FB
P3 VAC
P4 VDIFF
P5 ICOMP
P6 GND
P7 IREF
* PANASONIC NTC THERMISTOR (ERT-J1VR683J)
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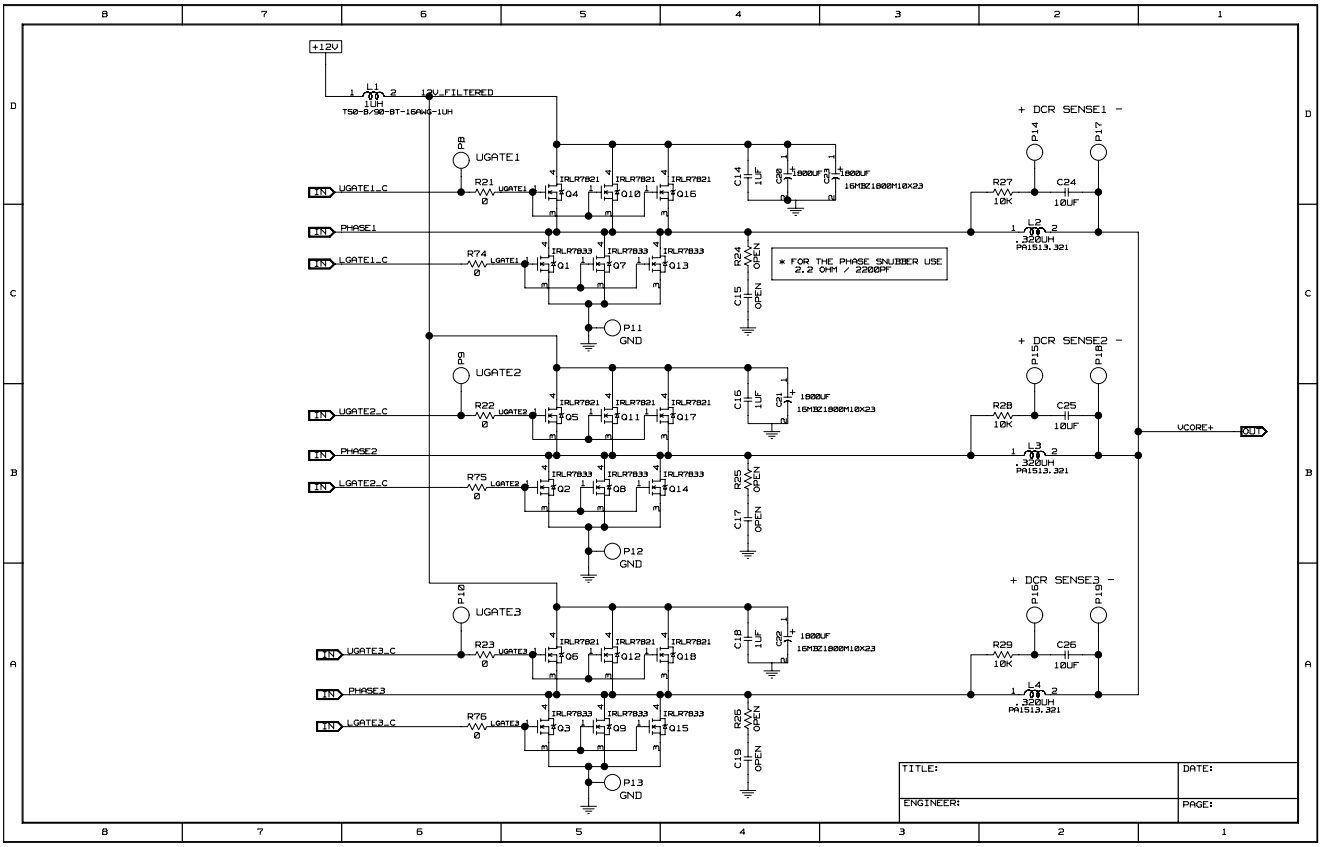
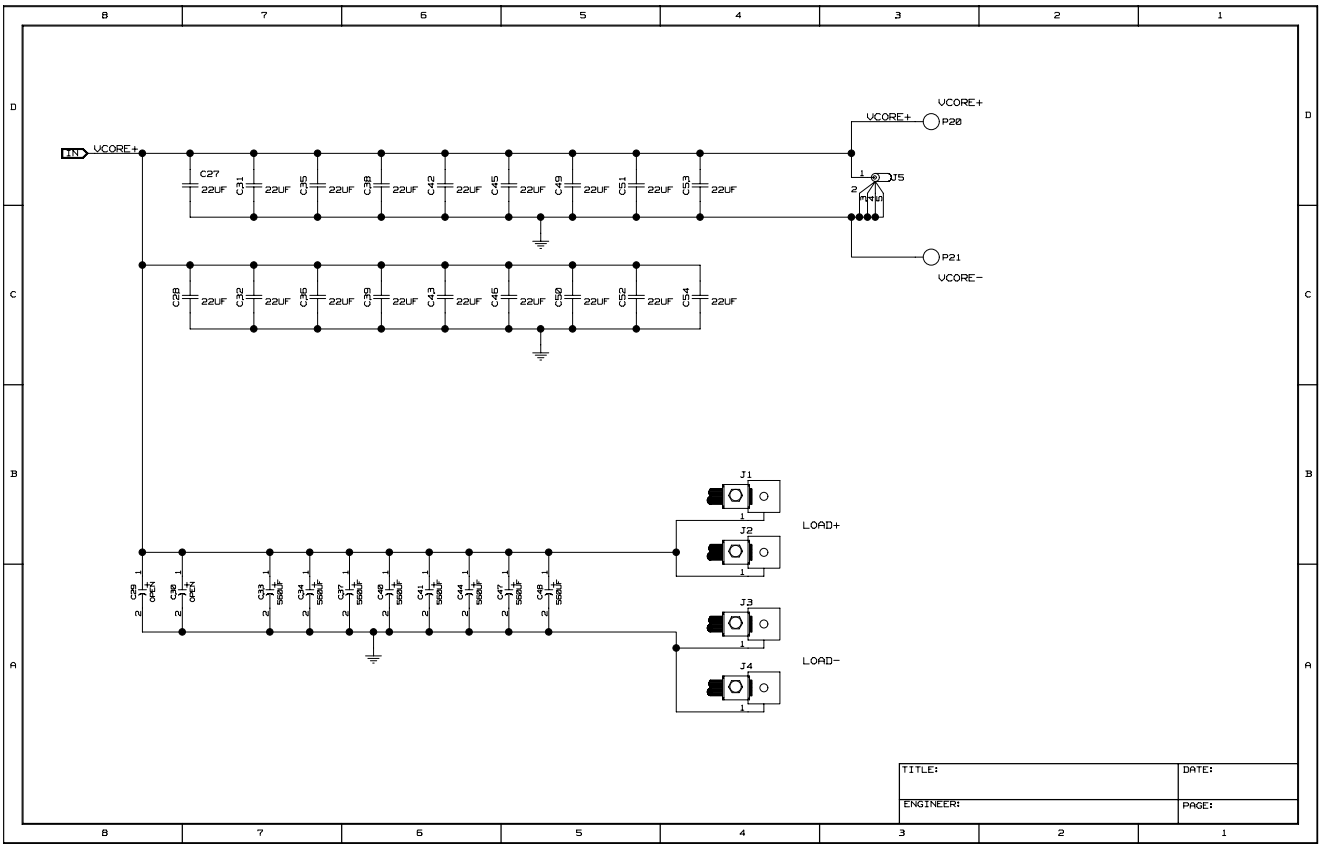
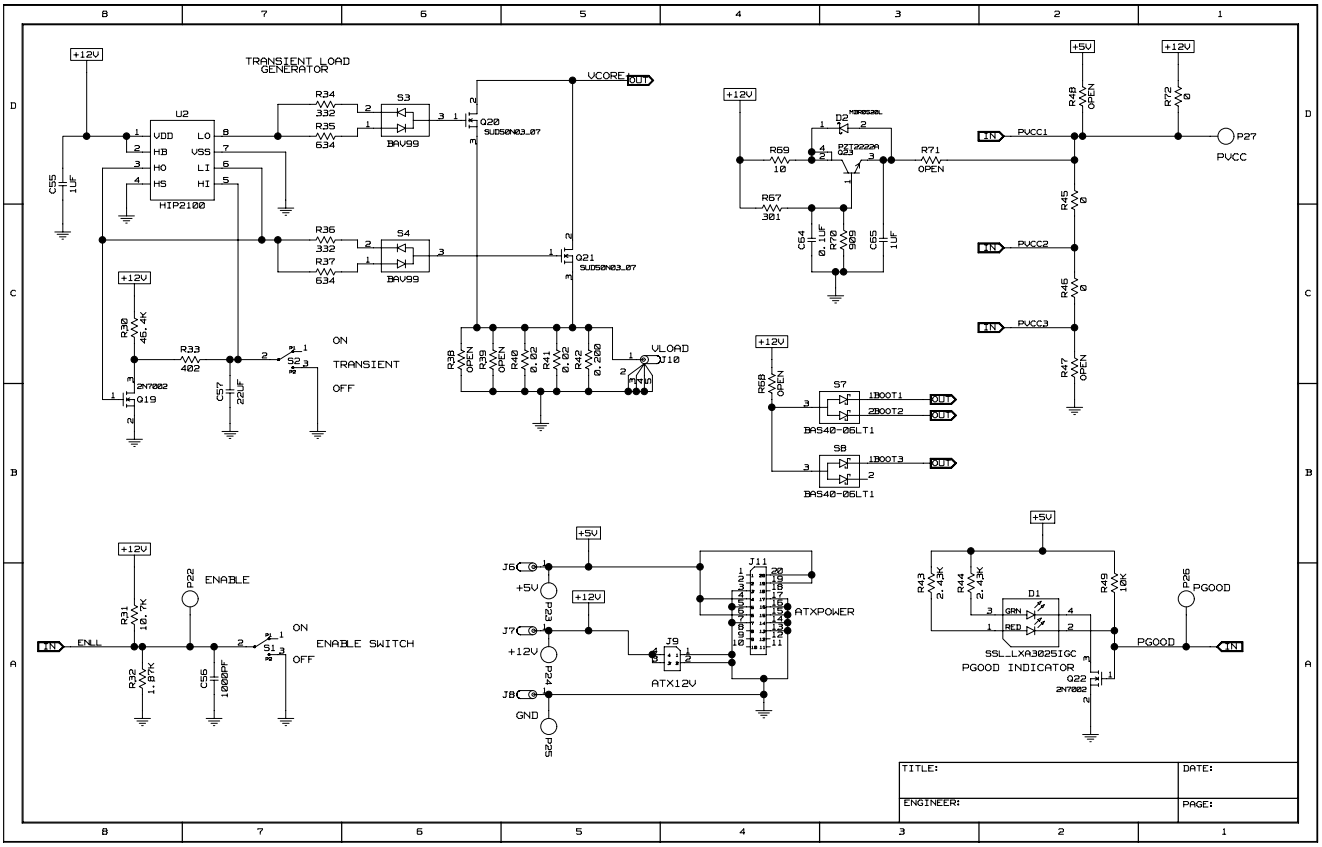
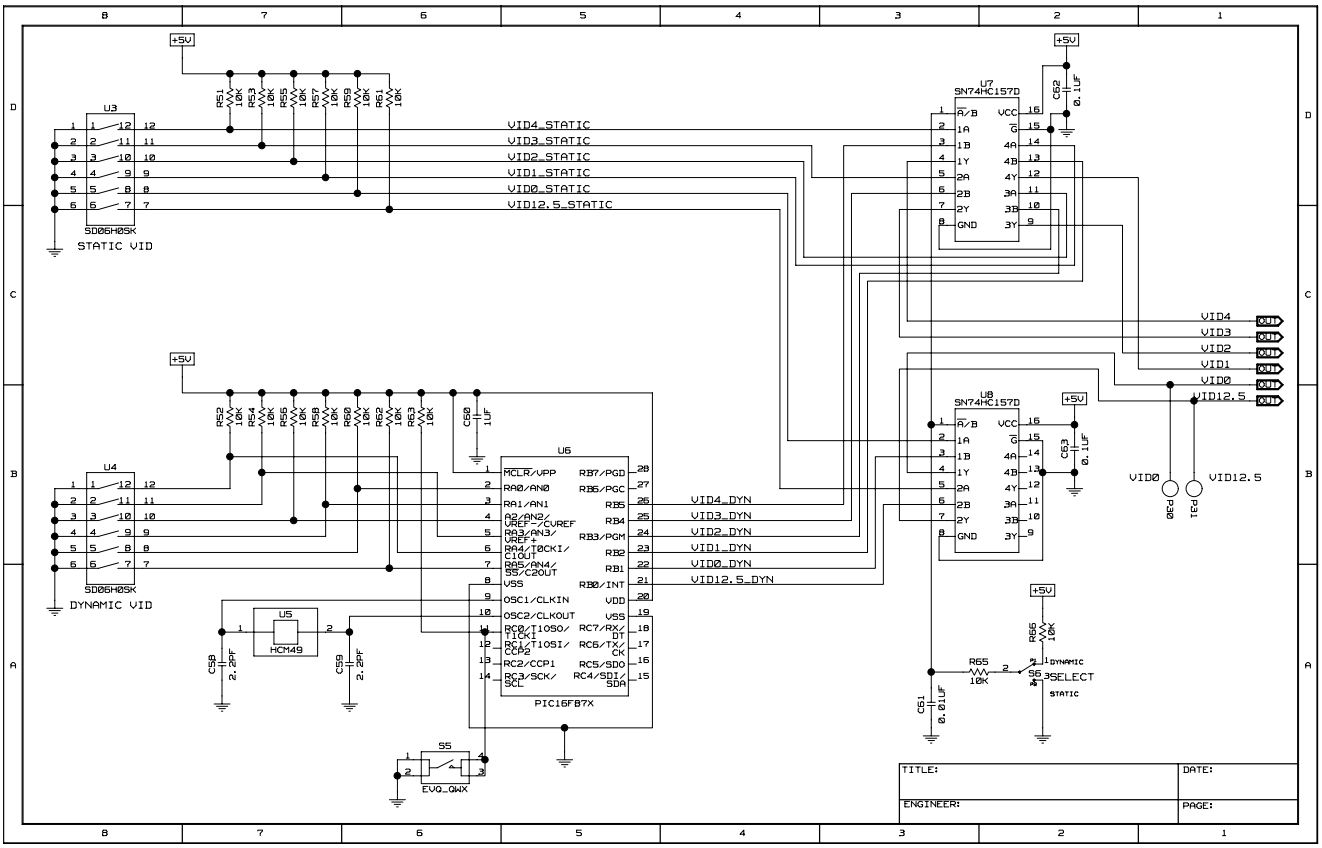

+12V
L1 1UH T50-8/90-BT-16AWG-1UH
12V_FILTERED
UGATE1
UGATE1_C
PHASE1
LGATE1_C
UGATE2
UGATE2_C
PHASE2
LGATE2_C
UGATE3
UGATE3_C
PHASE3
LGATE3_C
IRLR7821
IRLR7833
R21 0
R22 0
R23 0
R74 0
R75 0
R76 0
R24 OPEN
R25 OPEN
R26 OPEN
C14 1UF
C16 1UF
C18 1UF
C15 OPEN
C17 OPEN
C19 OPEN
C20 1800UF
C21 1800UF
C22 1800UF
16MBZ1800M10X23
* FOR THE PHASE SNUBBER USE 2.2 OHM / 2200PF
+ DCR SENSE1 -
+ DCR SENSE2 -
+ DCR SENSE3 -
R27 10K
R28 10K
R29 10K
C24 10UF
C25 10UF
C26 10UF
L2 .320UH PA1513.321
L3 .320UH PA1513.321
L4 .320UH PA1513.321
VCORE+
P8 UGATE1
P9 UGATE2
P10 UGATE3
P11 GND
P12 GND
P13 GND
P14 P15 P16 P17 P18 P19
TITLE:
DATE:
ENGINEER:
PAGE:

Schematic (Continued)





Schematic (Continued)



Bill of Material

Top Layer Components

QTY	REFERENCE	VALUE	DESCRIPTION	VENDOR	PART NO.	PACKAGE
1	C1	22pF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0805
1	C2	6800pF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0805
3	C3, C66, C67	OPEN	Capacitor, Ceramic	Various		0603
1	C4	OPEN	Capacitor, Ceramic	Various		0805
1	C5	1000pF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0805
4	C6, C11-C13	1.0µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0805
1	C7	.01µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0603
4	C8-C10, C64	0.1µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0805
5	C14, C16, C18, C55, C65	1.0µF	Capacitor, Ceramic, 16V, X7R, 10%	Various		1206
3	C15, C17, C19	OPEN	Capacitor, Ceramic	Various		0805
4	C20-C23	1800µF	Capacitor, AL Electrolytic, 16V	Rubycon	16MBZ1800M10X23	Thru Hole
18	C27, C28, C31, C32, C35, C36, C38, C39, C42, C43, C45, C46, C49-C54	22µF	Capacitor, Ceramic, 6.3V, X5R, 20%	Various		1206
2	C29, C30	OPEN	Capacitor			Thru Hole
8	C33, C34, C37, C40, C41, C44, C47, C48	560µF	Capacitor, OS-CON, 4V	Sanyo	4SEPC560MX	Thru Hole

Top Layer Components (Continued)

QTY	REFERENCE	VALUE	DESCRIPTION	VENDOR	PART NO.	PACKAGE
1	C57	22µF	Capacitor, Ceramic, 16V, X5R, 20%	TDK	C3225X5R1C226M	1210
1	C68	.01µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0603
1	C63	0.1µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0603
1	D1		Red/Green LED	Lumex	SLL-LXA3025IGC	SMT
1	D2		Schottky Diode	Fairchild	MBR0520L	SOD-123
4	J1-J4		Terminal Connector	Burndy	KPA8CTP	Solder Mount
2	J5, J10		Probe Socket	Tektronix	1314353-00	Thru Hole
2	J6-J7		Female Banana Connector, Red	Johnson Components	111-0702-001	Screw On
1	J8		Female Banana Connector, Black	Johnson Components	111-0703-001	Screw On
1	J9		2x2 Power HDR 1MTG Hole	Molex	39-29-9042	Thru Hole
1	J11		2x10 Power Conn-1MTG Pin	Molex	39-29-9203	Thru Hole
1	L1	1.0µH	Inductor, T50-8/90 core, 8 turns AWG16	Micrometals	T50-8/90	Thru Hole
3	L2-L4	0.320µH	Inductor, 13x13mm	Pulse	PA1513.321	Surface Mount
22	P1-P5, P7-P10, P14-P20, P22, P26, P28, P29, P30, P31		Small Test Point	Jolo	SPCJ-123-01	Thru Hole
9	P6, P11-P13, P21, P23-P25, P27		Turret Test Point	Keystone	1514-2	Thru Hole
6	Q1, Q2, Q8, Q9, Q13, Q15		Power MOSFET	International Rectifier	IRLR7833	TO-252AA
6	Q3, Q5-Q7, Q14, Q16	OPEN	Power MOSFET			TO-252AA
6	Q4, Q10-Q12, Q17, Q18		Power MOSFET	International Rectifier	IRLR7821	TO-252AA
1	Q19		General Purpose MOSFET	Various	2N7002	SOT-23
2	Q20, Q21		Power MOSFET	Vishay	SUD50N03-07	TO-252AA
1	Q23		General Purpose NPN Transistor	Fairchild	PZT2222A	SOT-223
1	R1	5.49kΩ	Resistor, 1%, 1/16W	Various		0603
1	R2	OPEN	Resistor	Various		0603
1	R3	1.0kΩ	Resistor, 1%, 1/16W	Various		0603
1	R4	OPEN	Resistor	Various		0603
1	R5	OPEN	Resistor	Various		0603
5	R6, R45, R46, R50, R73	0Ω	Resistor, 1%, 1/16W	Various		0603
1	R7	88.7kΩ	Resistor	Various		0603
7	R8, R21-R23, R74-R76	0Ω	Resistor, 1%, 1/10W	Various		0805
1	R9	26.1kΩ	Resistor, 1%, 1/16W	Various		0603
1	R10	28.7kΩ	Resistor, 1%, 1/16W	Various		0603
1	R11	1.69kΩ	Resistor, 1%, 1/16W	Various		0603
1	R12	68kΩ	NTC Thermistor	Panasonic	ERT-J1VR683J	0603
1	R13	100kΩ	Resistor, 1%, 1/16W	Various		0603
1	R14	22.1kΩ	Resistor, 1%, 1/16W	Various		0603

Top Layer Components (Continued)

QTY	REFERENCE	VALUE	DESCRIPTION	VENDOR	PART NO.	PACKAGE
3	R15-R17	36.5kΩ	Resistor, 1%, 1/16W	Various		0603
3	R18-R20	806Ω	Resistor, 1%, 1/16W	Various		0603
3	R24-R26	OPEN	Resistor, 1%, 1/8W	Various		1206
1	R30	46.4kΩ	Resistor, 1%, 1/16W	Various		0603
1	R33	402Ω	Resistor, 1%, 1/16W	Various		0603
2	R34, R36	332Ω	Resistor, 1%, 1/16W	Various		0603
2	R35, R37	634Ω	Resistor, 1%, 1/16W	Various		0603
2	R38, R39	OPEN	Thick Film Chip Resistor	Various		2512
2	R40-R41	.020Ω	Thick Film Chip Resistor, 1%, 1W	Various		2512
1	R42	.200Ω	Thick Film Chip Resistor, 1%, 1W	Various		2512
1	R47	OPEN	Resistor	Various		0603
1	R48	OPEN	Resistor	Various		1206
1	R67	301Ω	Resistor, 1%, 1/10W	Various		0805
1	R68	OPEN	Resistor, 1%, 1/8W	Various		1206
1	R69	10Ω	Resistor, 1%, 1/10W	Various		0805
1	R70	909Ω	Resistor, 1%, 1/10W	Various		0805
1	R71	OPEN	Resistor, 1%, 1/8W	Various		1206
1	R72	0.0Ω	Resistor, 1%, 1/8W	Various		1206/2512
3	R79-R81	10Ω	Resistor, 1%, 1/16W	Various		0603
3	S1, S2, S6		Switch SPDT, Ultra Mini Toggle	C&K Components	GT11MSCKE	SMD
2	S3, S4		Dual Diode	Various	BAV99	SOT-23
1	S5		Momentary Pushbutton Switch	Panasonic	SW_EVQ_QWX	SMD
2	S7, S8		Common Anode Dual Schottky Diode	On-Semiconductor	BAS40-06LT1	SOT-23
1	U1		Endura Multi-phase Controller	Intersil	ISL6566CR	MLFP-40
1	U2		MOSFET Driver IC	Intersil	HIP2100IB	SO-8
2	U3, U4		Low Profile DIP Switch, SPST, 6 Position	C&K Components	SD06H0SK	SMT
1	U5		8.00MHz Quartz Crystal	Citizen	HCM49-8.000MABJT	SMD

Bottom Layer Components

QTY	REFERENCE	VALUE	DESCRIPTION	VENDOR	PART NO.	PACKAGE
3	C24-C26	10µF	Capacitor, Ceramic, 16V, X7R, 10%	Various		1206
1	C56	1000pF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0603
2	C58, C59	2.2pF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0603
1	C60	1.0µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0805
1	C61	.01µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0603
2	C62, C63	0.1µF	Capacitor, Ceramic, 50V, X7R, 10%	Various		0603
1	Q22		General Purpose MOSFET	Various	2N7002	SOT-23

Bottom Layer Components (Continued)

QTY	REFERENCE	VALUE	DESCRIPTION	VENDOR	PART NO.	PACKAGE
19	R27-R29, R49, R51-R63, R65, R66	10kΩ	Resistor, 1%, 1/16W	Various		0603
1	R31	10.7kΩ	Resistor, 1%, 1/16W	Various		0603
1	R32	1.87kΩ	Resistor, 1%, 1/16W	Various		0603
2	R43, R44	2.43kΩ	Resistor, 1%, 1/16W	Various		0603
1	U6		8-bit microcontroller	Microchip	PIC16F873A-SO	SOIC-32W
2	U7, U8		Quad 2-to-1 Line Data Selector/Multiplexer	Texas Instruments	SN74HC157D	SOIC-16

ISL6566EVAL1 Layout

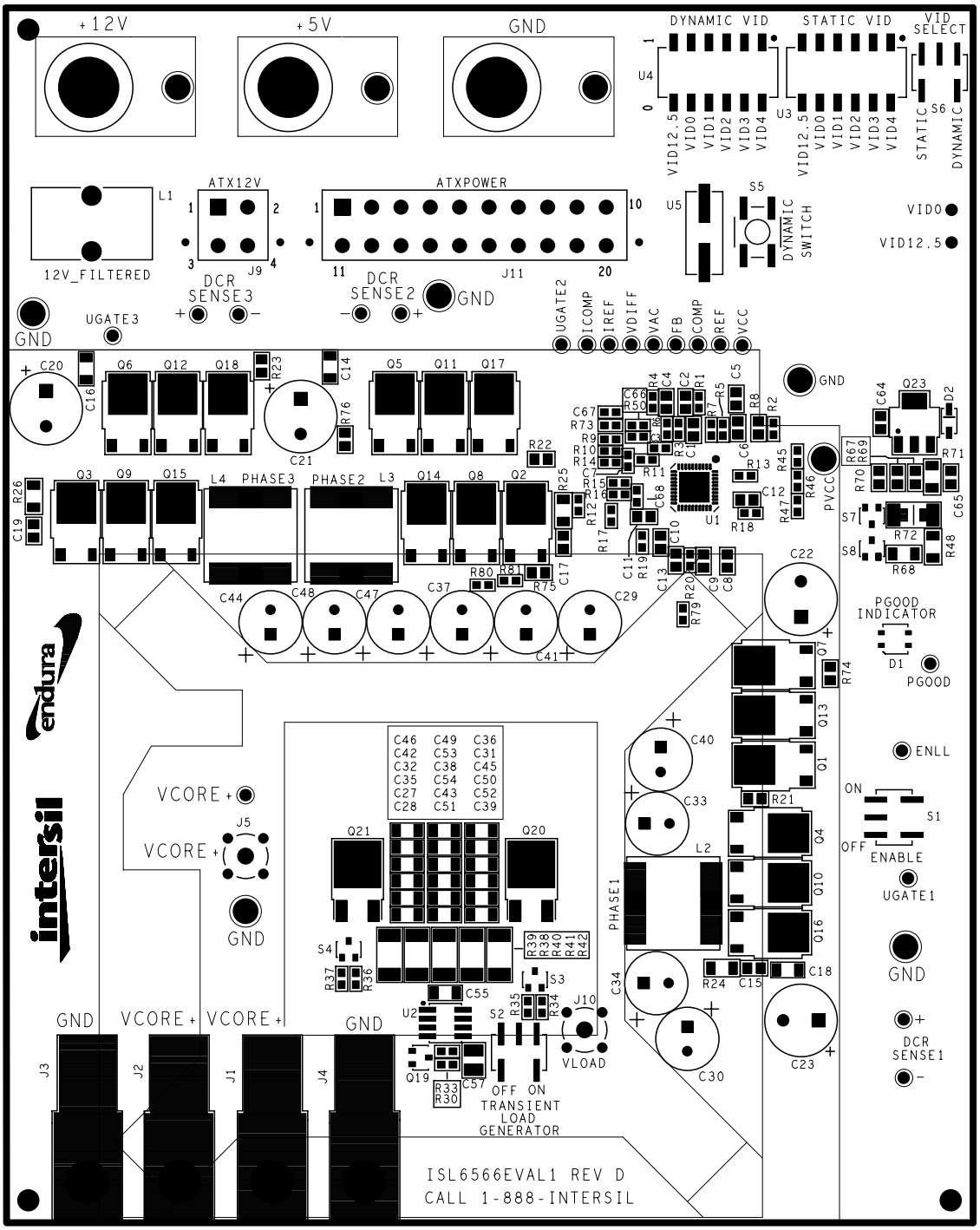


FIGURE 15. SILK SCREEN TOP

ISL6566EVAL1 Layout (Continued)

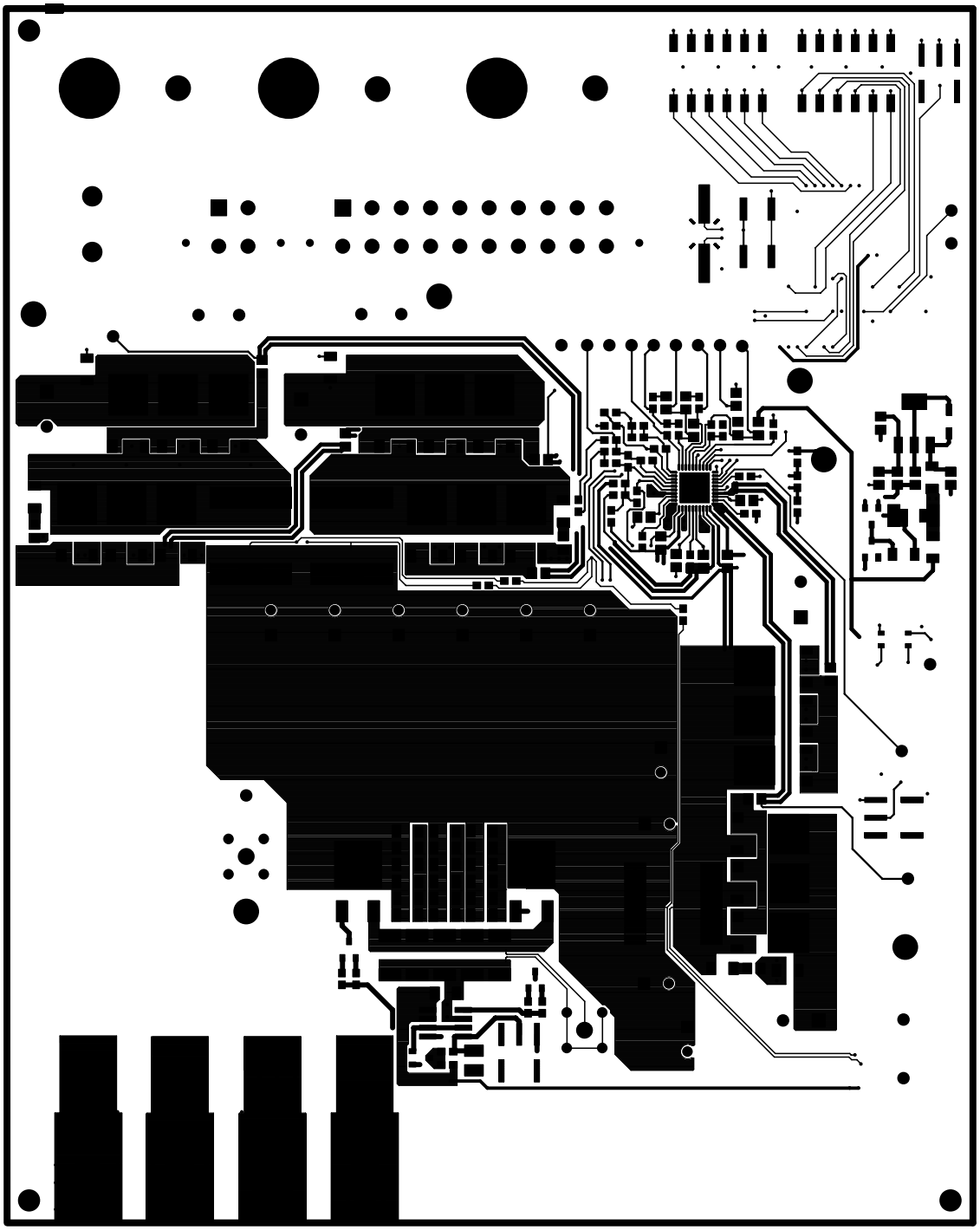


FIGURE 16. LAYER 1: TOP COPPER

ISL6566EVAL1 Layout (Continued)

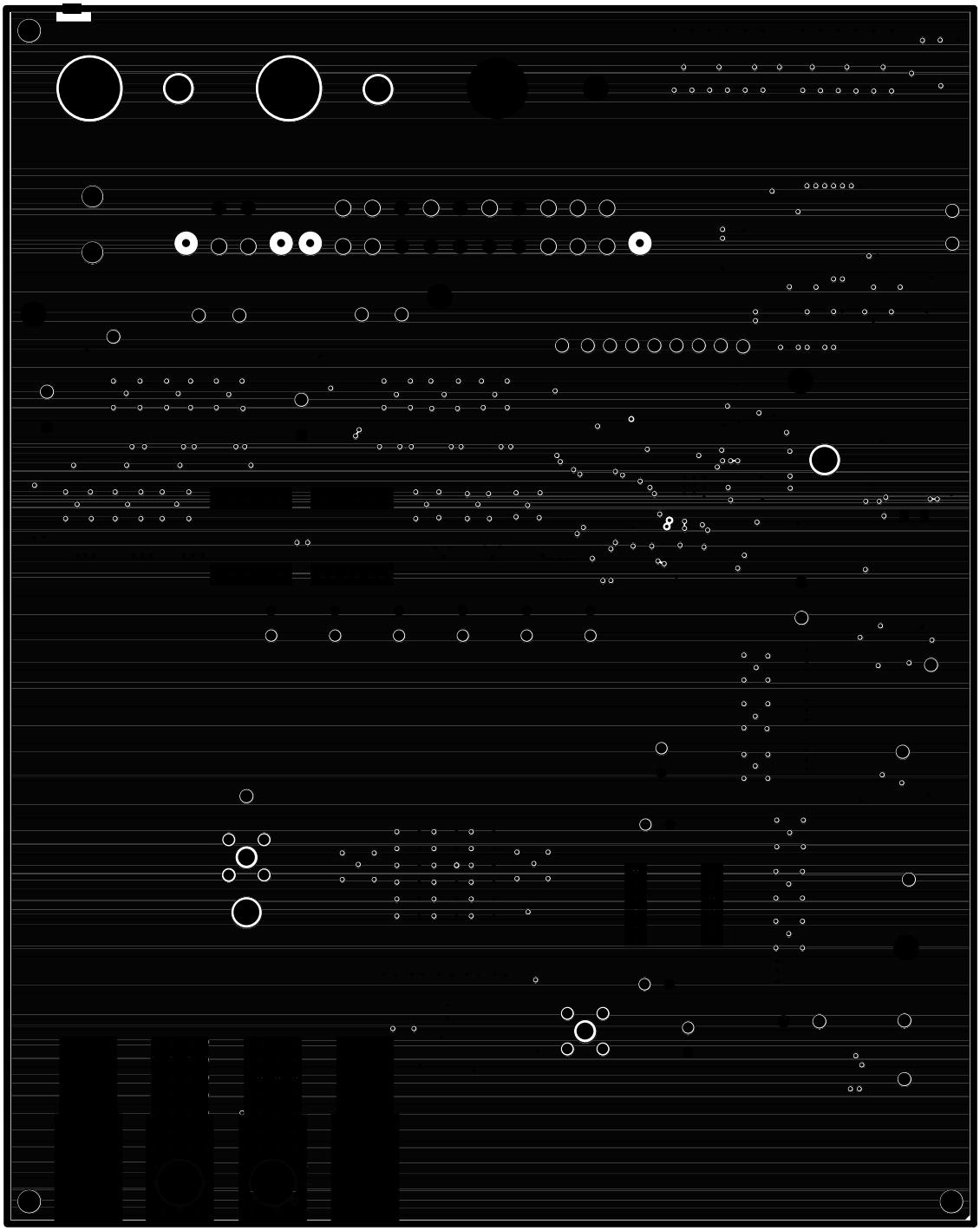


FIGURE 17. LAYER 2: GROUND PLANE

ISL6566EVAL1 Layout (Continued)

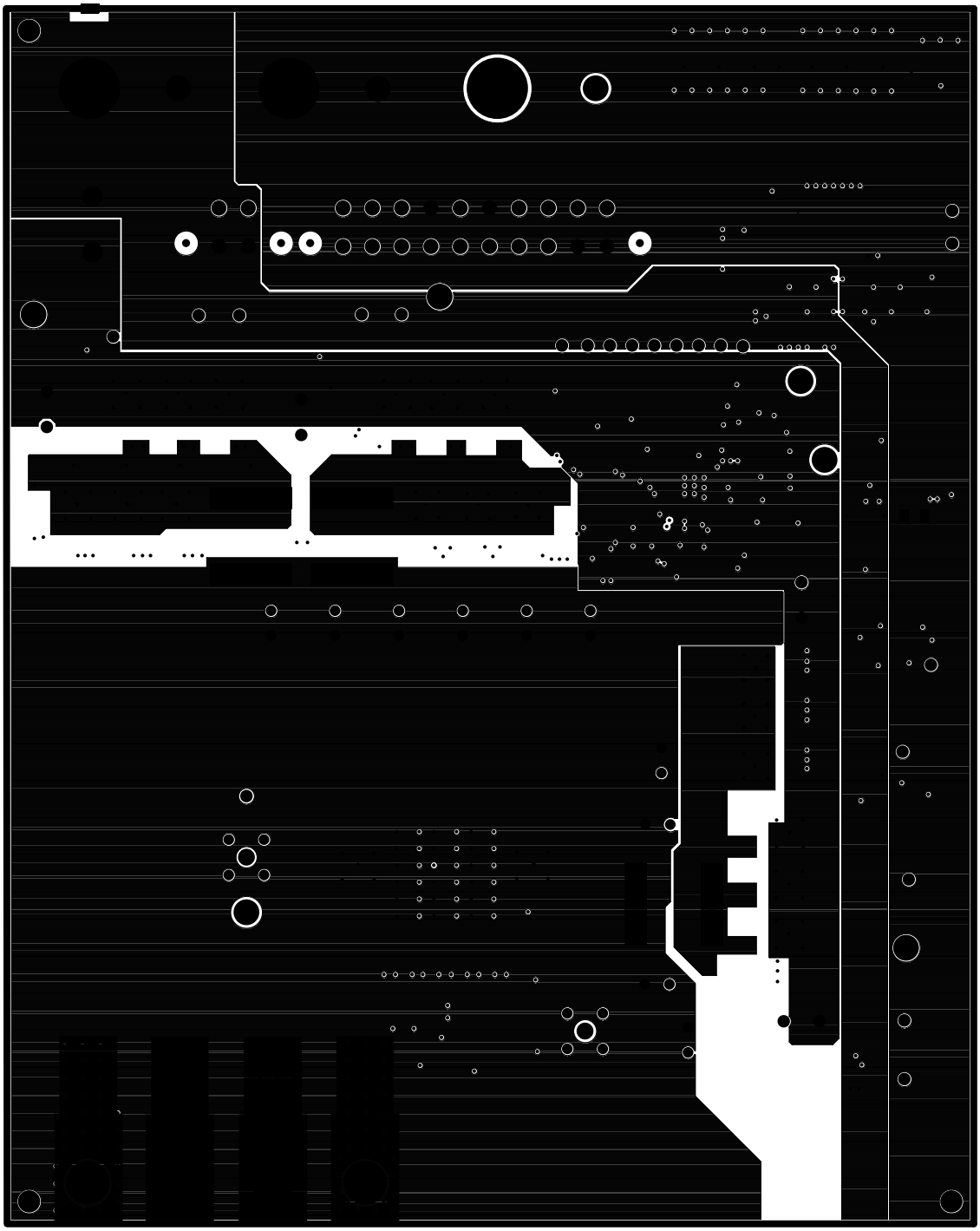


FIGURE 18. LAYER 3: POWER PLANE

ISL6566EVAL1 Layout (Continued)

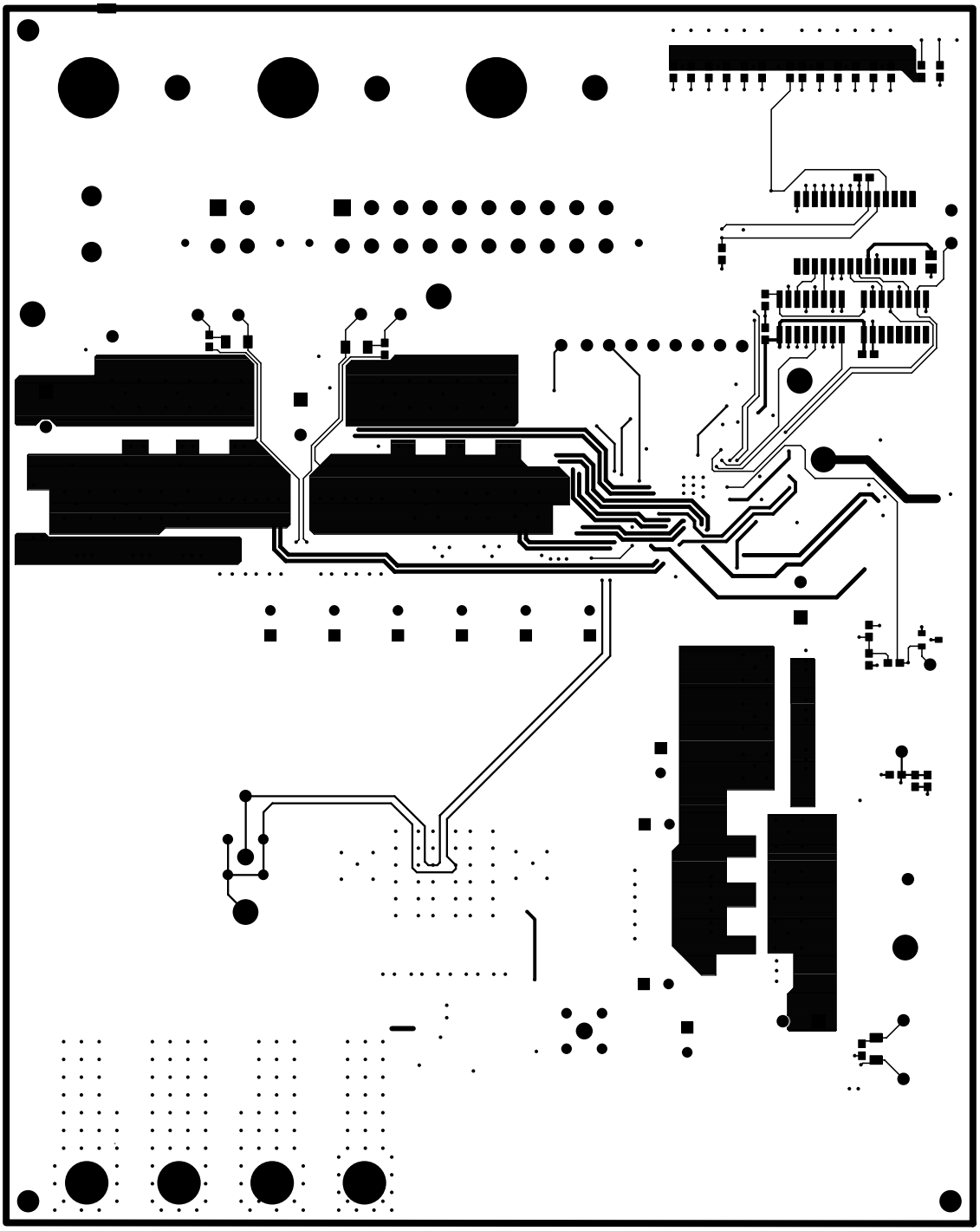


FIGURE 19. LAYER 4: BOTTOM COPPER

ISL6566EVAL1 Layout (Continued)

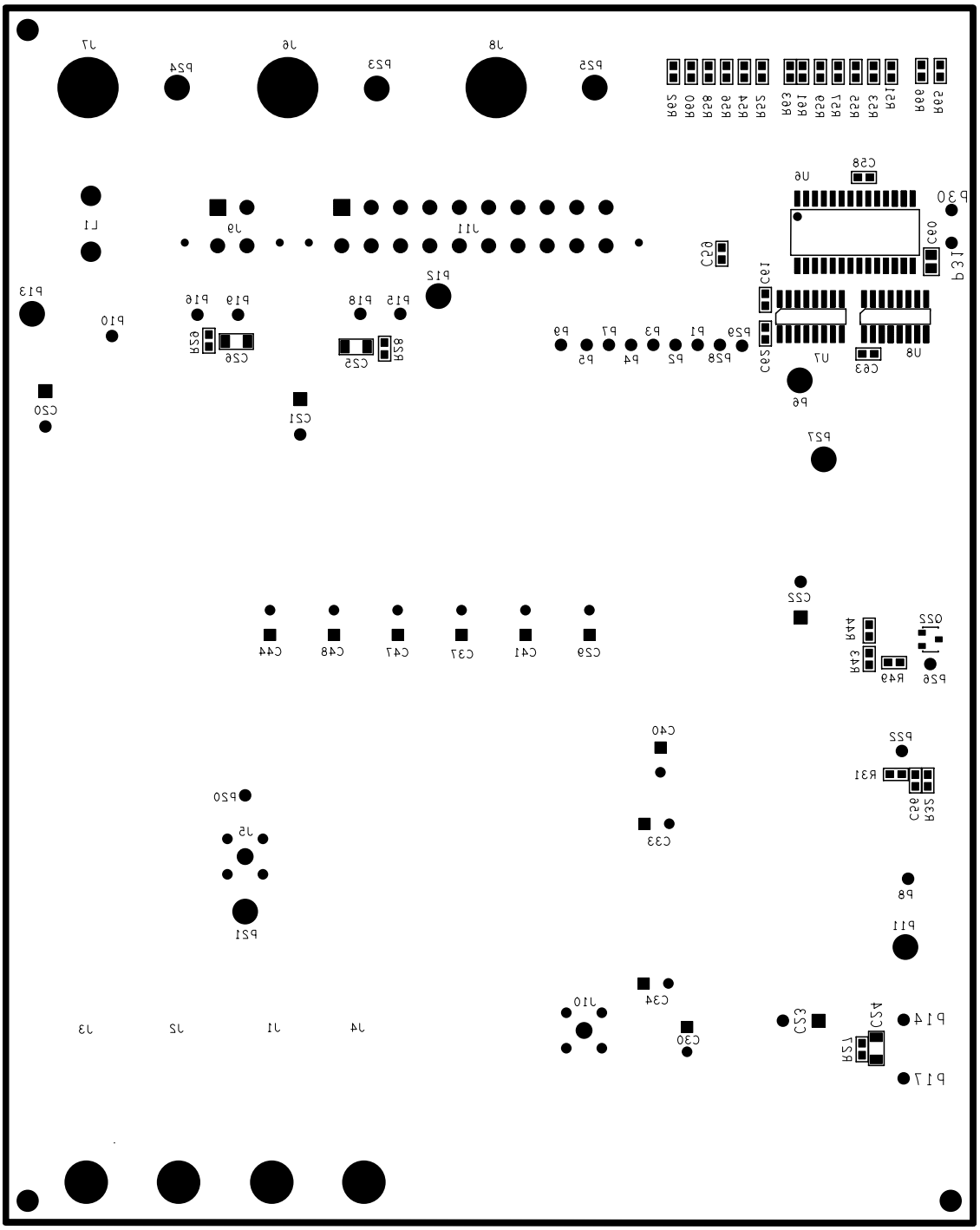


FIGURE 20. SILK SCREEN BOTTOM