

## Evaluating the AD7172-4 Low Power 24-Bit, 31.25 kSPS, Sigma-Delta ADC with True Rail-to-Rail Buffers

### FEATURES

Full featured evaluation board for the **AD7172-4**  
 PC control in conjunction with the system demonstration  
 platform (SDP, see the **EVAL-SDP-CB1Z** from  
 Analog Devices, Inc., for additional information)  
 PC software for control and data analysis (time domain)  
 Standalone capability

### EVALUATION KIT CONTENTS

**EVAL-AD7172-4SDZ** evaluation board  
 Evaluation software CD  
 7 V to 9 V ac to dc adapter  
 Plastic screw washer set

### EQUIPMENT NEEDED

DC signal source

### GENERAL DESCRIPTION

The **EVAL-AD7172-4SDZ** evaluation kit features the **AD7172-4**, a 24-bit, 31.25 kSPS analog-to-digital converter (ADC) with integrated rail-to-rail analog input buffers, on-board power supply regulation, and an external amplifier section for amplifier evaluation. A 7 V to 9 V ac to dc adapter is regulated to 5 V and 3.3 V; this voltage supplies the **AD7172-4** and support components. The **EVAL-AD7172-4SDZ** connects to a USB port via the SDP on the **EVAL-SDP-CB1Z** controller board.

The **EVAL-AD7172-4SDZ** evaluation software fully configures the **AD7172-4** device functionality via a user accessible register interface and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

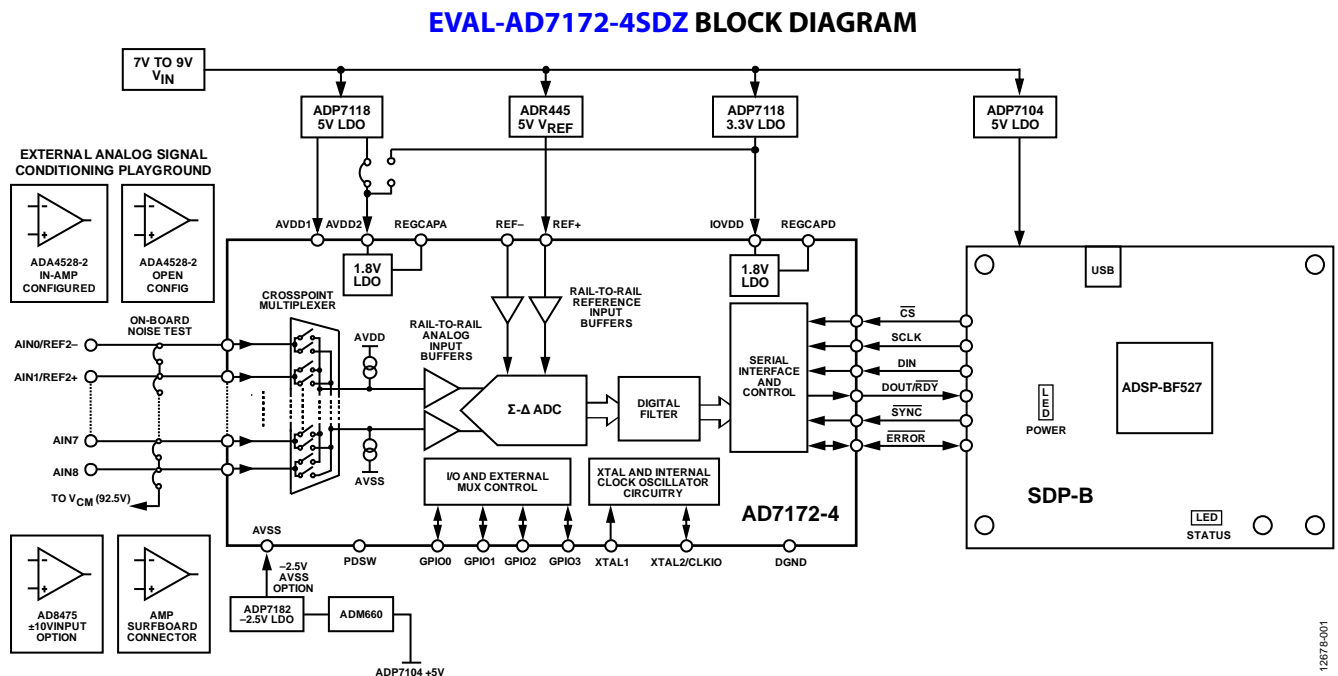


Figure 1.

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## REVISION HISTORY

8/15—Revision 0: Initial Version

## EVAL-AD7172-4SDZ QUICK START GUIDE

### RECOMMENDED QUICK START GUIDE

Follow these steps to set up the board:

1. Disconnect the [EVAL-SDP-CB1Z](#) board from the USB port of the PC.
2. Install the [EVAL-AD7172-4SDZ](#) software from the enclosed CD. Restart the PC after installation.
3. Connect the [EVAL-SDP-CB1Z](#) board to the [EVAL-AD7172-4SDZ](#) board, as shown in Figure 2.
4. Fasten the two boards with the enclosed plastic screw washer set.
5. Connect the external 9 V power supply to the J5 connector of the [EVAL-AD7172-4SDZ](#) board, as shown in Figure 2. Set LK2 to Position B.
6. Connect the [EVAL-SDP-CB1Z](#) to the PC via the USB cable. For Windows® XP, the user may need to search for the [EVAL-SDP-CB1Z](#) drivers.
7. Choose to automatically search for the drivers for the [EVAL-SDP-CB1Z](#) board if prompted by the Windows operating system.
8. Launch the [EVAL-AD7172-4SDZ](#) software from the Analog Devices subfolder in the **Programs** menu.

### QUICK START NOISE TEST

Use the following procedure to test the noise performance:

1. Insert Link LK8 to Link LK16 to initiate the noise performance test mode. In this mode, analog input channels short to  $V_{CM}$ , which is equal to 2.5 V.
2. Click **Sample** to acquire samples from the ADC (see Figure 7).

The **Samples** numeric control in the top right corner of the [AD7172-4 Evaluation Software](#) window sets the number of samples collected in each batch (see Figure 7).

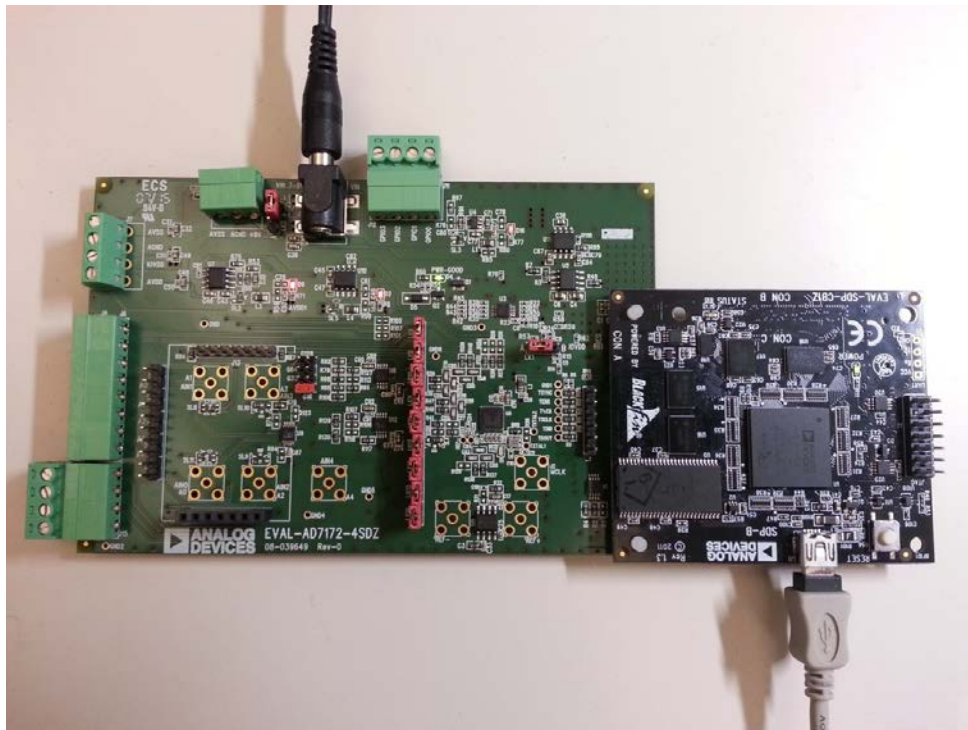


Figure 2. Hardware Configuration, Setting Up the [EVAL-AD7172-4SDZ](#)

## EVALUATION BOARD HARDWARE

### DEVICE DESCRIPTION

The [AD7172-4](#) is a highly accurate, high resolution, multiplexed, 4-/8-channel (fully differential/single-ended)  $\Sigma$ - $\Delta$  ADC. The [AD7172-4](#) has a maximum channel to channel scan rate of 6.21 kSPS (161  $\mu$ s) for fully settled data. The output data rates range from 1.25 SPS to 31.25 kSPS. The device includes integrated rail-to-rail analog input and reference input buffers, an integrated precision 2.5 V reference, and an integrated oscillator.

See the [AD7172-4](#) data sheet for complete specifications. Consult the data sheet in conjunction with this user guide when using the [EVAL-AD7172-4SDZ](#). Full details for the [EVAL-SDP-CB1Z](#) are available on the Analog Devices website.

### HARDWARE LINK OPTIONS

See Table 1 for default link options. By default, the [EVAL-AD7172-4SDZ](#) is configured to operate from the supplied 9 V ac to dc adapter connected to the J5 connector. The 5 V supply required for the [AD7172-4](#) comes from the on-board low dropout (LDO) regulator. The [ADP7118](#), with a 5 V output voltage, receives its input voltage from the J3 connector or the J5 connector (depending on the position of LK2) and generates a 5 V output.

**Table 1. Default Link and Solder Link Options**

Link	Default Option	Description
LK1	A	Selects the voltage applied to the power supply sequencer circuit (U3); dependent on AVDD1. Place in Position A if using 5 V AVDD1, or Position B if using 2.5 V AVDD1 and – 2.5 V AVSS.
LK2	B	Selects the external power supply from Connector J3 (Position A) or Connector J5 (Position B).
LK3 to LK7	Not inserted	Inserting these links sets up the on-board noise test prior to SL8 to SL11 to allow the inputs to the on-board amplifiers, U8 and U9, to be shorted. In this mode, all inputs short to $V_{CM}$ , which is equal to 2.5 V.
LK8 to LK16	Inserted	Inserting these links sets up the on-board noise test close to the ADC analog inputs. In this mode, all inputs short to $V_{CM}$ , which is equal to 2.5 V.
SL1	A	Sets the voltage applied to the AVDD2 pin. Operates using the AVDD1 supply (default). Position B sets the AVDD2 voltage to a 3.3 V supply from the <a href="#">ADP7118</a> (3.3 V) (U10) regulator.
SL2	A	Selects between an external or on-board AVDD1 source. Supplies AVDD1 from the <a href="#">ADP7118</a> (5 V) (U7) (default).
SL3	A	Selects between an external or on-board AVSS source. Supplies AVSS from the <a href="#">ADP7182</a> (–2.5 V) (U4) (default).
SL4	C	Connects AIN4 to: A4/J6 (Position A); $V_{CM}$ , which is equal to 2.5 V (Position B); or AVSS (Position C). Position B and Position C are used to simplify the use of a single-ended input source.
SL5	B	Selects between an external or on-board IOVDD source. Supplies IOVDD from the <a href="#">ADP7118</a> (3.3 V) (U10) (default). The evaluation board operates with a 3.3 V logic.
SL8	A	Routes A0 to: the AIN0/REF2– pin on the <a href="#">AD7172-4</a> (Position A), Buffer/In-Amp U8 (Position B), Funnel Amp U9 with gain of 0.8 $\times$ (Position C), or J10-1 (Position D).
SL9	A	Routes A2 to: the AIN2 pin on the <a href="#">AD7172-4</a> (Position A), Buffer U12 (Position B), or Funnel Amp U9 gain of 0.4 $\times$ (Position C).
SL10	A	Routes A3 to: the AIN3 pin on the <a href="#">AD7172-4</a> (Position A), Buffer U12 (Position B), or Funnel Amp U9 gain of 0.4 $\times$ (Position C).
SL11	A	Routes A1 to: the AIN1/REF2+ pin on the <a href="#">AD7172-4</a> (Position A), Buffer/In-Amp U8 (Position B), Funnel Amp U9 with gain of 0.8 $\times$ (Position C), or J10-7 (Position D).
G16	Inserted	Sets the on-board U8 in-amp to a gain of 16. Insert only one of G16, G32, G64, or G128 at a time.
G32	Not Inserted	Sets the on-board U8 in-amp to a gain of 32. Insert only one of G16, G32, G64, or G128 at a time.
G64	Not Inserted	Sets the on-board U8 in-amp to a gain of 64. Insert only one of G16, G32, G64, or G128 at a time.
G128	Not Inserted	Sets the on-board U8 in-amp to a gain of 128. Insert only one of G16, G32, G64, or G128 at a time.
R49 to R51	Inserted	Connects AVSS and AGND for single-supply operation. To operate in split supply mode, remove these links.

**SOCKETS AND CONNECTORS**

**Table 2. Connector Details**

Connector	Function	Connector Type	Manufacturer	Manufacturer Number	Order Code <sup>1</sup>
J1	Connector to the <a href="#">EVAL-SDP-CB1Z</a>	120-way connector, 0.6 mm pitch	Hirose	FX8-120S-SV(21)	FEC1324660
J2	External MCLK input	Straight PCB mount SMB/SMA jack	Tyco	1-1337482-0	Not applicable
J3	External bench top voltage supply for the <a href="#">EVAL-AD7172-4SDZ</a>	Power socket block, 3-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 3-G-3,81	FEC3704737
J5	External ac to dc adapter input for the <a href="#">EVAL-AD7172-4SDZ</a> , 7 V to 9 V	DC power connectors, 2 mm SMT power jack	Kycon	KLDX-SMT2-0202-A	MOUSER 806-KLDX-SMT20202A
J6	Analog input terminal block; wired connection to external source or sensor	Power socket block, 8-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 8-G-3,81	FEC3704774
J9	External bench top voltage supply option for AVDD1/AVDD2, IOVDD, and AVSS inputs on the <a href="#">AD7172-4</a>	Screw terminal block, 3.81 mm pitch	Phoenix Contact	MKDS 1/4-3.81	FEC3704592
J10	Optional header	7-way, 2.54 mm pin header	Samtec	SSW-107-01-T-S	FEC1803478
J13	Optional header	7-way, 2.54 mm socket	Samtec	TLW-107-05-G-S	FEC1668499
A0 to A4	Analog inputs to ADC	Straight PCB mount SMB/SMA jack	Tyco	1-1337482-0	Not applicable
A7	Pmod™-compatible header	6-pin single inline header (0.1 inch pitch)	Harwin	20-9990646	FEC 1022255

<sup>1</sup> Order codes starting with FEC are for Farnell.

**SERIAL INTERFACE**

The [EVAL-AD7172-4SDZ](#) connects via the serial peripheral interface (SPI) to the Blackfin® [ADSP-BF527](#) on the [EVAL-SDP-CB1Z](#). There are four input signals: CS, SCLK, DIN, and SYNC, and one output signal from the ADC, DOUT/RDY (see Figure 1).

To operate the [EVAL-AD7172-4SDZ](#) in standalone mode, disconnect the evaluation board from the [EVAL-SDP-CB1Z](#) controller board. Use the test points labeled on the [EVAL-AD7172-4SDZ](#) to connect the signals to an alternative digital capture setup or the Pmod-compatible header (A7).

**POWER SUPPLIES**

Power the [EVAL-AD7172-4SDZ](#) from the ac to dc adapter connected to J5, or from an external bench top supply applied to J3 or J9. Linear LDO regulators generate the required voltages from the applied input voltage (V<sub>IN</sub>) rail when using J3 or J5. Use J9 to bypass the on-board regulators. An [ADP7118](#) regulator generates the 5 V (single-supply) and 2.5 V (split supply) supplies for the AVDD1 and AVDD2 rails to the ADC; a second [ADP7118](#) generates 3.3 V for the IOVDD rail. The [ADP7104](#) supplies 5 V for the [EVAL-SDP-CB1Z](#) controller board as well as 5 V for the [ADM660](#) voltage converter to generate -5 V to supply the [ADP7182](#). The [ADP7182](#) generates the -2.5 V supply for AVSS when operating in split supply mode. Each supply is decoupled where it enters the board and again at each device in accordance with the schematic (available for download at <http://www.analog.com/EVAL-AD7172-4>, including a bill of materials). Table 3 shows the various power supply configurations available, including split supply operation.

Table 3. Power Supply Configurations<sup>1</sup>

Configuration	Input Voltage Range	Description
Single Supply (Regulated)	7 V to 9 V	The 7 V to 9 V input is regulated to 5 V for AVDD1/AVDD2 and 3.3 V for IOVDD. This also powers the external 5 V reference. See the Single-Supply (Regulated) section.
Single Supply (Unregulated)	7 V to 9 V, 5 V, and 3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Single Supply (Unregulated) section.
Split Supply (Regulated)	7 V to 9 V	The 7 V to 9 V input is regulated to 2.5 V for AVDD1/AVDD2, -2.5 V for AVSS and 3.3 V for IOVDD. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Regulated) section.
Split Supply (Unregulated)	7 V to 9 V, ±2.5 V, and 3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Unregulated) section.

<sup>1</sup> Only one configuration can be used at a time.

## POWER SUPPLY CONFIGURATIONS

### Single-Supply (Regulated)

There are two available power supply options for the single supply (regulated) configuration.

- Connect the ac to dc adapter (included) to J5 and set LK2 to Position B.
- Connect the bench top power supply to J3, set LK2 to Position A, and ensure that AVSS = AGND = 0 V.

Set all other links and solder links to the default settings as outlined in Table 1.

### Single Supply (Unregulated)

To set up the board, use the following procedure:

1. Move SL2 and SL5 to Position A.
2. Connect the two terminals of J9 (AGND and AVSS).
3. Connect the 0 V input (GND) to J9 at the AGND terminal.
4. Connect the 5 V input to J9 at the AVDD terminal.
5. Connect the 3.3 V input to J9 at the IOVDD terminal.
6. Connect the 7 V to 9 V input to J5.

Set all other links and solder links to the default settings as outlined in Table 1.

### Split Supply (Regulated)

To set up the board, use the following procedure:

1. Remove R49 to R51. These links connect AVSS to AGND.
2. Insert a 0 Ω resistor at R85.
3. Set LK1 to Position B, which sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.
4. Connect a bench top power supply to J5 and set LK2 to Position B.

Set all other links and solder links to the default settings as outlined in Table 1.

### Split Supply (Unregulated)

To set up the board, use the following procedure:

1. Move SL2, SL3, and SL5 to Position A.
2. Remove R49 to R51.
3. Connect the 0 V input (GND) to J9 at the AGND terminal.
4. Connect the 2.5 V input to J9 at the AVDD terminal.
5. Connect the -2.5 V input to J9 at the AVSS terminal.
6. Connect the 3.3 V input to J9 at the IOVDD terminal.
7. Connect the 7 V to 9 V input to J5.
8. Set LK1 to Position B, which sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links to the default settings as outlined in Table 1.

## ANALOG INPUTS

The [EVAL-AD7172-4SDZ](#) primary analog inputs can be applied in two separate ways.

- At the J6 connector on the left side of the board
- At the A0 to A4 SMB/SMA footprints on the evaluation board

The analog inputs route directly to the associated analog input pins on the [AD7172-4](#) provided that the LK3 to LK16 links (on-board noise test) are removed. The [EVAL-AD7172-4SDZ](#) software is set up to analyze dc inputs to the ADC. The [AD7172-4](#) input buffers work for dc input signals.

## REFERENCE OPTIONS

The [EVAL-AD7172-4SDZ](#) includes an external 5 V reference, the [ADR445](#). This reference connects to the REF+ input, and the REF- input is connected to AVSS. The [AD7172-4](#) has a second reference input, AIN0/REF2- and AIN1/REF2+. There are also two SMB/SMA footprints for connecting an external voltage reference source of the [ADR445](#).



# EVALUATION BOARD SOFTWARE

## SOFTWARE INSTALLATION

The EVAL-AD7172-4SDZ evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the installer. The default installation location for the software is **C:\Program Files\Analog Devices\EVAL-AD7172-4SDZ\**.

Install the evaluation software before connecting the EVAL-AD7172-4SDZ and the EVAL-SDP-CB1Z to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

To install the software, take the following steps:

1. Install the EVAL-AD7172-4SDZ software.
2. Install the EVAL-SDP-CB1Z system demonstration platform board drivers.
3. Place the software and drivers in the appropriate locations by proceeding through all of the installation steps.
4. Connect the EVAL-SDP-CB1Z board to the PC only after the software and drivers install.

The installer may prompt you to allow the program to make changes to the computer. Click **Yes** to proceed (see Figure 3).

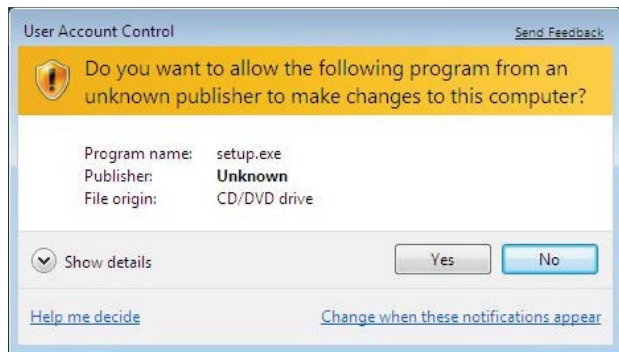


Figure 3. AD7172-4 User Account Control Permission Dialog Box

You may receive a security warning as part of the EVAL-SDP-CB1Z controller board driver installation. Click **Install** to proceed with the installation of the driver (see Figure 4). Without this confirmation, the software cannot operate correctly.

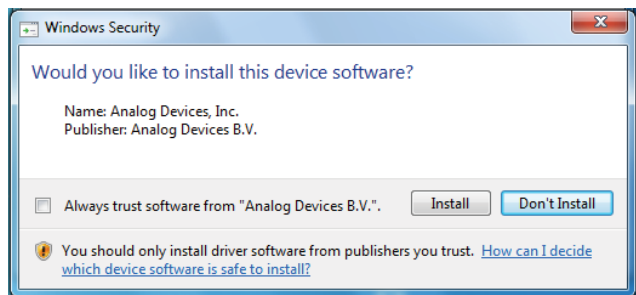


Figure 4. EVAL-SDP-CB1Z Drivers Installation Confirmation Dialog Box

After installation is complete, connect the EVAL-AD7172-4SDZ to the EVAL-SDP-CB1Z, as shown in Figure 2. Connect the EVAL-SDP-CB1Z board via the USB cable to the computer.

Follow these steps to verify the EVAL-SDP-CB1Z controller board driver is installed and working correctly:

1. Run the **Found New Hardware Wizard** (this window opens up automatically when the EVAL-SDP-CB1Z connects to the computer).
2. After the drivers are installed, check that the board has connected correctly by going to the **Device Manager** of the PC. Go to **My Computer > Manage > Device Manager**, (see Figure 5).
3. The **EVAL-SDP-CB1Z** appears under the **ADI Development Tools** as **Analog Devices System Development Platform (32MB)** or a similar title.

These steps confirm the installation is complete.

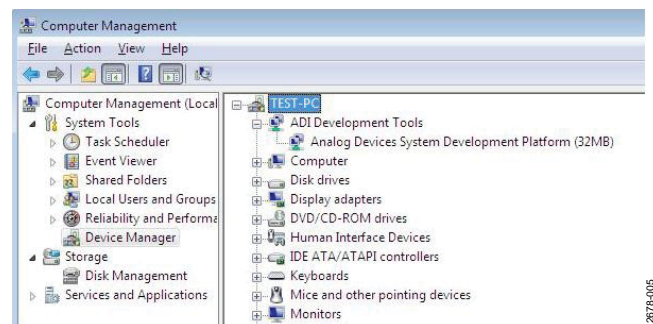


Figure 5. Device Manager

## LAUNCHING THE SOFTWARE

The AD7172-4 software can be launched when the EVAL-AD7172-4SDZ and EVAL-SDP-CB1Z are correctly connected to the PC.

To launch the AD7172-4 software, complete the following steps:

1. From the **Start** menu, click **Programs > Analog Devices > EVAL-AD7172-4SDZ**. The main window of the software displays (see Figure 7).
2. If the AD7172-4 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, the **Select Interface...** dialog box appears (see Figure 6).
3. Connect the evaluation board to the USB port of the PC, wait a few seconds, and click the green double arrows, shown in Figure 6, to rescan the USB ports. When connected, click **Work Online** to proceed (see Figure 6).

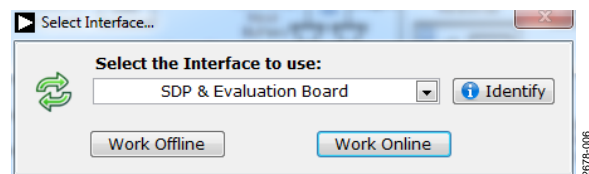


Figure 6. Select Interface Dialog Box

# EVALUATION BOARD SOFTWARE OPERATION

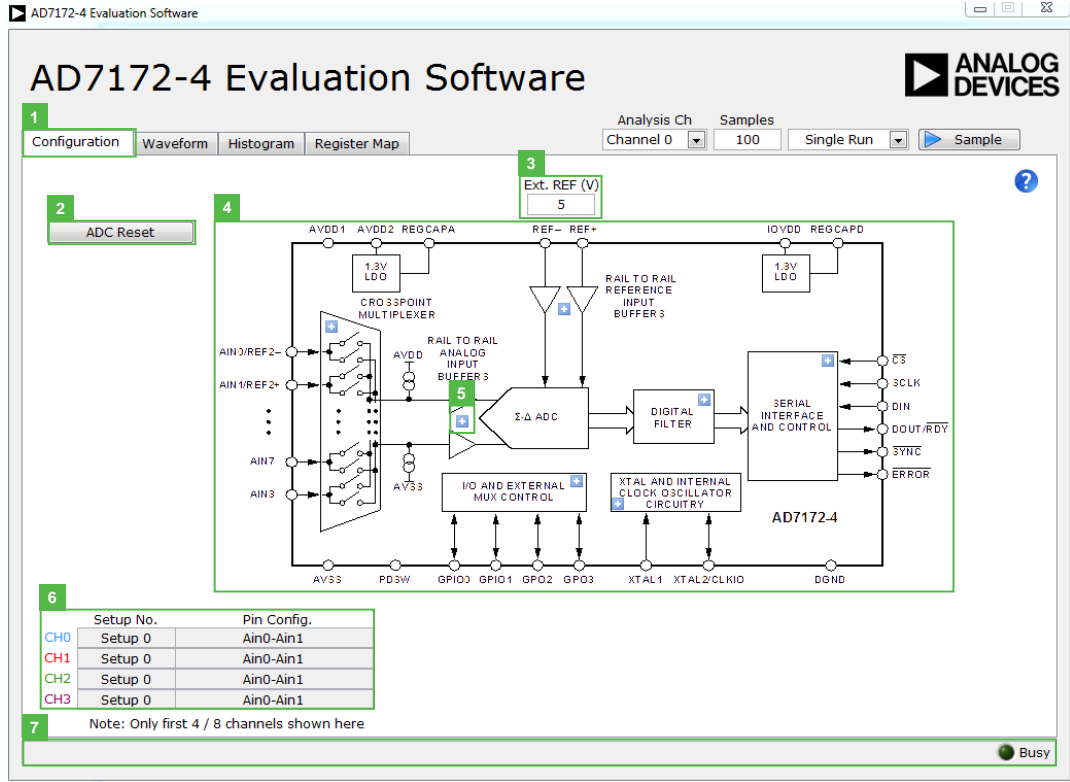


Figure 7. Configuration Tab of the AD7172-4 Evaluation Software

## OVERVIEW OF THE MAIN WINDOW

The main window of the software displays the control buttons and analysis indicators of the AD7172-4 evaluation board software (see Figure 7). This window is divided into four tabs: **Configuration**, **Waveform**, **Histogram**, and **Register Map**.

## CONFIGURATION TAB

See Figure 7 for the **Configuration** (1) tab.

### ADC Reset

Click the **ADC Reset** (2) button to perform a software reset of the AD7172-4 (see Figure 7). The AD7172-4 does not have a hardware reset pin. Perform a hard reset by removing power to the board. The software reset has the same effect as a hard reset.

### External Reference

The **Ext. REF (V)** (3) box sets the external reference voltage used for calculating the results on the **Waveform** and **Histogram** tabs (see Figure 7). The evaluation board has an external 5 V ADR445 reference that can be disconnected by removing R32. You can change the external reference voltage value within this box to ensure the correct calculation of results on the **Waveform** and **Histogram** tabs.

## Functional Block Diagram

The functional block diagram (4) of the ADC shows each of the separate functional blocks within the ADC (see Figure 7). Click one of the configuration buttons in this graph to open the configuration pop-up window for that block. Not all blocks have a configuration button.

### Configuration Pop-Up Button

The configuration pop-up button (5) opens a window that allows configuration of the relevant functional block (see Figure 7).

### Channel Configuration Overview

The channel configuration overview (6) section shows the channel configuration, including setup and analog inputs (see Figure 7). This provides a quick assessment of how the ADC is set up.

### Status Bar

The status bar (7) displays status updates such as **Analysis Completed** and **Reset Completed** during software use, as well as the software version and **Busy** indicator (see Figure 7).



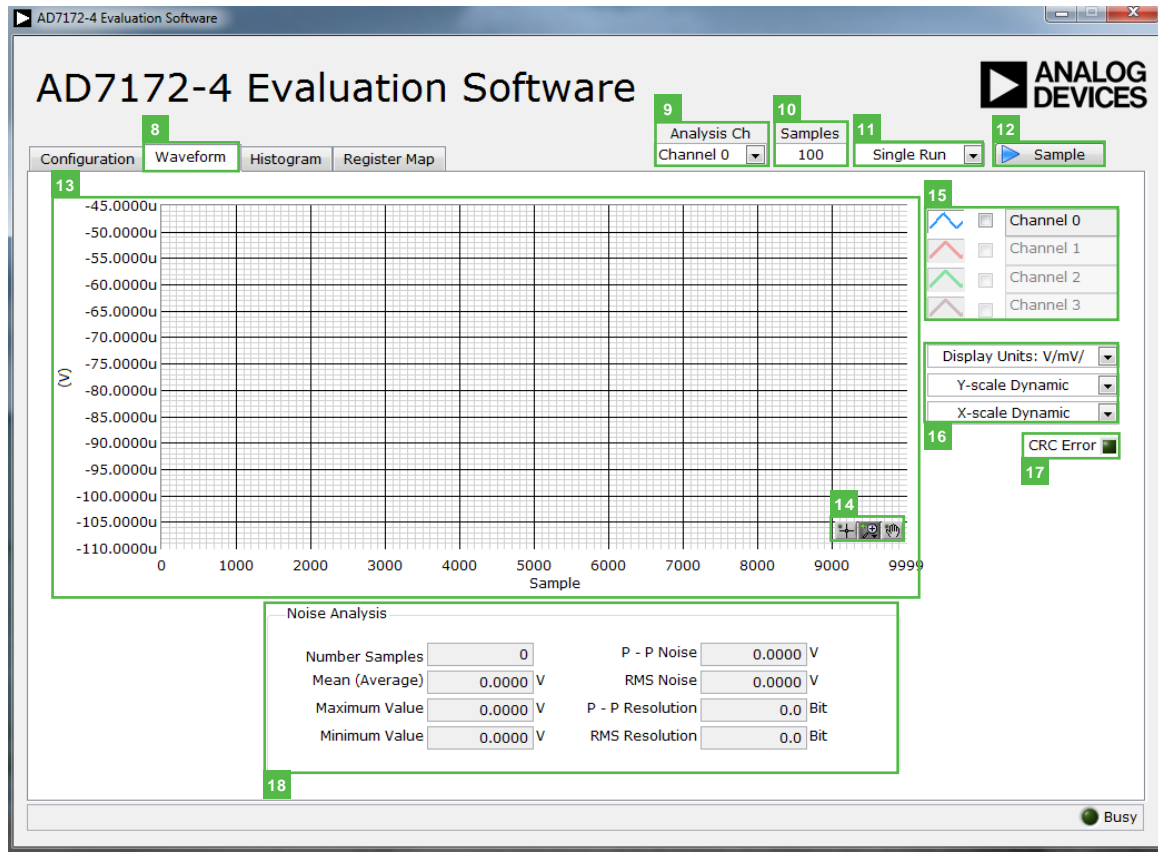


Figure 8. **Waveform** Tab of the **AD7172-4 Evaluation Software**

## WAVEFORM TAB

See Figure 8 for the **Waveform** (8) tab.

### Analysis Channel

The **Noise Analysis** (18) section and waveform graph shows the analysis of the channel selected via the **Analysis Ch** (9) drop-down combo box (see Figure 8).

### Samples

The **Samples** (10) numeric control and batch control (11) set the number of samples gathered per batch and indicate whether only a single batch or multiple batches of samples are gathered. The **Samples** (10) numeric control is unrelated to the ADC mode. You can capture a defined sample set or continuously gather batches of samples. In both cases, the number of samples set in the **Samples** (10) numeric input dictates the number of samples (see Figure 8).

### Sample

Click the **Sample** (12) button to start gathering ADC results. Results appear in the waveform graph (13) (see Figure 8).

### Waveform Graph and Controls

The data waveform graph (13) shows each successive sample of the ADC output. The control toolbar (14) in the graph allows you to zoom in on the data. Click the x-axis and y-axis to change the scales on the graph (see Figure 8).

### Channel Selection

The channel selection (15) control allows you to choose which channels display on the data waveform (see Figure 8). These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

### Display Units and Axis Controls

In the display units and axis controls section (16), click the **Display Units: V/mV** drop-down combo box to select whether the data graph displays in units of voltages or codes (see Figure 8). This selection affects both the waveform graph and the histogram graph. The axis controls can be dynamic or fixed. When **Y-scale Dynamic** and **X-scale Dynamic** are switched on, the axes automatically adjust to show the entire range of the ADC results after each sample batch. Click the drop down arrows to select the **Fixed** option to program the axis ranges to not adjust after each sample batch.

### CRC Error

The **CRC Error** (17) LED icon illuminates when a cyclic redundancy check (CRC) error is detected in the communications between the software and the **AD7172-4** (see Figure 8). The CRC functionality on the **AD7172-4** is disabled by default and must be enabled for this indicator to work.

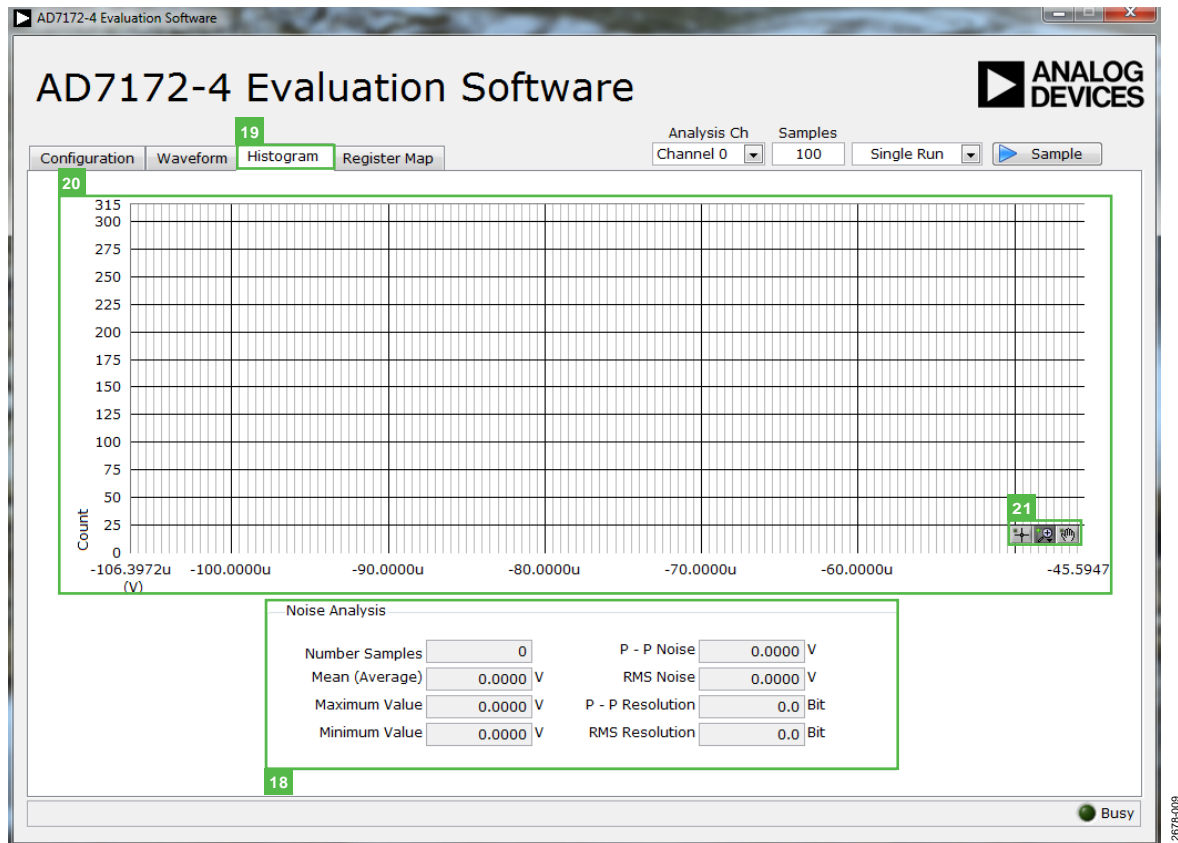


Figure 9. Histogram Tab of the AD7172-4 Evaluation Software

### Noise Analysis

The Noise Analysis (18) section displays the results of the noise analysis for the selected analysis channel (see Figure 8). This section includes both noise and resolution measurements.

### HISTOGRAM TAB

See Figure 9 for the Histogram (19) tab.

### Histogram Graph and Controls

The data histogram graph (20) shows the number of times each sample of the ADC output occurs. The control toolbar (21) in the histogram graph allows you to zoom in on the data (see Figure 9). Click the x-axis and y-axis to change the scales on the graph (see Figure 9).

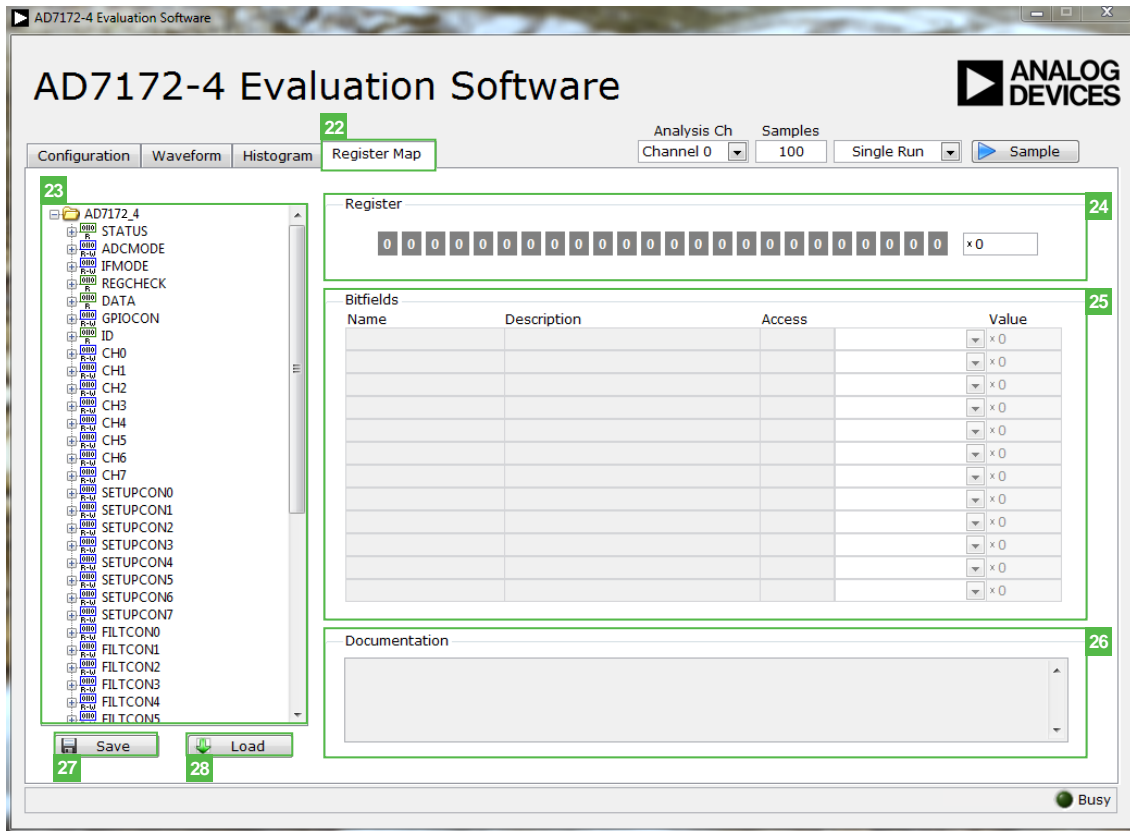


Figure 10. Register Map Tab of the AD7172-4 Evaluation Software

**REGISTER MAP TAB**

See Figure 10 for the Register Map (22) tab.

**Register Tree**

The register tree (23) control shows the full register map in a tree control. Each register is shown. Click the expand button next to each register to show all the bit fields contained within that register (see Figure 10).

**Register**

The Register (24) control allows you to change the individual bit of the register selected in the register tree (23). Click on the bit in the register tree (23) or program the register value directly into the number control on the right (see Figure 10).

**Bitfields**

The Bitfields (25) list shows all the bit fields of the register selected in the register tree (23). Change the values using the drop-down menu or by directly entering a value into the Value number control on the right (see Figure 10).

**Documentation**

The Documentation (26) field contains the documentation for the register of bit field selected in the register tree (23) (see Figure 10).

**Save and Load**

The Save (27) and Load (28) buttons allow you to save the current register map setting to a file and load the setting from the same file (see Figure 10).

**EXITING THE SOFTWARE**

To exit the software, click the close button at the top right corner of the AD7172-4 Evaluation Software window (see Figure 7).

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Legal Terms and Conditions**

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.