

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1049

TRIPLE OUTPUT, HIGH POWER, HIGH EFFICIENCY POE PD

LTC4264CDE, LTC3825EFE

DESCRIPTION

Demonstration circuit 1049 is a high-power triple output supply featuring the LTC4264 with the LTC3825. This board acts as a pre-standard high power Power-over-Ethernet (PoE) Powered Device (PD) and connects at the RJ45 to a compatible high power Power Sourcing Equipment (PSE) device. The LTC4264 provides IEEE802.3af standard PoE PD interfacing. When the PD is fully powered, the LTC4264 switches power over to the LTC3825 through an on-board high power MOSFET.

The highly-integrated LTC3825, small supply utilizes an isolated flyback topology with synchronous rectifi-

cation that requires no opto-isolator allowing for low-parts count. The DC1049 output supplies are 5V @ 2A, 11.8V @ 0.27A, and 3.3V @ 2.5A.

DC1049 also demonstrates the use of an auxiliary 24V wall adapter. When present, the auxiliary supply becomes the dominant supply over PoE to provide power to the LT3825.

Design files for this circuit board are available. Call the LTC factory.

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Table 1. Typical Performance Summary ($T_A = 25^\circ\text{C}$)

PARAMETER	CONDITION	VALUE
PoE Input Voltage	In from PSE	37V to 57V
PoE Input High Current Limit	I_{LIM_EN} Enabled, Nominal Current	750mA
	I_{LIM_EN} Disabled, Nominal Current	1.45A
PoE Signature Resistance	SHDN Enabled	23.25k Ω to 26.00k Ω
	SHDN Disabled, Maximum Value	11.8k Ω
24V Auxiliary Input Voltage	In from Auxiliary Supply	22.8V to 57V
Output Voltage V_{OUT} (NOTE)	V_{IN} from PoE	5V $\pm 2.5\%$ @ 2A
		11.8V $\pm 2\%$ @ 0.27A
	V_{IN} from 24V $\pm 5\%$ Auxiliary Supply	3.3V $\pm 3\%$ @ 2.5A
		5V $\pm 2.5\%$ @ 2A
Typical Output Ripple V_{OUT}	$V_{IN} = 48V$	11.8V $\pm 2\%$ @ 0.27A
		3.3V $\pm 3\%$ @ 2.5A
		5V: < 20mVpp @ 2A
Nominal Switching Frequency		250kHz
Isolation Voltage		1500VDC

NOTE: Output power is rated to not exceed PoE maximum input power with I_{LIM_EN} Enabled.

QUICK START PROCEDURE

DC1049 is easy to set up to evaluate the performance of the LTC4264 with the LTC3825 in a high power PD application. Refer to Figure 1 and Figure 2 for proper measurement equipment setup and follow the procedure below:

1. Place test equipment (voltmeters, ammeters, and loads) across outputs 5V, 11.8V, and 3.3V.
2. Input Supply Options:
 - a) PoE: Connect a high power PSE with a CAT5 cable to RJ45 connector J1 or 37V to 57V op-

tion applied across V+ and POE- if PSE is not available (diode bridge is bypassed).

- b) Auxiliary: Connect a 24V Auxiliary Supply at J3 or 22.8V to 57V option applied across AUX+ and AUX- if wall adapter is not available.
3. Check for the proper output voltages 5V, 11.8V, and 3.3V.
 4. Once the proper output voltages are established, adjust the loads within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

OPERATING PRINCIPLES

A compatible high power PSE is connected to the DC1049 at the RJ45 connector J1. A diode bridge is required by IEEE802.3af across the data pairs and spare pairs. Schottky diodes are used at the input to improve efficiency over standard diode bridges. A high power specific Ethernet transformer is used on the data pairs. The LTC4264 provides IEEE802.3af standard PoE 25k signature resistance and has the option of displaying a power class through jumper JP3. When the PD is fully powered, the LTC4264 limits the inrush current. When voltage is above the turn on UVLO, the LTC4264 signals a power good to the LTC3825 to begin operation and switches power through its onboard power MOSFET. The LTC4264 implements a high current limit of 750mA. Higher currents are allowed by disabling the current limit through JP2 on the DC1049. The LTC4264 can also be shutdown through JP1 to disable the functions including turning off the internal MOSFET and presenting an invalid signature resistance to a PSE.

Once power is switched over to the LTC3825, the device regulates the output voltages by sensing the average of all the output voltages via a transformer winding during the flyback time. This allows for tight output regulation without the use of an opto-isolator, providing improved dynamic response and reliability. Synchronous rectification increases the conversion efficiency and cross-regulation effectiveness above a conventional flyback topology. No external driver ICs or delay circuits are needed to achieve synchronous rectification; a single resistor is all that is needed to program the synchronous rectifier's timing.

The DC1049 also demonstrates accepting input power from a 24V auxiliary supply (wall wart) connected at J3. When present, the LTC4264 is disabled through Q5 to give the auxiliary supply priority over supplying power to the output and not require power from a PSE. In a high power PD application that does not use the auxiliary supply, D15 can be shorted for higher efficiency in the PD.

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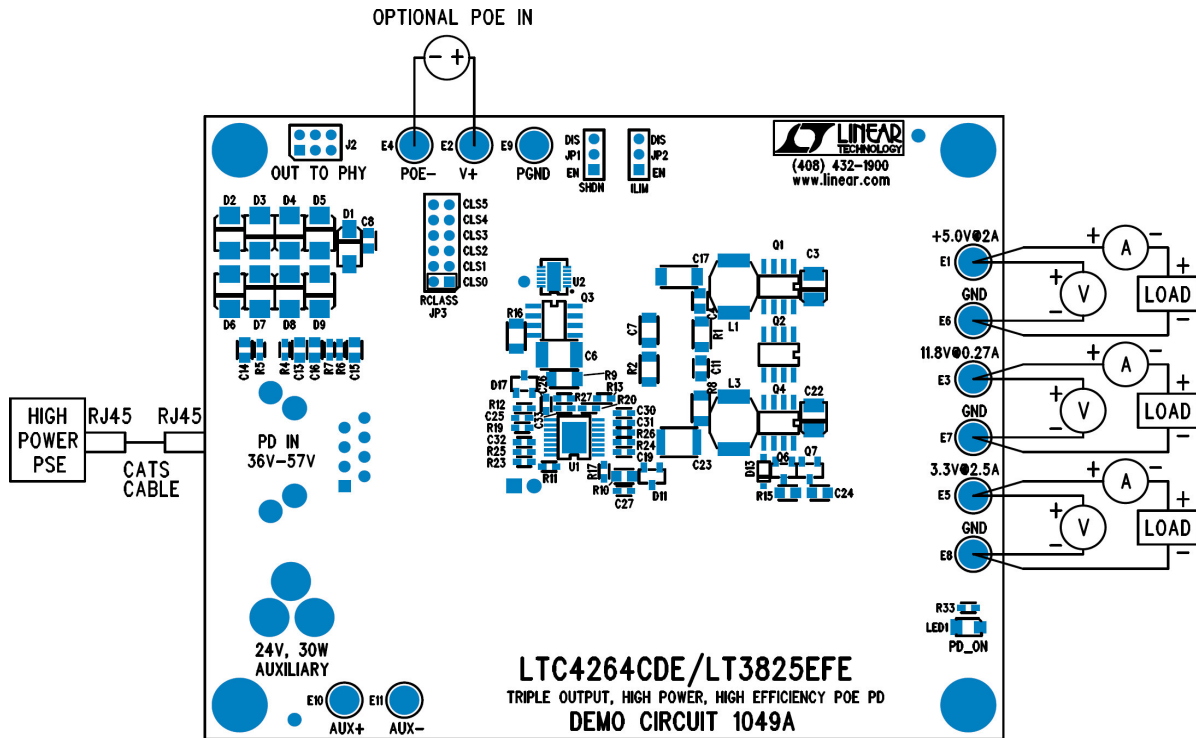


Figure 1. Proper high power PoE measurement equipment setup

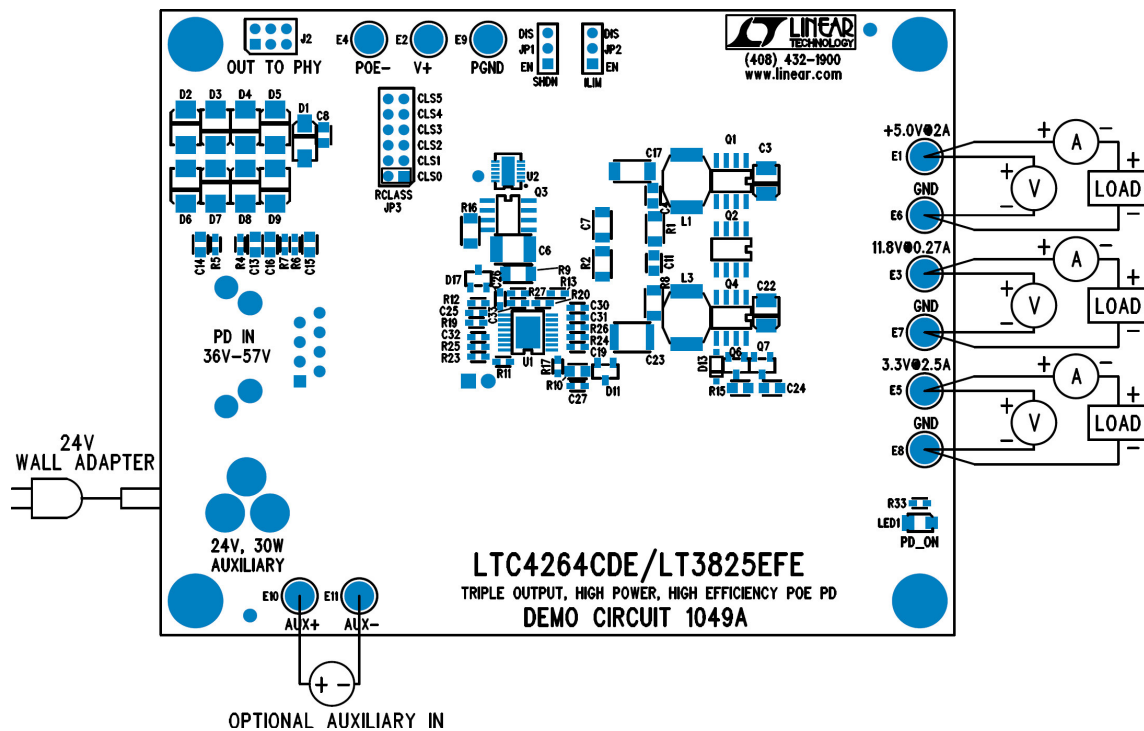


Figure 2. Proper auxiliary supply measurement equipment setup

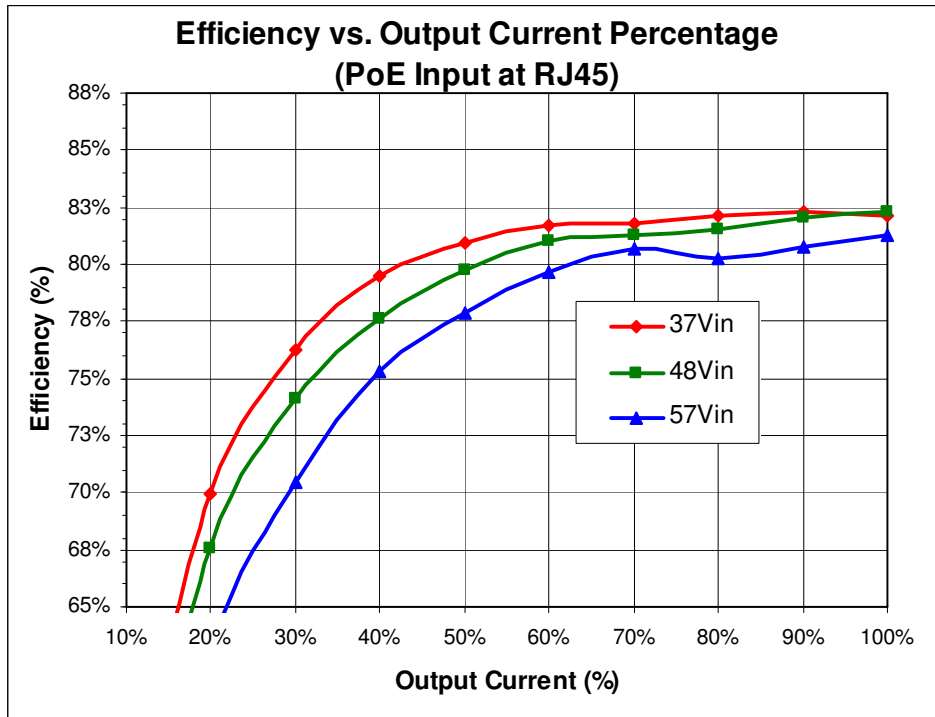


Figure 3. Efficiency curves for different input voltages for PoE in.

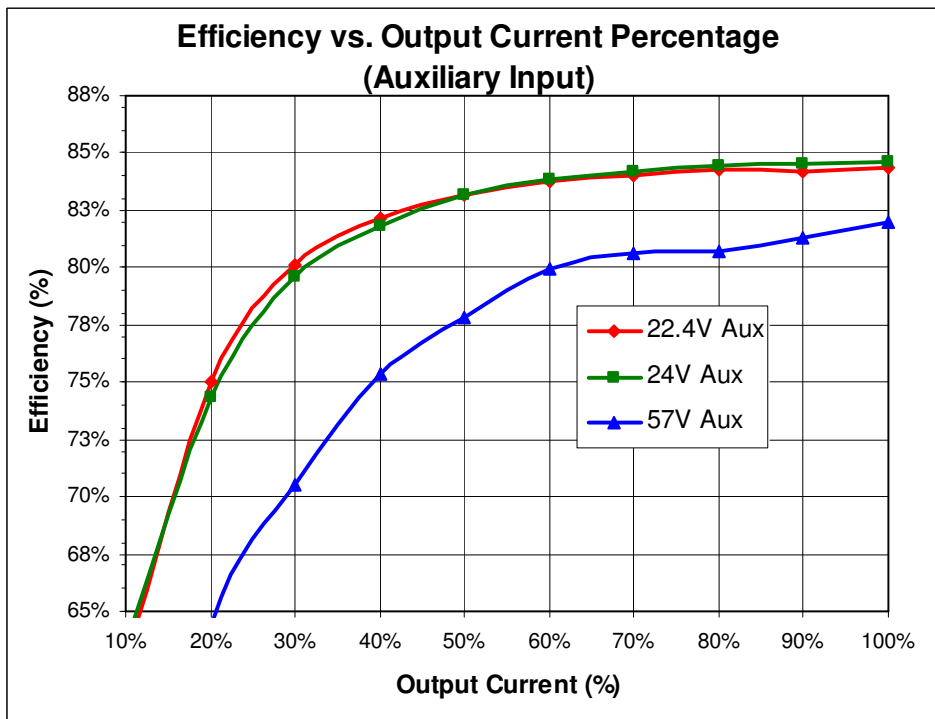


Figure 4. Efficiency curves for different input voltages for auxiliary in.

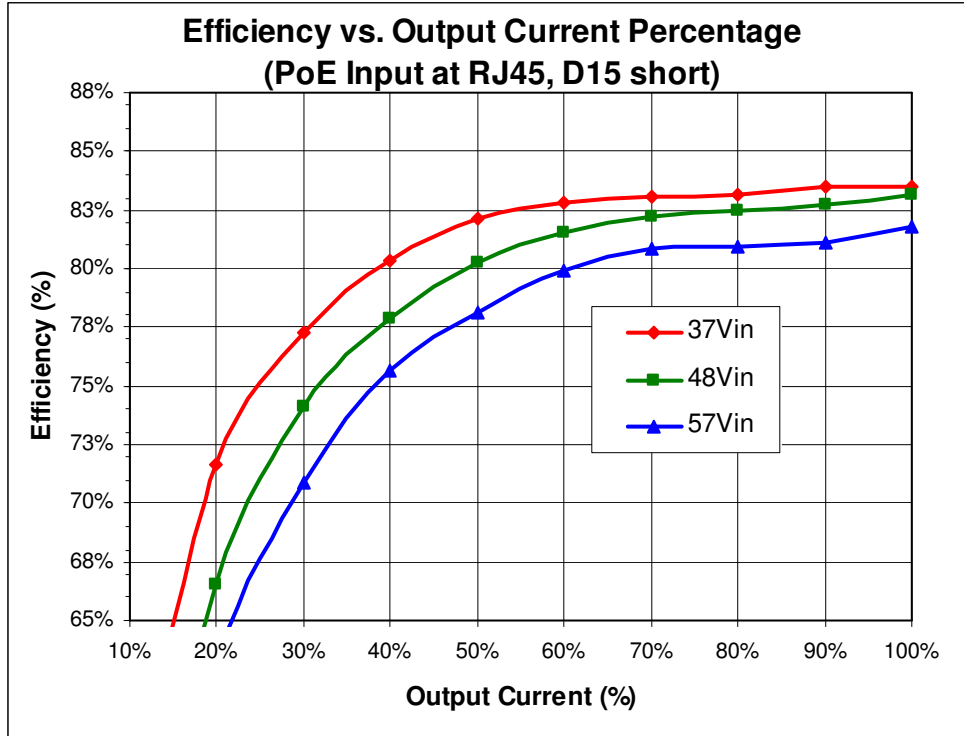


Figure 5. Efficiency curves for different input voltages for PoE in with D15 short.

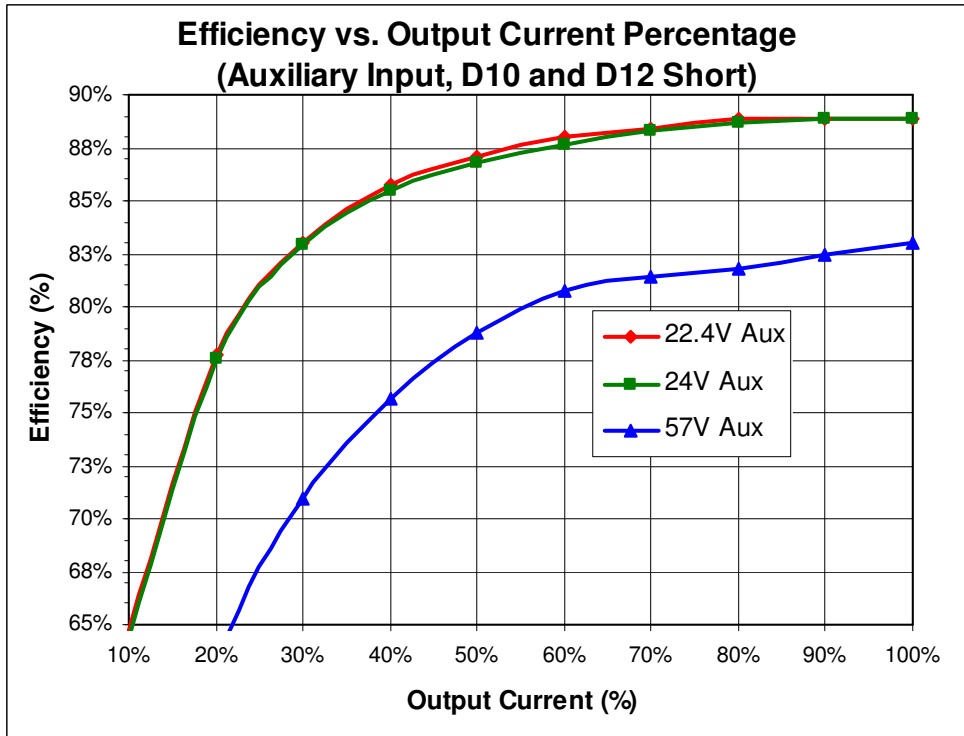
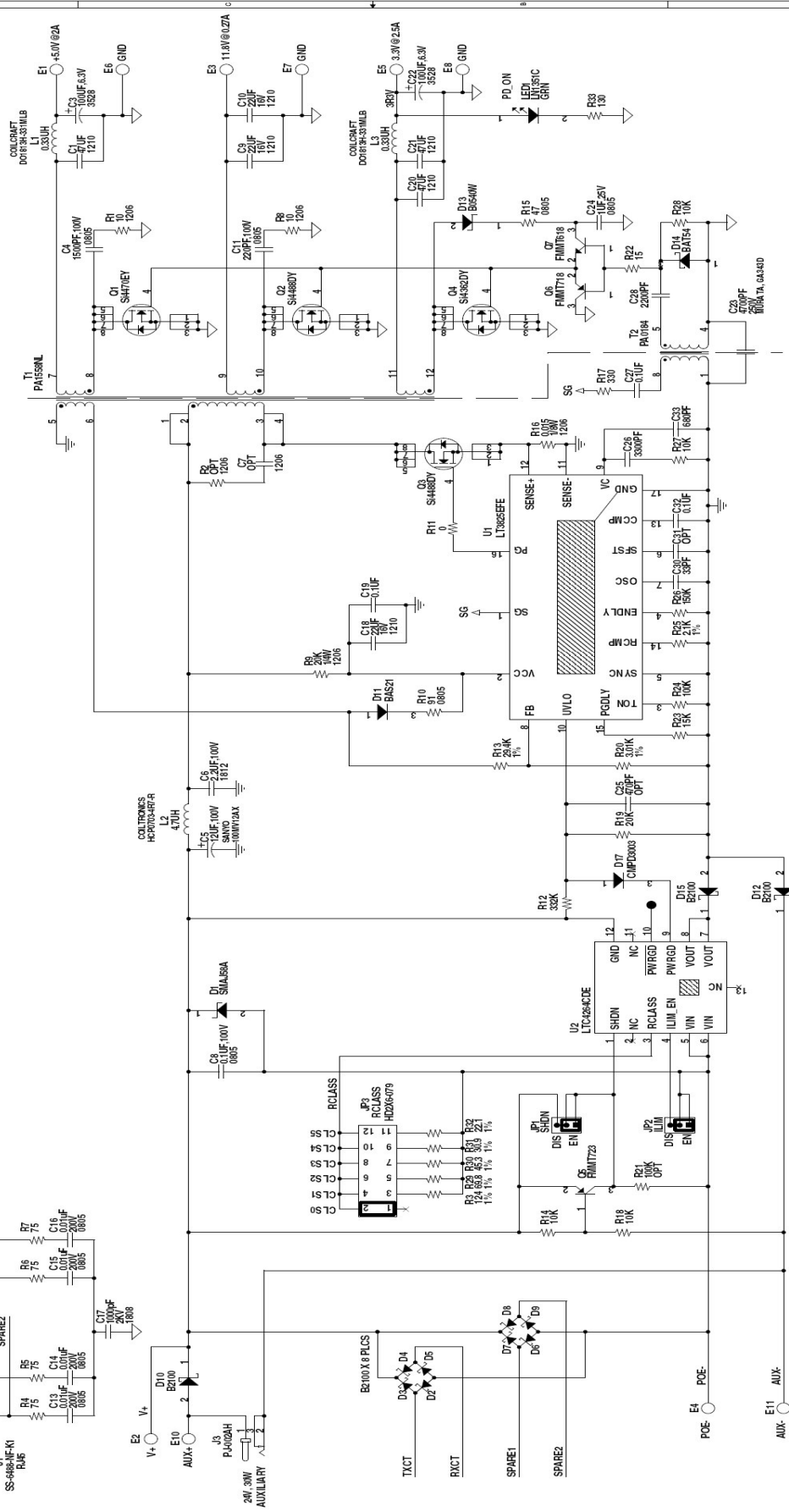
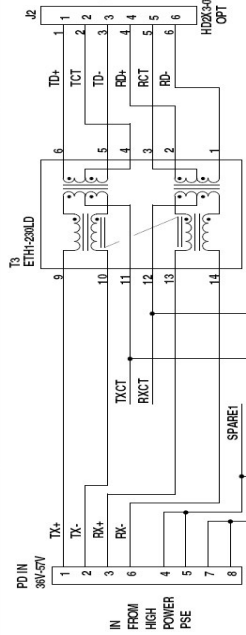


Figure 6. Efficiency curves for different input voltages for auxiliary in with D10 and D12 short.

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48VIN TO 5V@3A, 3.3V@5A, AND 11.8V@0.5A ISOLATED SUPPLY
HIGH POWER PD
(NON COMPLIANT TO IEEE802.3AF IF PD POWER EXCEEDS 12.95W)



CUSTOMER NOTICE		CONTRACT NO.	
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS. HOWEVE, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATION ENGINEERING FOR ASSISTANCE.		1630 McCarty Blvd. Milpitas, CA 95035 Phone: (408)432-1900 Fax: (408)432-5007 LTC Confidential - For Customer Use Only	
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		APPROVALS DRAWN: KWT CHECKED: APPROVED: ENGINEER: JLANE DESIGNER:	
		TITLE: SCHEMATIC	
		TRIPLE OUTPUT, HIGH POWER, HIGH EFFICIENCY POE PD	
		SIZE: DWG. NO.	
		PART NO. DC1049A-2 * LTC4264CDEL T3825EFC	
		DATE: Thursday, May 17, 2007	
		SHEET 1 OF 1	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 0603. ALL CAPACITORS ARE 0603.
2. INSTALL SHUNTS ON JP1, JP3, PIN 1 AND 2.
3. REMOVE R14, R18, AND Q5, AND SHORT D15 IN DESIGN IF AUXILIARY SUPPLY IS NOT USED.