



PC Card (PCMCIA) Interface Switch—12-V Suspend Capability

FEATURES

- Programmable V_{CC} Ramp
- Smart Switching
- 12-V Sleepmode Compatible
- Extremely Low R_{ON}
- Reverse Blocking Switches
- V_{PP} Programmable to 0, 12-V or V_{CC}
- Safe Power-Up
- Low Power Consumption
- PC Card 3-V/5-V Compatible
- Logic Compatible Inputs
- Single SO-16 Package

DESCRIPTION

The Si9712 combines low on-resistance with slow ramp time and smart switching for overall best performance in integrated PC Card interface switches.

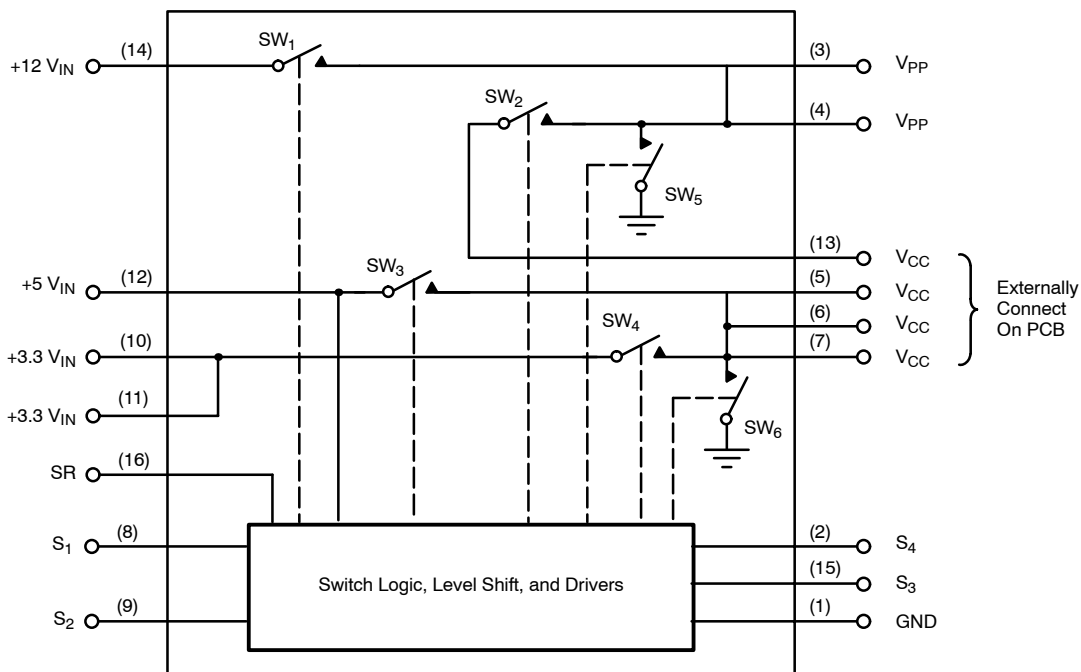
The Si9712 operates off the 5-V supply and has built-in level shifting for gate drive. Internal logic protects against an external control input error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9712 to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The Si9712 complies with the release of the PC Card standard by supplying 0 V, 12 V, and V_{CC} to the V_{PP} output and 0 V, 3.3 V, and 5 V to the V_{CC} output. The V_{CC} ramp time is user programmable with an external capacitor connected to the SR pin.

The PC Card switch is packaged in a narrow body SO-16 package and is rated over the industrial temperature range -40 to 85°C .

The Si9712 is available in both standard and lead (Pb)-free packages.

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

| | |
|---|--------|
| Voltages Referenced to Ground | |
| +12 V _{IN} | 15 V |
| +5 V _{IN} | 7 V |
| +3.3 V _{IN} ^c | 7 V |
| S ₁ through S ₄ (CMOS Inputs) | 7 V |
| I _{OUT} V _{PP} ^a | 300 mA |
| All Pins | -0.5 V |
| I _{OUT} V _{CC} ^b | 4 A |

| | |
|---------------------------------|---------|
| PD Max: (T _A = 25°C) | 2.5 W |
| (T _A = 85°C) | 1.0 W |
| Junction Temperature | 125°C |
| Thermal Rating—R _{ΘJA} | 40 °C/W |

Notes

- Pins 3, 4 connected together externally.
- Pins 5, 6, 7, 13 connected together externally.
- Pins 10, 11 connected together externally.

RECOMMENDED OPERATING CONDITIONS

| | |
|---|-----------------|
| +12 V _{IN} | 0 or 12 V ± 10% |
| +5 V _{IN} (must be present) | 5 V ± 10% |
| +3.3 V _{IN} ^c | 3.3 V ± 10% |
| C _{SR} | 33 nF |
| I _{OUT} V _{PP} ^a | 150 mA |
| I _{OUT} V _{CC} ^b | 2 A |

| | |
|----------------------------------|------------|
| V _{PP} Load Capacitance | 10 μF Max |
| V _{CC} Load Capacitance | 150 μF Max |

Notes

- Pins 3, 4 connected together externally.
- Pins 5, 6, 7, 13 connected together externally.
- Pins 10, 11 connected together externally.

| SPECIFICATIONS | | | | | | | |
|------------------------------------|-----------------------|---|-----------------------|-----------------------|------------------|------------------|------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified | | Limits -40 to 85°C | | | Unit |
| | | C _{SR} = 33 nF, +12 V _{IN} = 12 V, +5 V _{IN} = 5 V +3.3 V _{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V | | Min ^a | Typ ^b | Max ^a | |
| Switch 1 | | | | | | | |
| On-Resistance | R _{ON} | I = 120 mA, +12 V _{IN} = 11.4 V S ₃ = S ₁ = High S ₂ = S ₄ = Low | T _A = 25°C | | | 120 | mΩ |
| | | | T _A = 85°C | | | 145 | |
| Off Current (+12 V _{IN}) | I _{OFF} | +12 V _{IN} = 12.6 V S ₁ = Low | T _A = 25°C | | | 1 | μA |
| | | | T _A = 85°C | | | 10 | |
| Switching Time | t _{SW1(on)} | S ₂ = S ₄ = Low, See Figure 1 S ₃ = High | | 50 | 200 | 350 | μs |
| | t _{SW1(off)} | | | | 1.0 | 10 | |
| Delay Time | t _{d(on)} | See Figure 3 S ₂ = S ₄ = Low | | 1.0 | 6 | 20 | ms |
| | t _{d(off)} | | | 0.1 | 2.9 | 10 | |
| Rise Time | t _{SW1(on)} | S ₂ = S ₄ = Low, S ₃ = High, See Figure 2 | | 50 | 150 | 300 | μs |
| Switch 2 | | | | | | | |
| On-Resistance | R _{ON} | I = 120 mA, S ₂ = S ₃ = High S ₁ = S ₄ = Low | T _A = 25°C | | | 150 | mΩ |
| | | | T _A = 85°C | | | 180 | |
| Switching Time | t _{SW2(on)} | S ₁ = S ₄ = Low, S ₃ = High, See Figure 1 | | 50 | 200 | 350 | μs |
| | t _{SW2(off)} | | | | 1.0 | 10 | |
| Delay Time | t _{d(on)} | S ₁ = S ₄ = Low, See Figure 3 | | 1.0 | 6 | 20 | ms |
| | t _{d(off)} | | | 0.1 | 1.7 | 10 | |
| Rise Time | t _{SW2(on)} | S ₁ = S ₄ = Low, S ₃ = High, See Figure 2 | | 50 | 150 | 300 | μs |
| Switch 3 | | | | | | | |
| On-Resistance | R _{ON} | I = 500 mA, S ₃ = High S ₁ = S ₂ = S ₄ = Low | T _A = 25°C | | | 70 | mΩ |
| | | | T _A = 85°C | | | 95 | |
| Off Current (V _{CC}) | I _{OFF} | +5 V _{IN} = 5.5 V, V _{CC} = 0 V S ₁ = S ₂ = S ₃ = Low S ₄ = High +3.3 V _{IN} = Open Circuit | T _A = 25°C | | | 1 | μA |
| | | | T _A = 85°C | | | 10 | |
| Rise Time | t _{SW3(on)} | S ₁ = S ₂ = S ₄ = Low, See Figure 2 | | 0.1 | 1.7 | 10 | ms |
| Fall Time | t _{SW3(off)} | | | 3 | 30 | 50 | |



| SPECIFICATIONS | | | | | | | |
|--|----------------|---|-------------------------------------|-----------------------|------------------|------------------|------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $C_{SR} = 33 \text{ nF}$, $+12 \text{ V}_{IN} = 12 \text{ V}$, $+5 \text{ V}_{IN} = 5 \text{ V}$ $+3.3 \text{ V}_{IN} = 3.3 \text{ V}$, Low $\leq 0.8 \text{ V}$, High $\geq 2.2 \text{ V}$ | | Limits -40 to 85°C | | | Unit |
| | | | | Min ^a | Typ ^b | Max ^a | |
| Switch 4 | | | | | | | |
| On-Resistance | R_{ON} | $I = 500 \text{ mA}$, $S_4 = \text{High}$ $S_1 = S_2 = S_3 = \text{Low}$ | $T_A = 25^\circ\text{C}$ | | | 50 | mΩ |
| | | | $T_A = 85^\circ\text{C}$ | | | 70 | |
| Off Current (+3.3 V _{IN}) | I_{OFF} | $+3.3 \text{ V}_{IN} = 3.6 \text{ V}$, $S_1 = S_2 = S_3 = S_4 = \text{Low}$ | $T_A = 25^\circ\text{C}$ | | | 1 | μA |
| | | | $T_A = 85^\circ\text{C}$ | | | 10 | |
| Rise Time | $t_{SW4(on)}$ | $S_1 = S_2 = S_3 = \text{Low}$, See Figure 2 | | 0.1 | 0.9 | 10 | ms |
| Fall Time | $t_{SW4(off)}$ | | | 3 | 20 | 40 | |
| Switch 5 | | | | | | | |
| On-Resistance | R_{ON} | $I = 2 \text{ mA}$, $S_1 = S_2 = \text{Low}$ | $T_A = 25^\circ\text{C}$ | | 235 | 400 | Ω |
| | | | $T_A = 85^\circ\text{C}$ | | 325 | 550 | |
| Switch 6 | | | | | | | |
| On-Resistance | R_{ON} | $I = 2 \text{ mA}$, $S_3 = S_4 = \text{Low}$ | $T_A = 25^\circ\text{C}$ | | 140 | 400 | Ω |
| | | | $T_A = 85^\circ\text{C}$ | | 200 | 500 | |
| Power Supply | | | | | | | |
| +5 V _{IN} Current Input (on) | $I_{+5VIN(1)}$ | $S_1 = S_4 = 0 \text{ V}$, $S_2 = S_3 = 3 \text{ V}$ | | | 20 | 50 | μA |
| | $I_{+5VIN(2)}$ | $S_1 = S_4 = 3 \text{ V}$, $S_2 = S_3 = 0 \text{ V}$ | | | 20 | 50 | |
| +5 V _{IN} Current Input (off) | $I_{+5VIN(3)}$ | $S_1 = S_2 = S_3 = S_4 = 0 \text{ V}$ | | | <1 | 10 | |
| Switch Control Inputs | | | | | | | |
| Input Voltage High | $V_{I(H)}$ | | $+5 \text{ V}_{IN} = 5.5 \text{ V}$ | 2.2 | 1.8 | | V |
| | | | $+5 \text{ V}_{IN} = 4.5 \text{ V}$ | 2.2 | 1.6 | | |
| Input Voltage Low | $V_{I(L)}$ | | $+5 \text{ V}_{IN} = 5.5 \text{ V}$ | | 1.6 | 0.8 | |
| | | | $+5 \text{ V}_{IN} = 4.5 \text{ V}$ | | 1.4 | 0.8 | |
| Input Current High | $I_{I(H)}$ | S_1 through $S_4 = 5 \text{ V}$ | | | | 1.0 | μA |
| Input Current Low | $I_{I(L)}$ | S_1 through $S_4 = \text{GND}$ | | -1.0 | | | |

Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TIMING WAVEFORMS

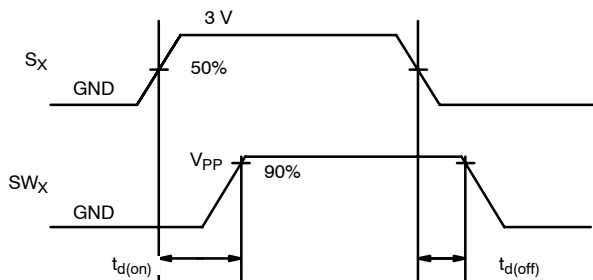


FIGURE 1. V_{PP} Switch Delay

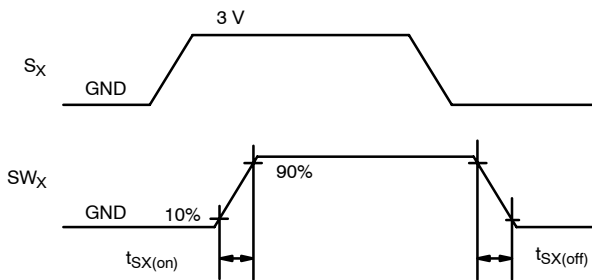


FIGURE 2. Switch Ramp

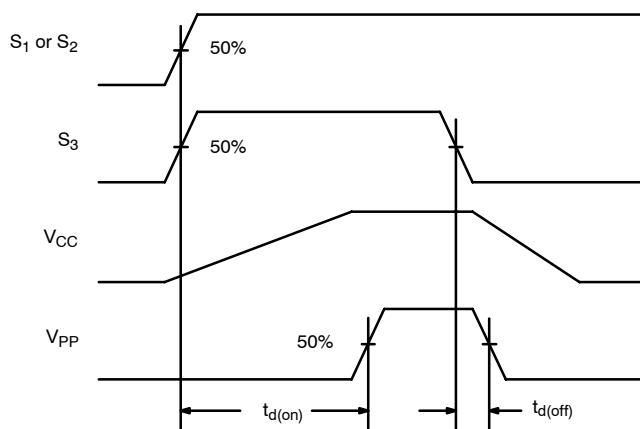
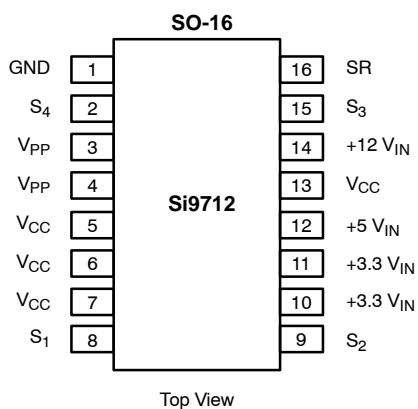


FIGURE 3. Delay from S_1 or S_2 to V_{PP} Power-up

PIN CONFIGURATION AND DESCRIPTION



Note: Pins 5, 6, 7, and 13 must be connected in the PCB for correct operation.

| Pin Number | Function | Description |
|-------------|---------------|---|
| 1. | GND | Ground connection. |
| 2 | S_4 | Control input for selecting +3.3 V_{IN} to V_{CC} . The PC Card terminology for this pin is V_{CC_EN0} . |
| 3, 4 | V_{PP} | Program and peripheral voltage to PC Card slot. |
| 5, 6, 7, 13 | V_{CC} | Supply voltage to slot. |
| 8 | S_1 | Control input for selecting +12 V_{IN} to V_{PP} . The PC Card terminology for this pin is V_{PP_EN1} . |
| 9 | S_2 | Control input for selecting V_{CC} to V_{PP} . The PC Card terminology for this pin is V_{PP_EN0} . |
| 10, 11 | +3.3 V_{IN} | +3.3-V supply. |
| 12 | +5 V_{IN} | +5-V supply. |
| 14 | +12 V_{IN} | +12-V supply. |
| 15 | S_3 | Control input for selecting +5 V_{IN} to V_{CC} . The PC Card terminology for this pin is V_{CC_EN1} . |
| 16 | SR | Slew rate control pin, capacitor to GND defines programmable ramp time. |

| ORDERING INFORMATION | | |
|----------------------|-------------------|---------|
| Part Number | Temperature Range | Package |
| Si9712DY | -40 to 85°C | SOIC-16 |
| Si9712DY-T1 | | |
| Si9712DY-T1—E3 | | |

| TRUTH TABLE ^b | | | | | | | | | |
|--------------------------|----------------|----------------|----------------|-----------------------|-----------------------|----------|----------|----------|----------|
| S ₁ | S ₂ | S ₃ | S ₄ | Switch 1 ^a | Switch 2 ^a | Switch 3 | Switch 4 | Switch 5 | Switch 6 |
| 0 | 0 | 0 | 0 | Off | Off | Off | Off | On | On |
| 0 | 0 | 0 | 1 | Off | Off | Off | On | On | Off |
| 0 | 0 | 1 | 0 | Off | Off | On | Off | On | Off |
| 0 | 0 | 1 | 1 | Off | Off | Off | Off | On | On |
| 0 | 1 | 0 | 0 | Off | Off | Off | Off | On | On |
| 0 | 1 | 0 | 1 | Off | On | Off | On | Off | Off |
| 0 | 1 | 1 | 0 | Off | On | On | Off | Off | Off |
| 0 | 1 | 1 | 1 | Off | Off | Off | Off | On | On |
| 1 | 0 | 0 | 0 | Off | Off | Off | Off | On | On |
| 1 | 0 | 0 | 1 | On | Off | Off | On | Off | Off |
| 1 | 0 | 1 | 0 | On | Off | On | Off | Off | Off |
| 1 | 0 | 1 | 1 | Off | Off | Off | Off | On | On |
| 1 | 1 | 0 | 0 | Off | Off | Off | Off | On | On |
| 1 | 1 | 0 | 1 | On | Off | Off | On | Off | Off |
| 1 | 1 | 1 | 0 | On | Off | On | Off | Off | Off |
| 1 | 1 | 1 | 1 | Off | Off | Off | Off | On | On |

Notes

- a. Turn on of switch 1 and 2 are internally delayed until after V_{CC} is valid. See Figure 3.
- b. Shaded lines are error conditions for PC Card applications, however, switches default to the states shown.

TIMING DIAGRAM

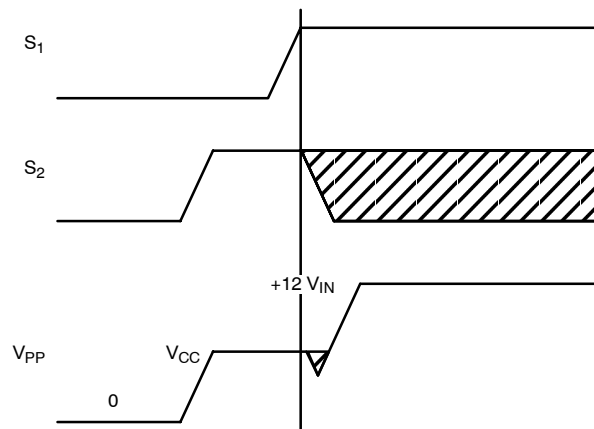
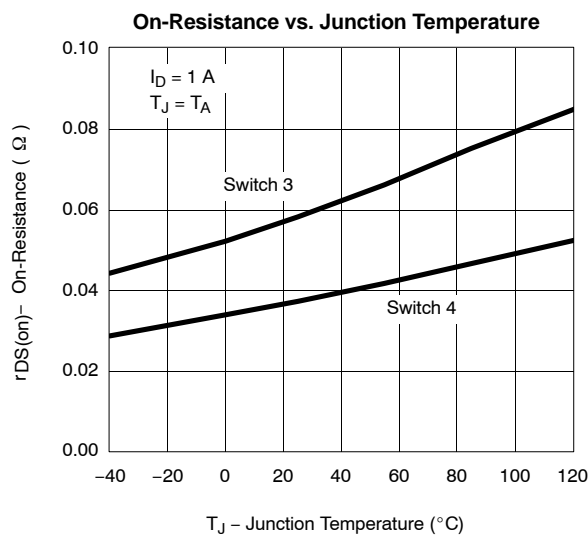
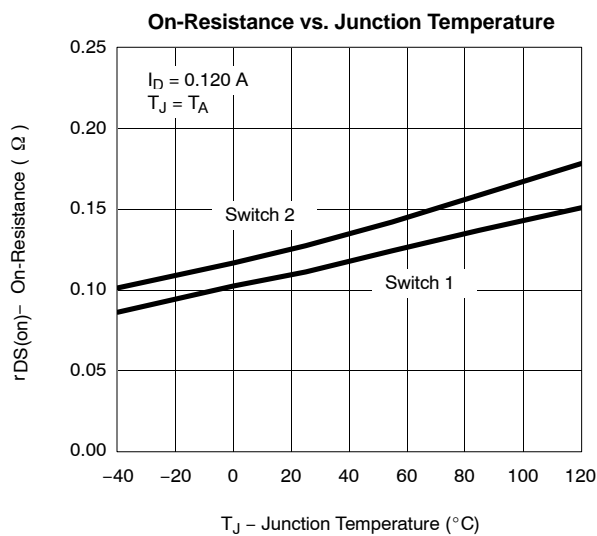
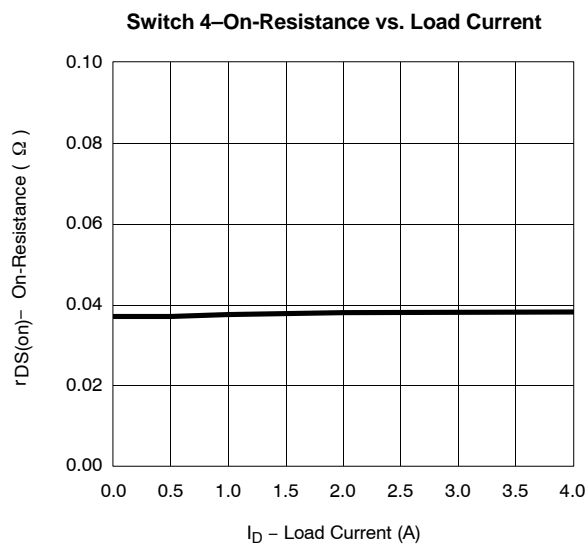
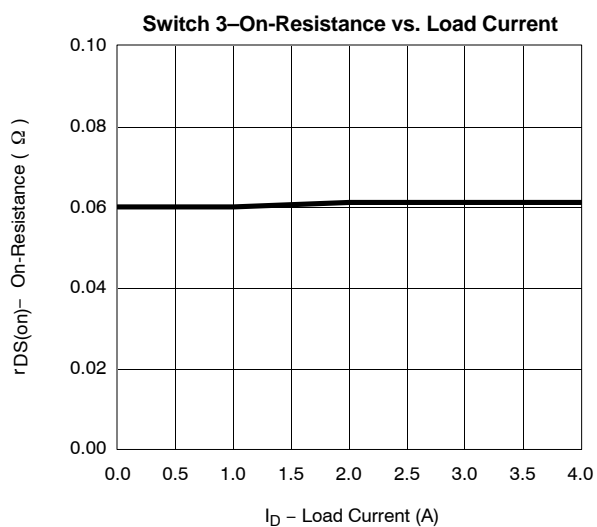
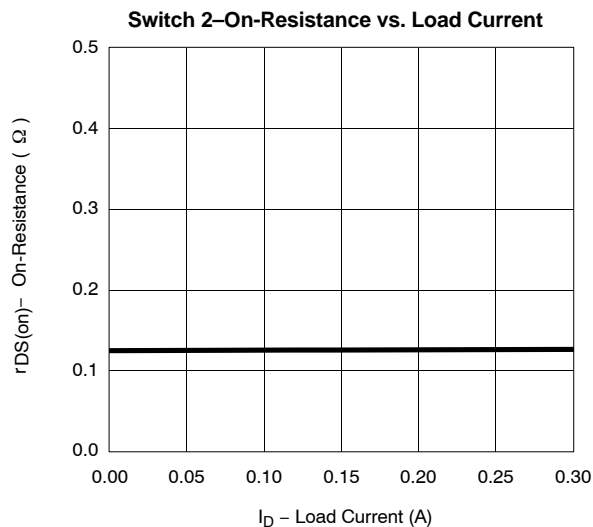
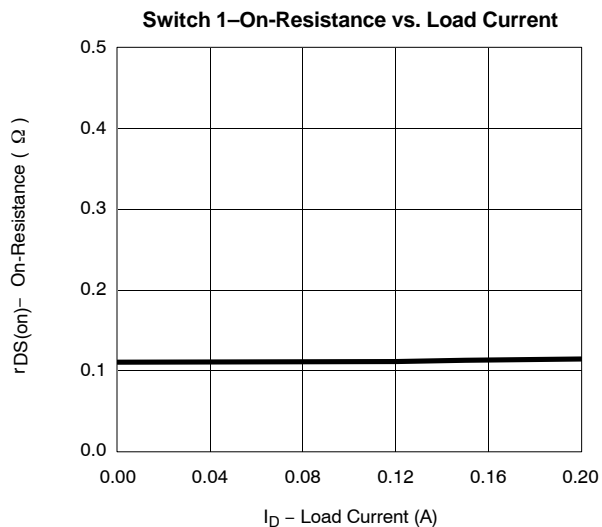


FIGURE 4. Break-Before-Make of SW₁ and SW₂



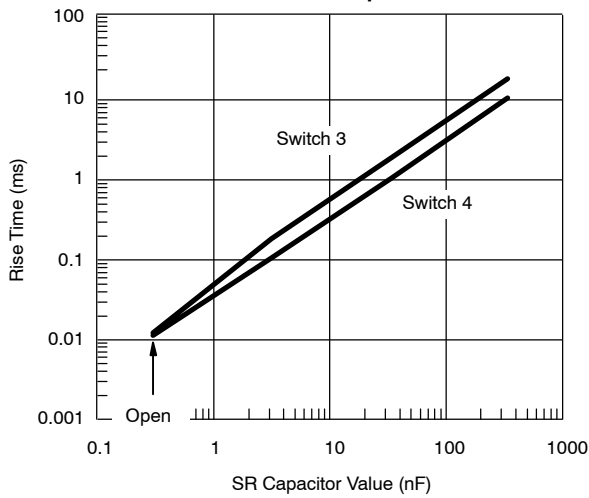
TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)



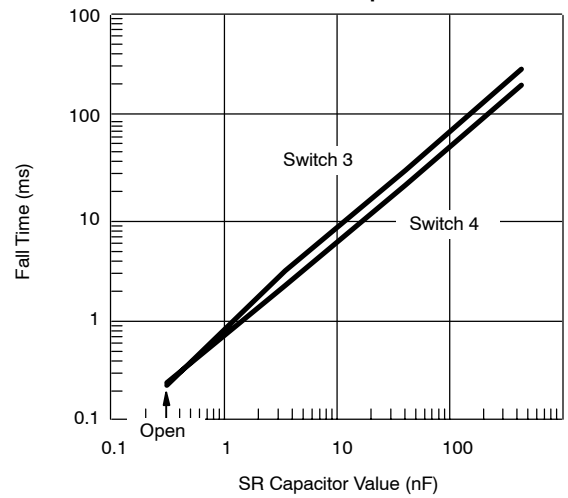


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

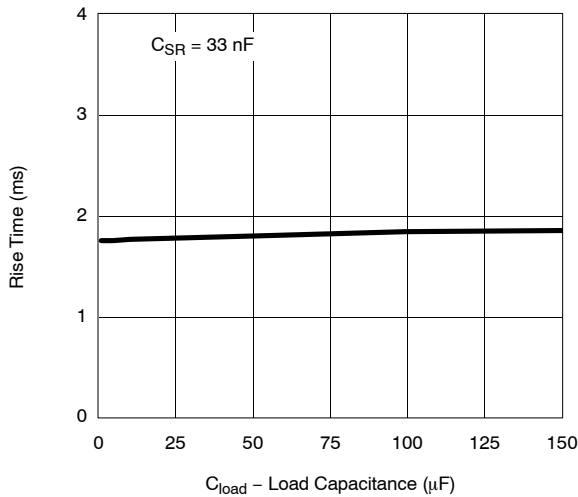
Rise Time vs. SR Capacitor Value



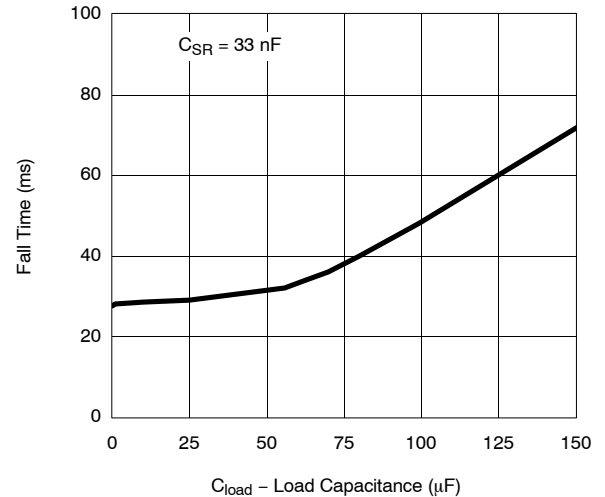
Fall Time vs. SR Capacitor Value



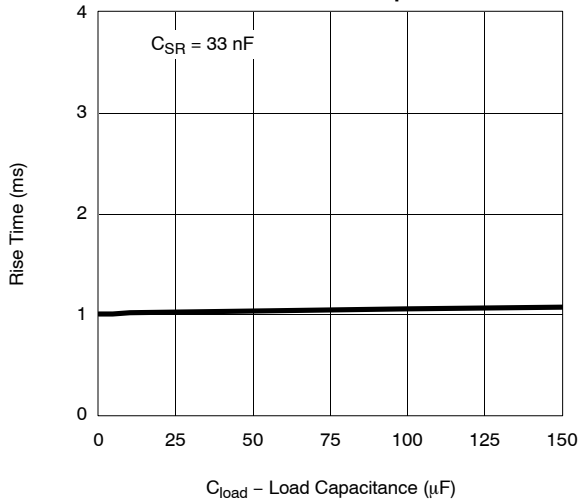
**Switch 3
Rise Time vs. Load Capacitance**



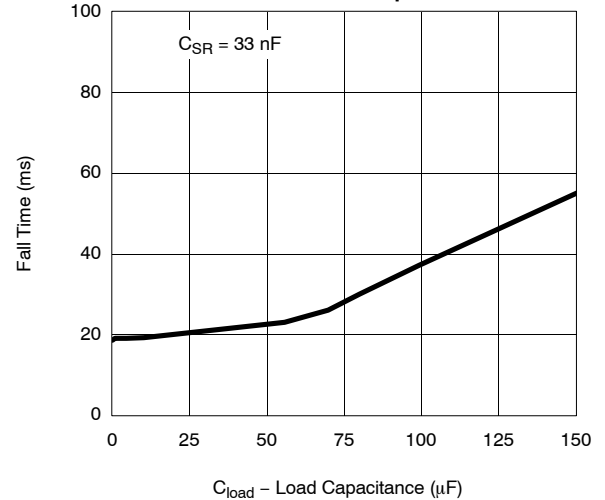
**Switch 3
Fall Time vs. Load Capacitance**



**Switch 4
Rise Time vs. Load Capacitance**



**Switch 4
Fall Time vs. Load Capacitance**





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