

N-channel 600 V, 0.135  $\Omega$  typ., 20 A MDmesh™ II  
Power MOSFETs in D<sup>2</sup>PAK and TO-220 packages

Datasheet - production data

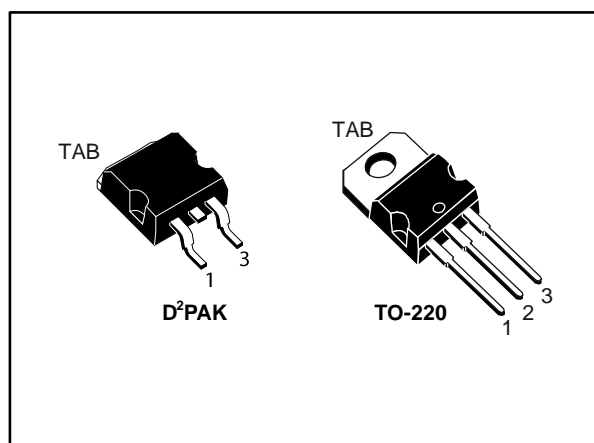
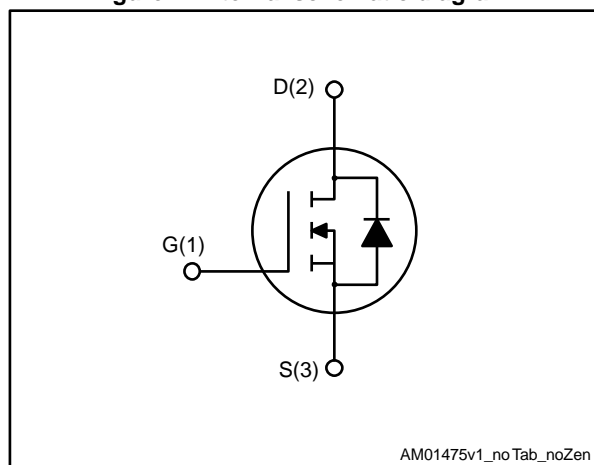


Figure 1: Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STB26NM60N	600 V	0.165 $\Omega$	20 A
STP26NM60N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STB26NM60N	26NM60N	D <sup>2</sup> PAK	Tape and reel
STP26NM60N		TO-220	Tube

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	80	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	140	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

**Notes:**

(1) Pulse width limited by safe operating area.

(2)  $I_{SD} \leq 20\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(\text{peak})} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3: Thermal data**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK	TO-220	
$R_{thj\text{-case}}$	Thermal resistance junction-case	0.89		$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient		62.5	$^\circ\text{C}/\text{W}$
$R_{thj\text{-pcb}}^{(1)}$	Thermal resistance junction-pcb	30		$^\circ\text{C}/\text{W}$

**Notes:**

(1) When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$ .

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Single pulse avalanche current (pulse width limited by $T_{j\text{max}}$ )	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	610	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	600			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C <sup>(1)</sup>			100	
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±0.1	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.135	0.165	Ω

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	1800	-	pF
C <sub>oss</sub>	Output capacitance		-	115	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	6	-	pF
C <sub>oss eq.</sub> <sup>(1)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V	-	310	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	60	-	nC
Q <sub>gs</sub>	Gate-source charge		-	8.5	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	30	-	nC
R <sub>G</sub>	Gate input resistance	f=1 MHz, I <sub>D</sub> =0 A	-	2.8	-	Ω

**Notes:**

<sup>(1)</sup>C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 10\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	13	-	ns
$t_r$	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
$t_f$	Fall time		-	50	-	ns

Table 8: Source-drain diode

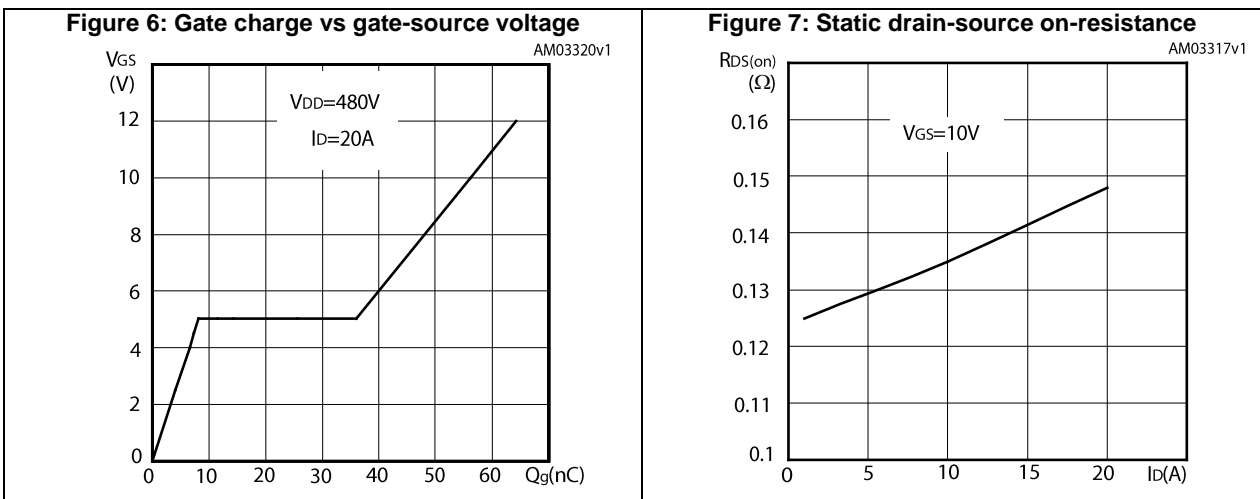
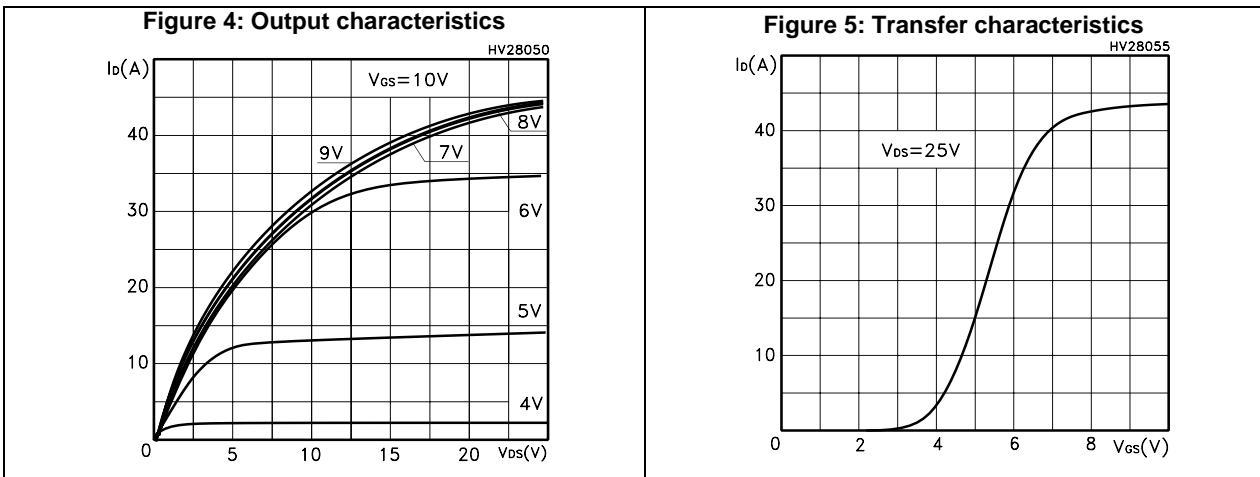
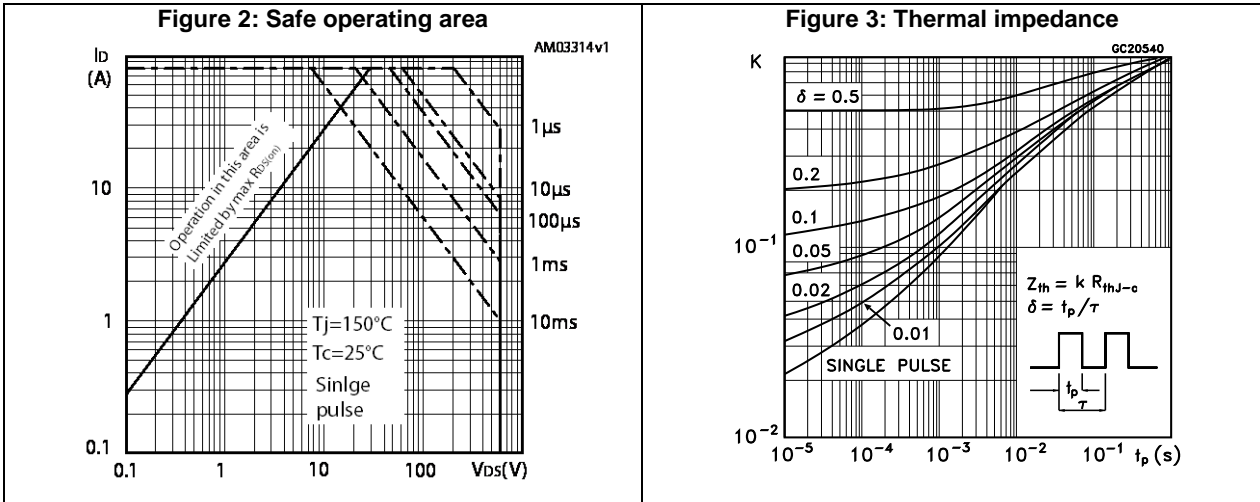
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	370		ns
$Q_{rr}$	Reverse recovery charge		-	5.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	31.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	450		ns
$Q_{rr}$	Reverse recovery charge		-	7.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	32.5		A

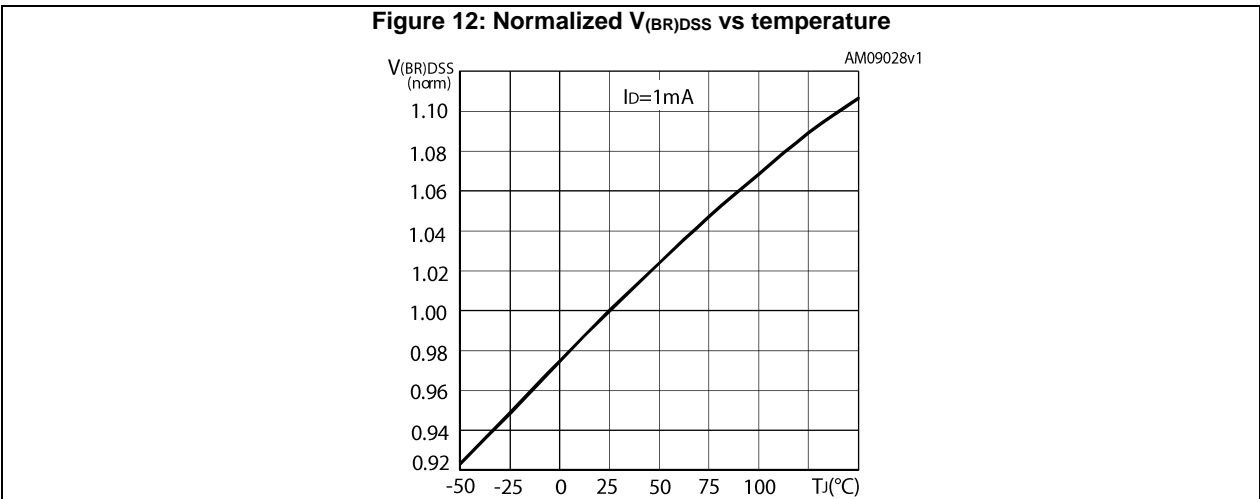
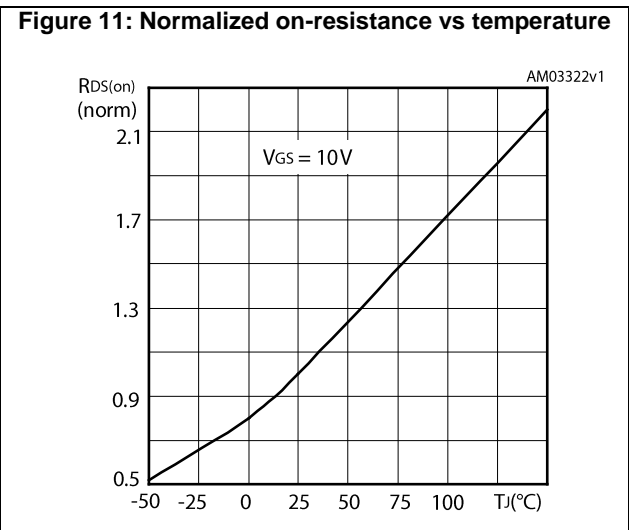
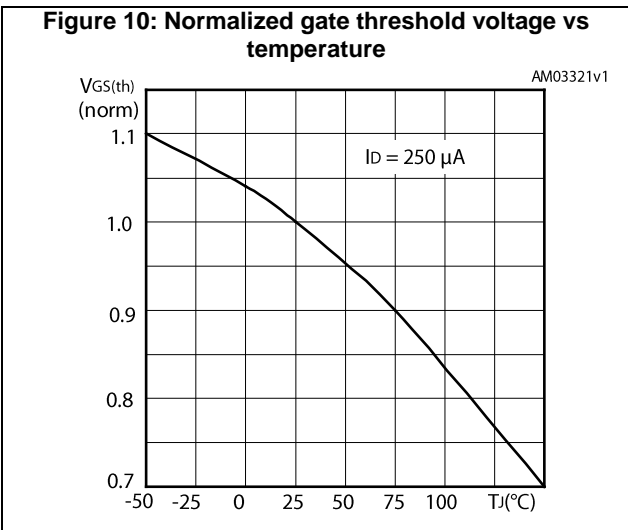
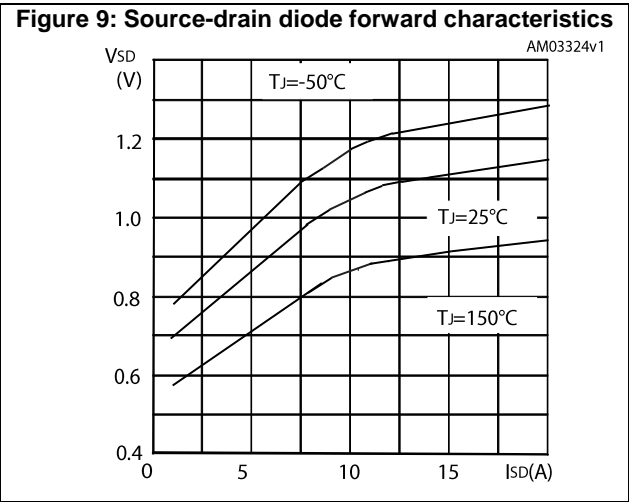
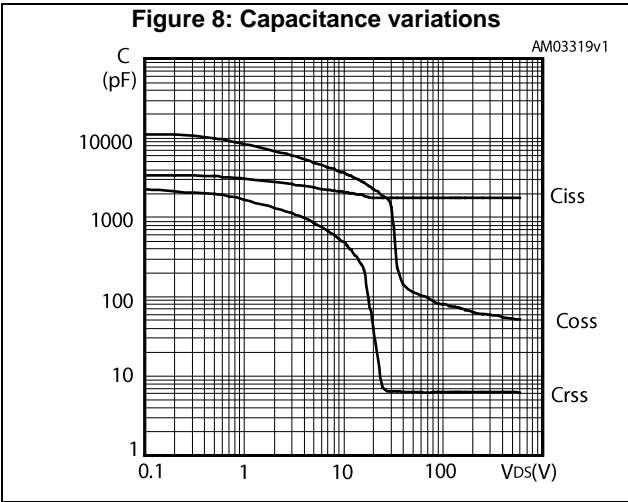
**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

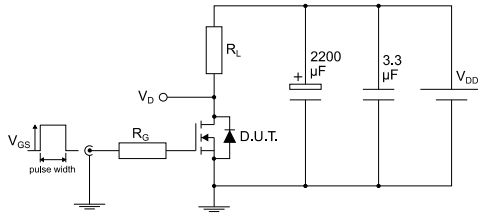
## 2.1 Electrical characteristics (curves)





### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



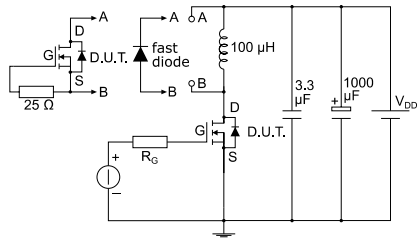
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**Figure 14: Test circuit for gate charge behavior**



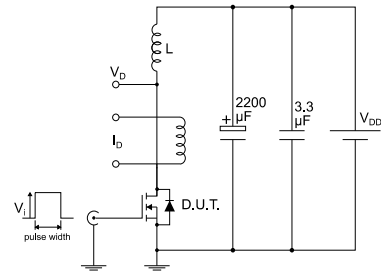
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



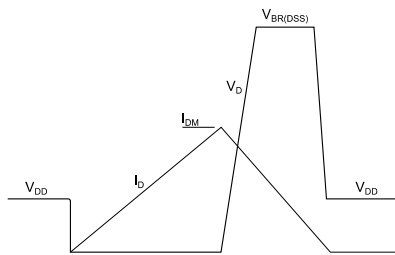
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**Figure 16: Unclamped inductive load test circuit**



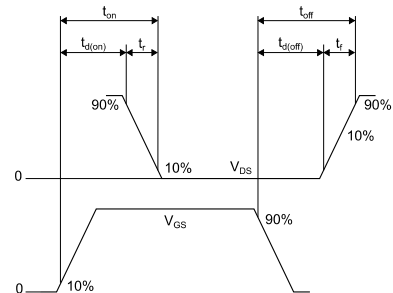
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D2PAK (TO-263) type A package information

Figure 19: D<sup>2</sup>PAK (TO-263) type A package outline

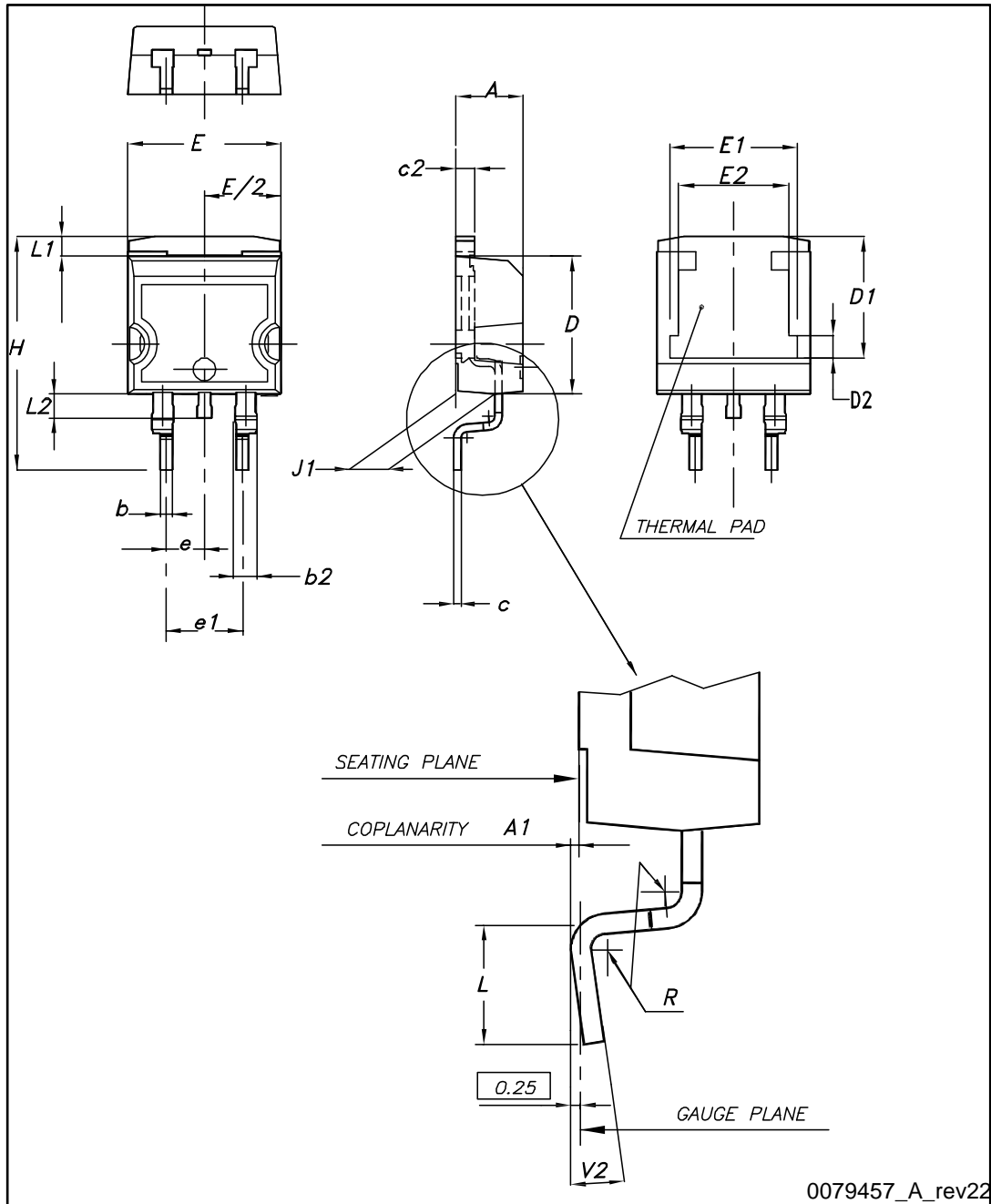
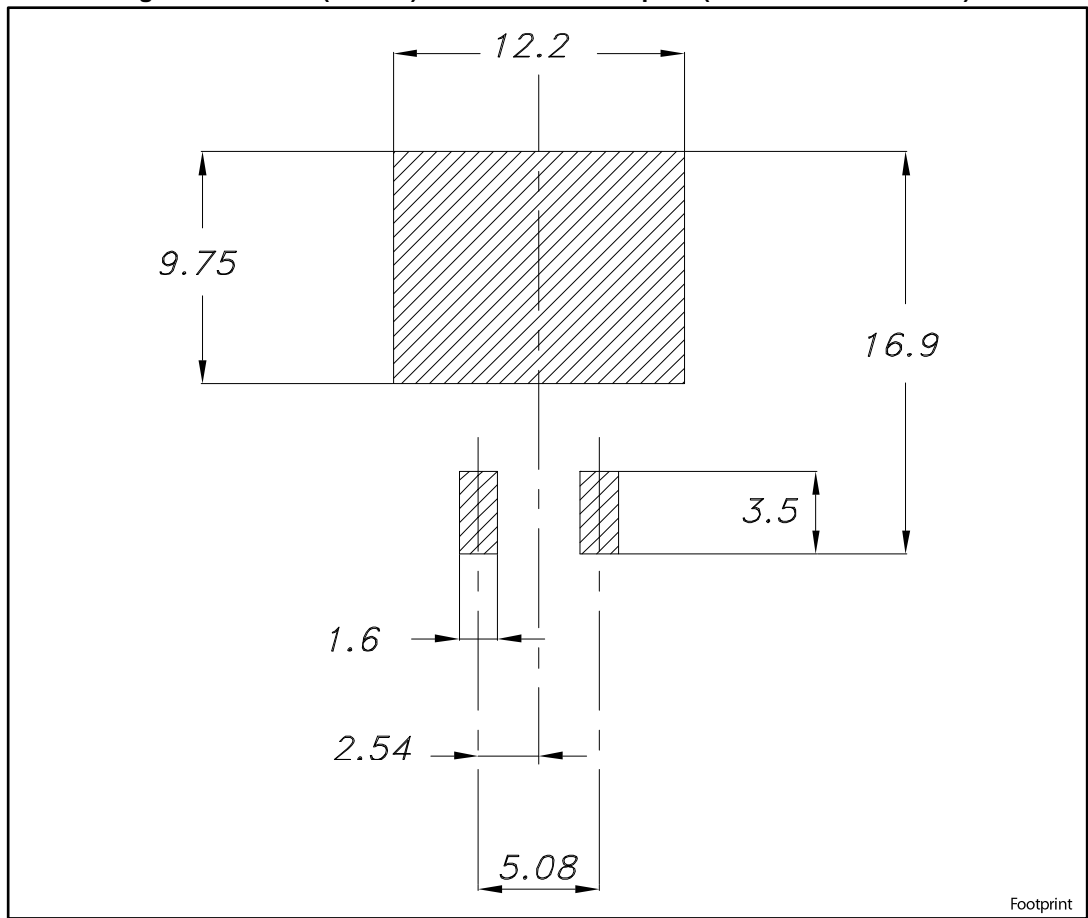


Table 9: D<sup>2</sup>PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20: D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



### 4.2 D2PAK packaging information

Figure 21: Tape outline

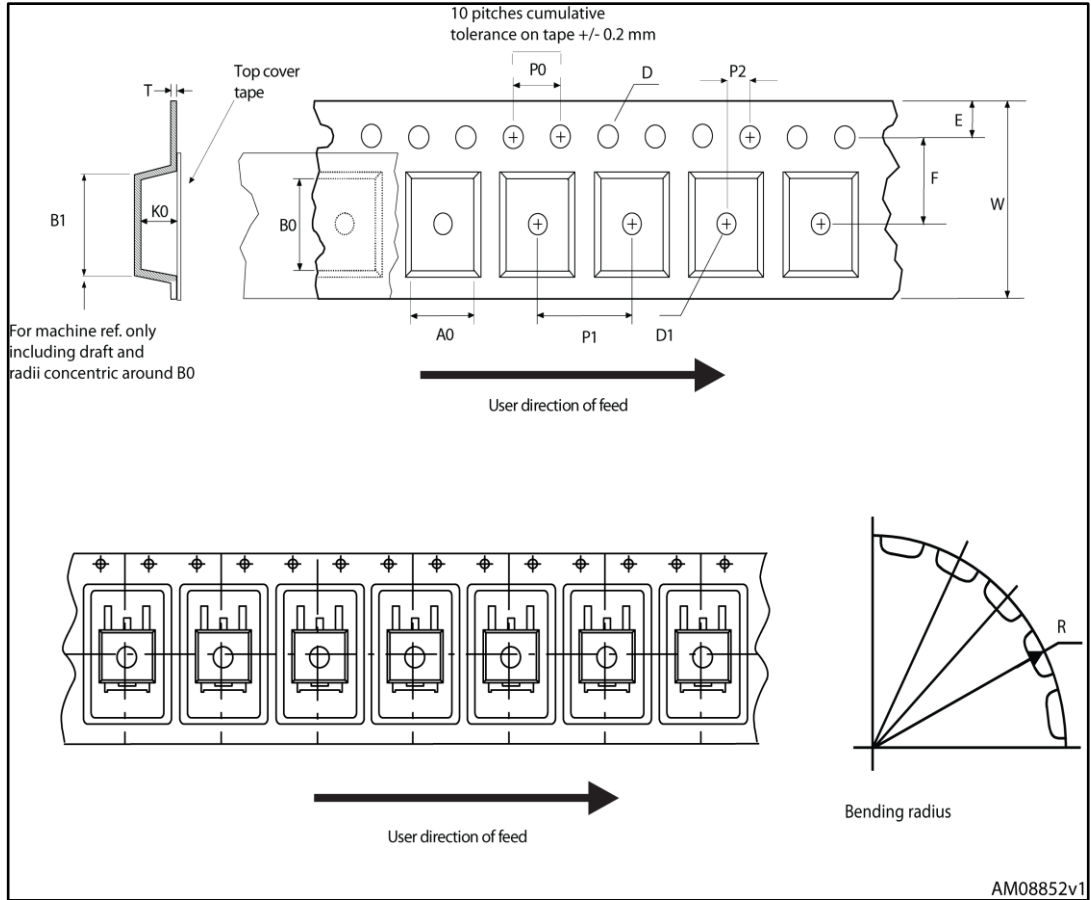


Figure 22: Reel outline

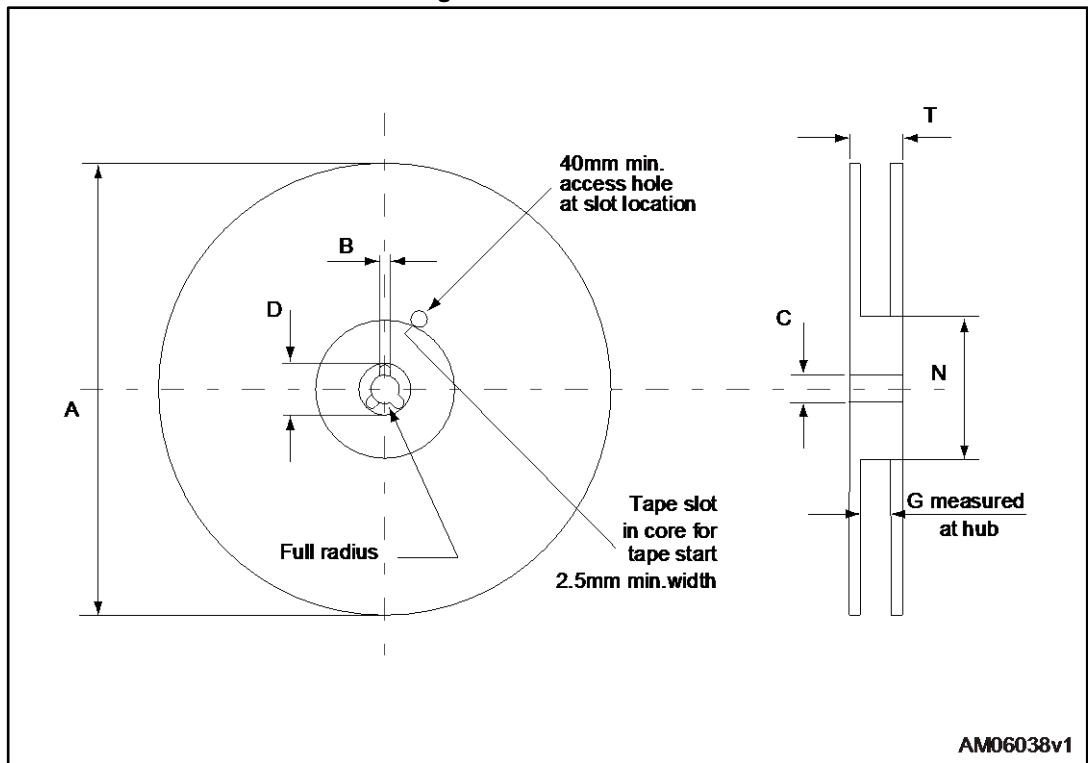


Table 10: D<sup>2</sup>PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

### 4.3 TO-220 type A package information

Figure 23: TO-220 type A package outline

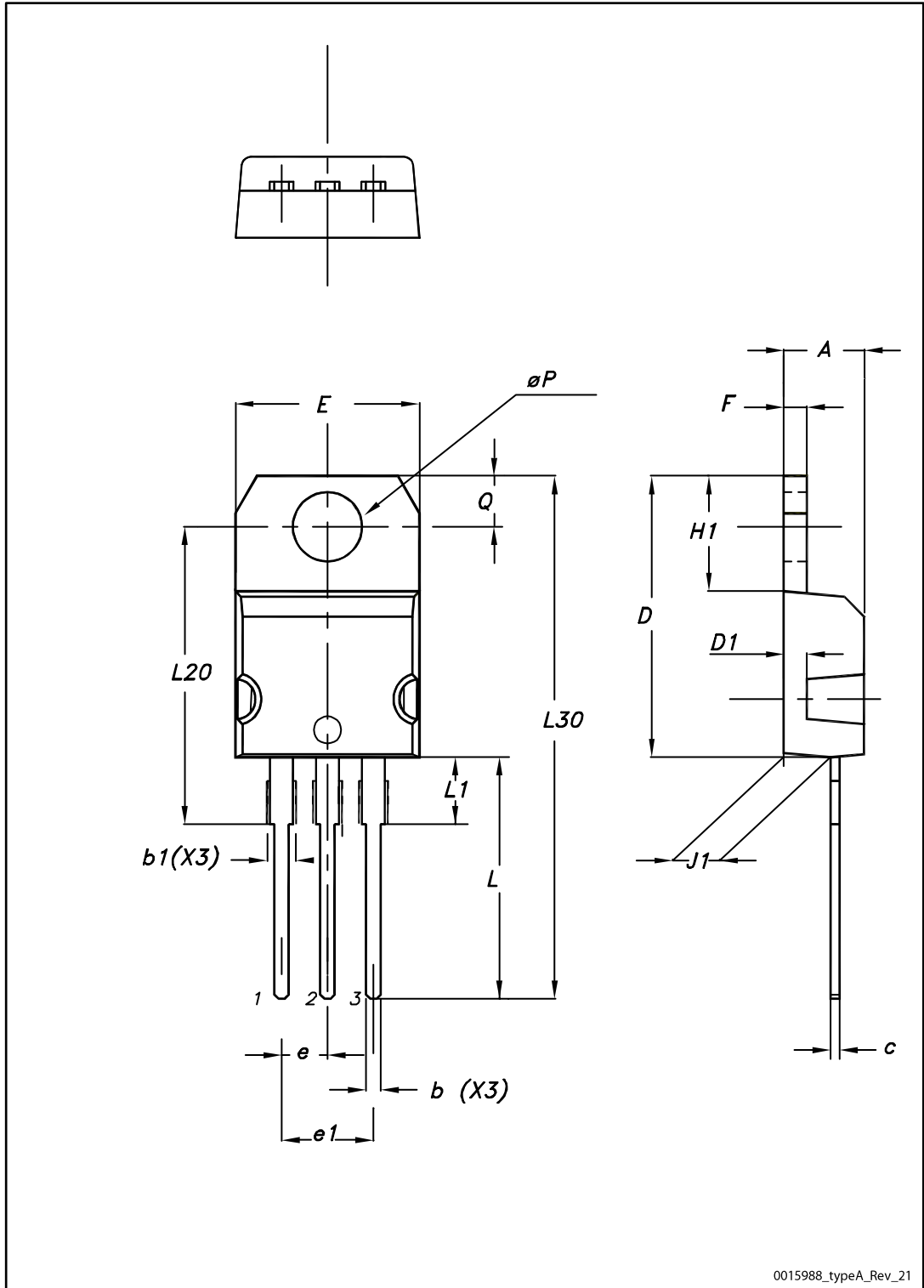


Table 11: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

## 5 Revision history

Table 12: Document revision history

Date	Revision	Changes
29-Apr-2009	1	First release.
17-Dec-2009	2	Added new package, mechanical data: D <sup>2</sup> PAK
20-Jun-2011	3	Inserted device in I <sup>2</sup> PAK.
13-Mar-2012	4	Updated P <sub>TOT</sub> and derating factor in <i>Table 2</i> . Update R <sub>thj-case</sub> for TO-220FP in <i>Table 3</i> . Update <i>Figure 10</i> and <i>Figure 15</i> . Update <i>Section 5: Packaging mechanical data</i> .
20-Jun-2012	5	Updated title on the cover page. Minor text changes.
09-Sep-2013	6	– The part numbers STI26NM60N and STW26NM60N have been moved to the separate datasheets – Modified: V <sub>GS</sub> value in <i>Table 2</i> .
12-Dec-2016	7	The part number STF26NM60N has been moved to a separate datasheet. Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> , <i>Table 5: "On/off states"</i> , <i>Table 6: "Dynamic"</i> and <i>Table 7: "Switching times"</i> . Modified <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text changes.



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