

v01.1010

14 Gbps, FAST RISE TIME XOR / XNOR GATE w/ PROGRAMMABLE OUTPUT VOLTAGE



Typical Applications

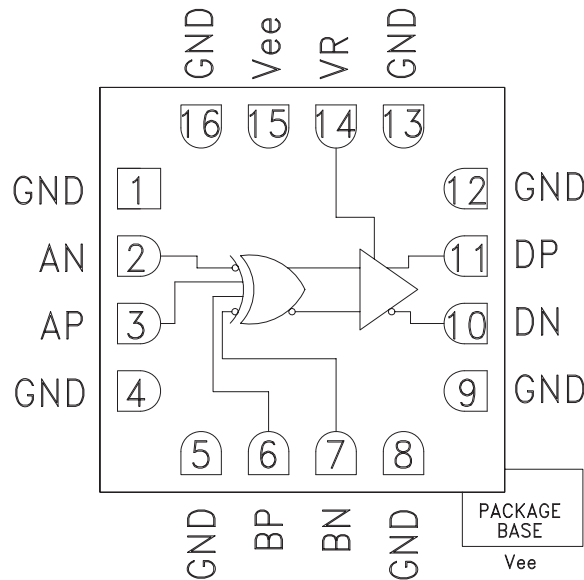
The HMC721LP3E is ideal for:

- 16 G Fiber Channel
- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 14 Gbps
- Digital Logic Systems up to 14 GHz

Features

- Inputs Terminated Internally in 50 Ohms
- Differential or Single-Ended Operation
- Fast Rise and Fall Times: 19 / 18 ps
- Low Power Consumption: 230 mW typ.
- Programmable Differential Output
Voltage Swing: 600 - 1200 mVp-p
- Propagation Delay: 95 ps
- Single Supply: -3.3 V
- 16 Lead 3x3 mm SMT Package: 9 mm²

Functional Diagram



General Description

The HMC721LP3E is a XOR/XNOR gate function designed to support data transmission rates of up to 14 Gbps, and clock frequencies as high as 14 GHz.

All differential inputs to the HMC721LP3E are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC721LP3E also features an output level control pin, VR, which allows for loss compensation or signal level optimization. The HMC721LP3E operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package..

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{ee} = -3.3\text{ V}$, $VR = 0\text{ V}$

| Parameter | Conditions | Min. | Typ. | Max | Units |
|--------------------------|----------------------------|------|---------|------|-------|
| Power Supply Voltage | | -3.6 | -3.3 | -3.0 | V |
| Power Supply Current | | | 70 | | mA |
| Maximum Data Rate | | | 14 | | Gbps |
| Maximum Clock Rate | | | 14 | | GHz |
| Input Voltage Range | | -1.5 | | 0.5 | V |
| Input Differential Range | | 0.1 | | 2.0 | Vp-p |
| Input Return Loss | Frequency <14 GHz | | 10 | | dB |
| Output Amplitude | Single-Ended, peak-to-peak | | 550 | | mVp-p |
| | Differential, peak-to-peak | | 1100 | | mVp-p |
| Output High Voltage | | | -10 | | mV |
| Output Low Voltage | | | -560 | | mV |
| Output Rise / Fall Time | Differential, 20% - 80% | | 19 / 18 | | ps |

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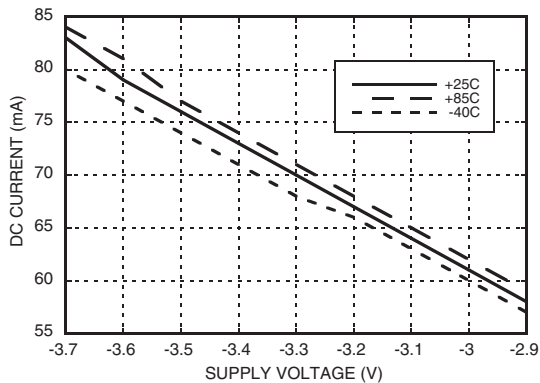


Electrical Specifications (continued)

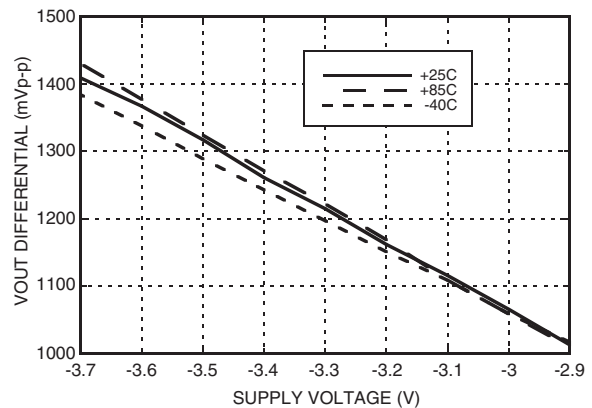
| Parameter | Conditions | Min. | Typ. | Max | Units |
|--------------------------|---|------|------|-----|--------|
| Output Return Loss | Frequency <13 GHz | | 10 | | dB |
| Small Signal Gain | | | 27 | | dB |
| Random Jitter Jr | rms | | | 0.2 | ps rms |
| Deterministic Jitter, Jd | peak-to-peak, 2 ¹⁵ -1 PRBS input [1] | | 2 | | ps, pp |
| Propagation Delay, td | | | 95 | | ps |
| VR Pin Current | VR = 0.0 V | | 2 | | mA |
| VR Pin Current | VR = +0.4 V | | | 3.5 | mA |

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 13 GHz, 2¹⁵-1 PRBS input, and a single-ended output

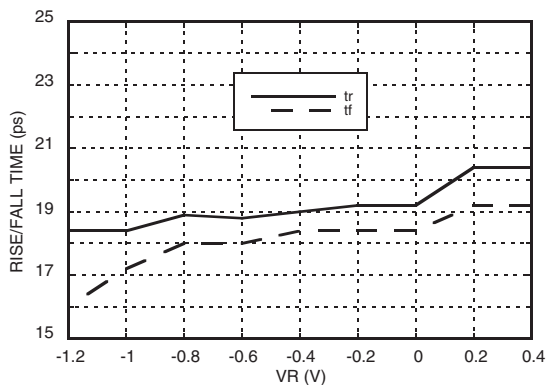
DC Current vs. Supply Voltage [1][2]



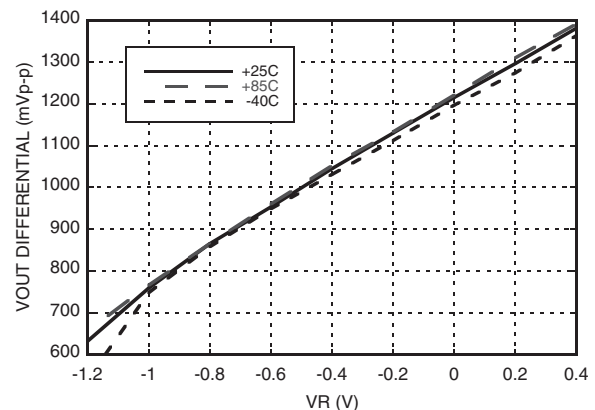
Output Differential Voltage vs. Supply Voltage [1][3]



Rise / Fall Time vs. VR [2][4]



Output Differential Voltage vs. VR [3][4]



[1] VR = 0.0 V

[2] Frequency = 13 GHz

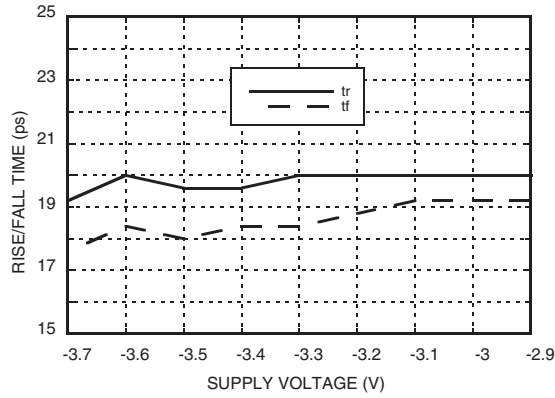
[3] Frequency = 10 GHz

[4] Vee = -3.3 V

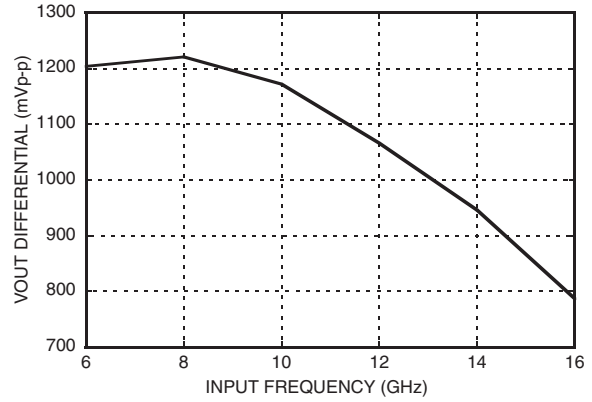


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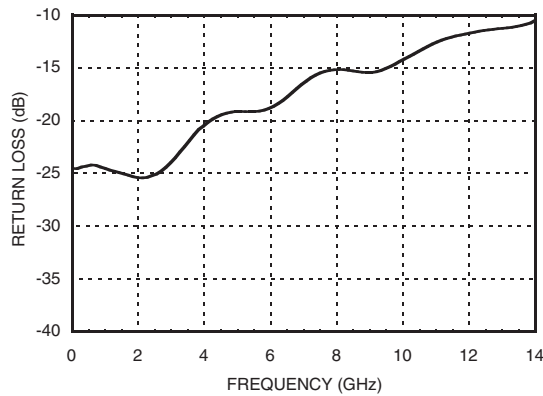
Rise / Fall Time vs. Supply Voltage [1][2]



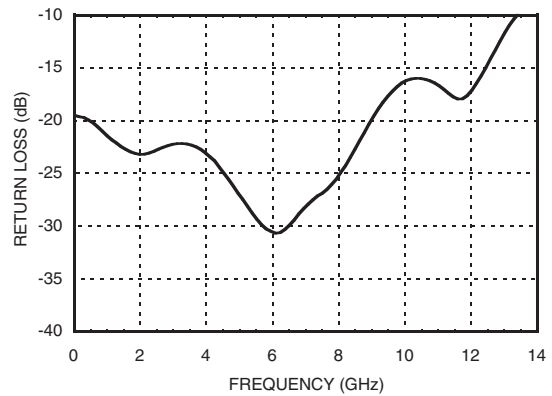
Output Differential Voltage vs. Frequency [1][3]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] VR = 0.0 V

[2] Frequency = 13 GHz

[3] Vee = -3.3 V

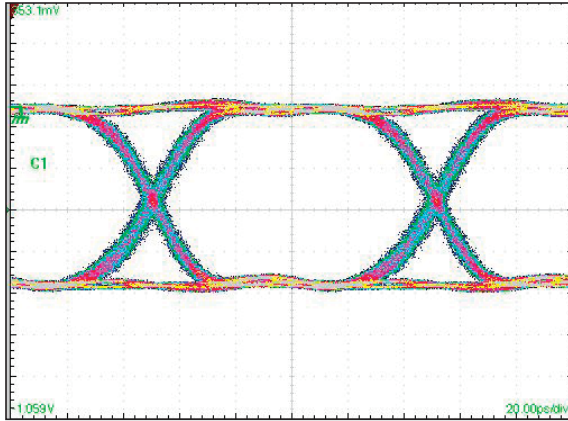
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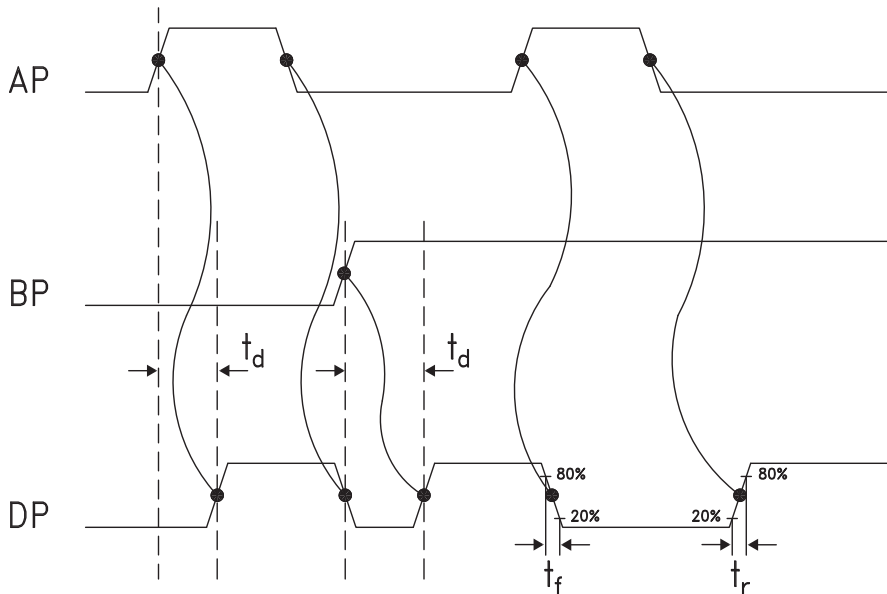
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Eye Diagram



[1] Test Conditions:
Waveform generated with an Agilent N4903A J-Bert. Rate = 10 Gbps.
Eye diagram data presented on a Tektronix CSA 8000

Timing Diagram



Truth Table

| Input | | Outputs |
|-------|---|---------|
| A | B | D |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

Notes:
A = AP - AN
B = BP - BN
D = DP - DN

H - Positive voltage level
L - Negative voltage level

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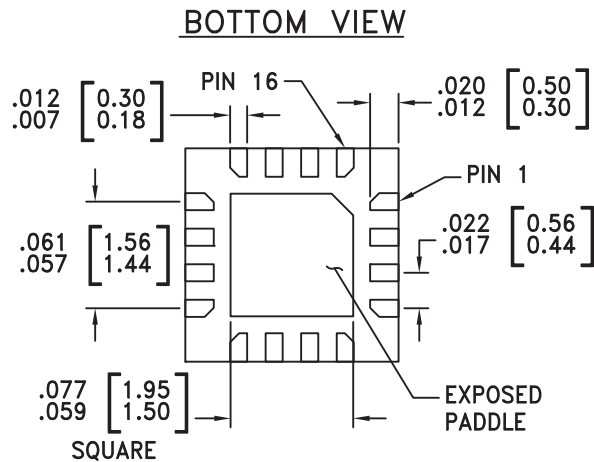
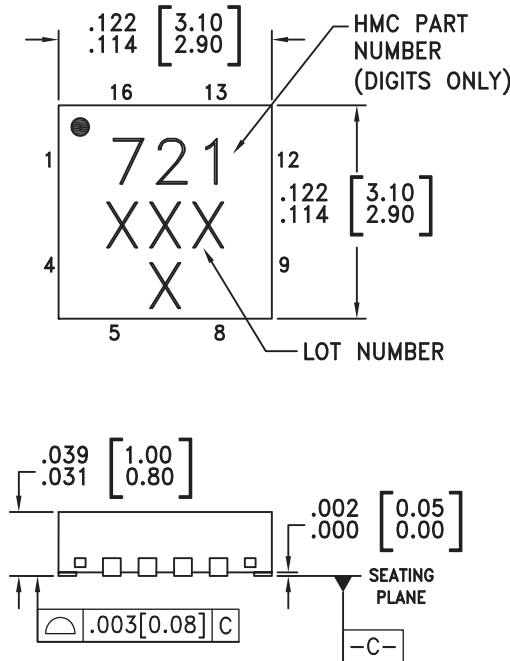
Absolute Maximum Ratings

| | |
|---|-------------------|
| Power Supply Voltage (Vee) | -3.75 V to +0.5 V |
| Input Signals | -2 V to +0.5 V |
| Output Signals | -1.5 V to +1 V |
| Junction Temperature | 125 °C |
| Continuous Pdiss (T = 85 °C) (derate 20.4 mW/°C above 85 °C) | 0.816 W |
| Thermal Resistance (Rthj-p) Worst case junction to package paddle | 49 °C/W |
| Storage Temperature | -65 °C to +150 °C |
| Operating Temperature | -40 °C to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.
8. PADDLE MUST BE SOLDERED TO Vee.


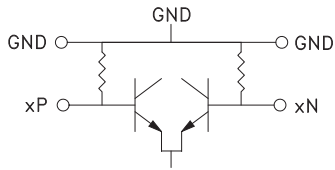
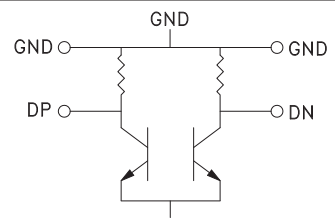

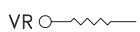
Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC721LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | 721 XXXX |

[1] Max peak reflow temperature of 235 °C
 [2] Max peak reflow temperature of 260 °C
 [3] 4-Digit lot number XXXX

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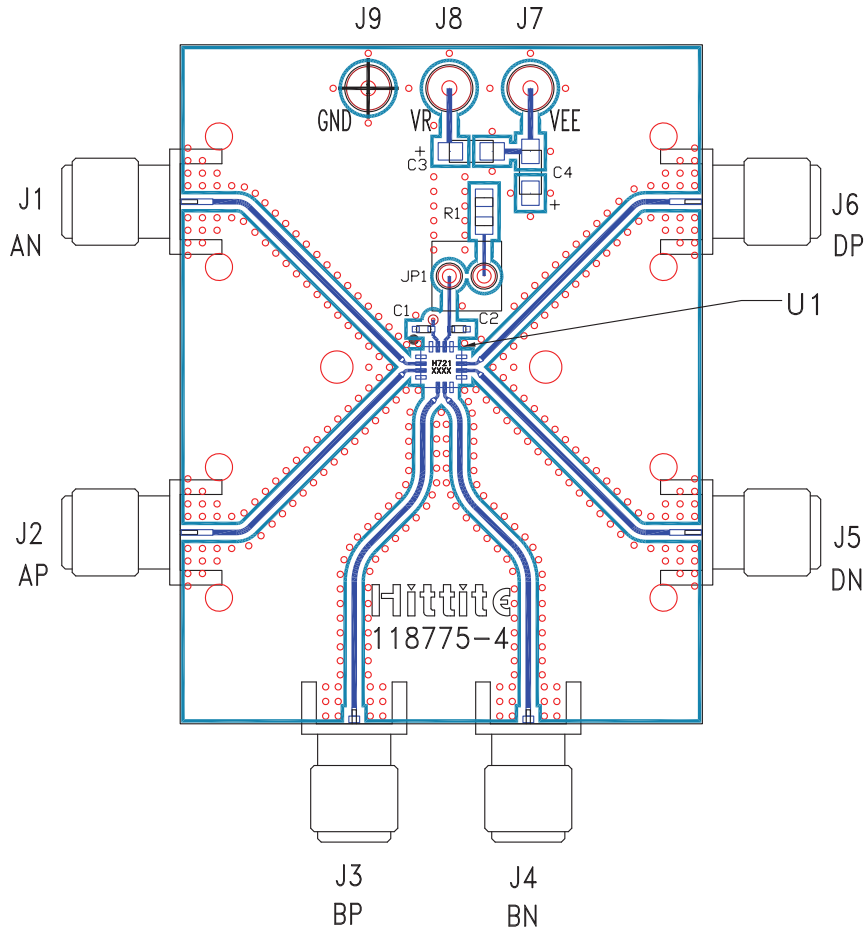
Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---------------------|------------------|--|---|
| 1, 4, 5, 8, 9, 12 | GND | Signal Grounds |  |
| 2, 3 6, 7 | AN, AP BP, BN | Differential Clock / Data Inputs: Current Mode Logic (CML) referenced to positive supply |  |
| 10, 11 | DN, DP | Differential Clock / Data Outputs: Current Mode Logic (CML) referenced to positive supply |  |
| 13, 16 | GND | Supply Ground |  |
| 14 | VR | Output level control. Output level may be adjusted by either applying a voltage to VR per "Output Differential vs. VR" plot. |  |
| 15, Package Base | Vee | Negative Supply | |

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Evaluation PCB



List of Materials for Evaluation PCB 118777 [1]

| Item | Description |
|---------|---|
| J1 - J6 | PCB Mount SMA RF Connectors |
| J7 - J9 | DC Pin |
| JP1 | 0.1" Header with Shorting Jumper |
| C1, C2 | 100 pF Capacitor, 0402 Pkg. |
| C3, C4 | 4.7 μF Capacitor, Tantalum |
| R1 | 10 Ohm Resistor, 0603 Pkg. |
| U1 | HMC721LP3E High Speed Logic, XOR / XNOR |
| PCB [2] | 118775 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

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Application Circuit

