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TEA19051B and TEA19032B QC4(+) secondary-side SMPS controller

Rev. 1 — 23 April 2018

Application note

Revision history

Revision history

Rev	Date	Description
v.1	20180423	first issue

1   Introduction

The TEA19051B is a secondary side SMPS controller with an embedded Digital Signal Processor that supports the USB Power Delivery 2.0 (USB-PD2), USB-PD3, QC2, QC3, PPS, QC4, and QC4+ protocols via a USB Type-C cable connection (Ref. 1).

Figure 1 and Figure 2 show the typical application diagrams. Table 1 and Table 2 provide further details on pinning functionality. The TEA19051B is available in an HVSON16 package and an SO14 package. The TEA19032B is the same secondary side controller, but in an SO10 package.

A complete smart-charging Switch Mode Power Supply (SMPS) can be built in combination with the TEA193x primary controller and the TEA199x secondary side SR controller. Due to its small component count, a small form factor SMPS can be built that meets efficiency requirements like CoC Tier-2, EuP Iot6, and DOE v6 with an extremely no-load power (< 30 mW).

For communication with the consumer device, information exchange is established via the DP and DM pins for QC2 and QC3 protocols. The USB-PD and QC4(+) protocols use the CC1 and CC2 lines for communication.

Resulting control and protection information is directed to the primary side controller by adjusting the optocoupler current. Consumer devices requiring output currents exceeding 3 A must either use a captive cable or apply USB-PD e-marking. The TEA19032/TEA19051B does not support the VCONN mechanism, which supplies powered cables.

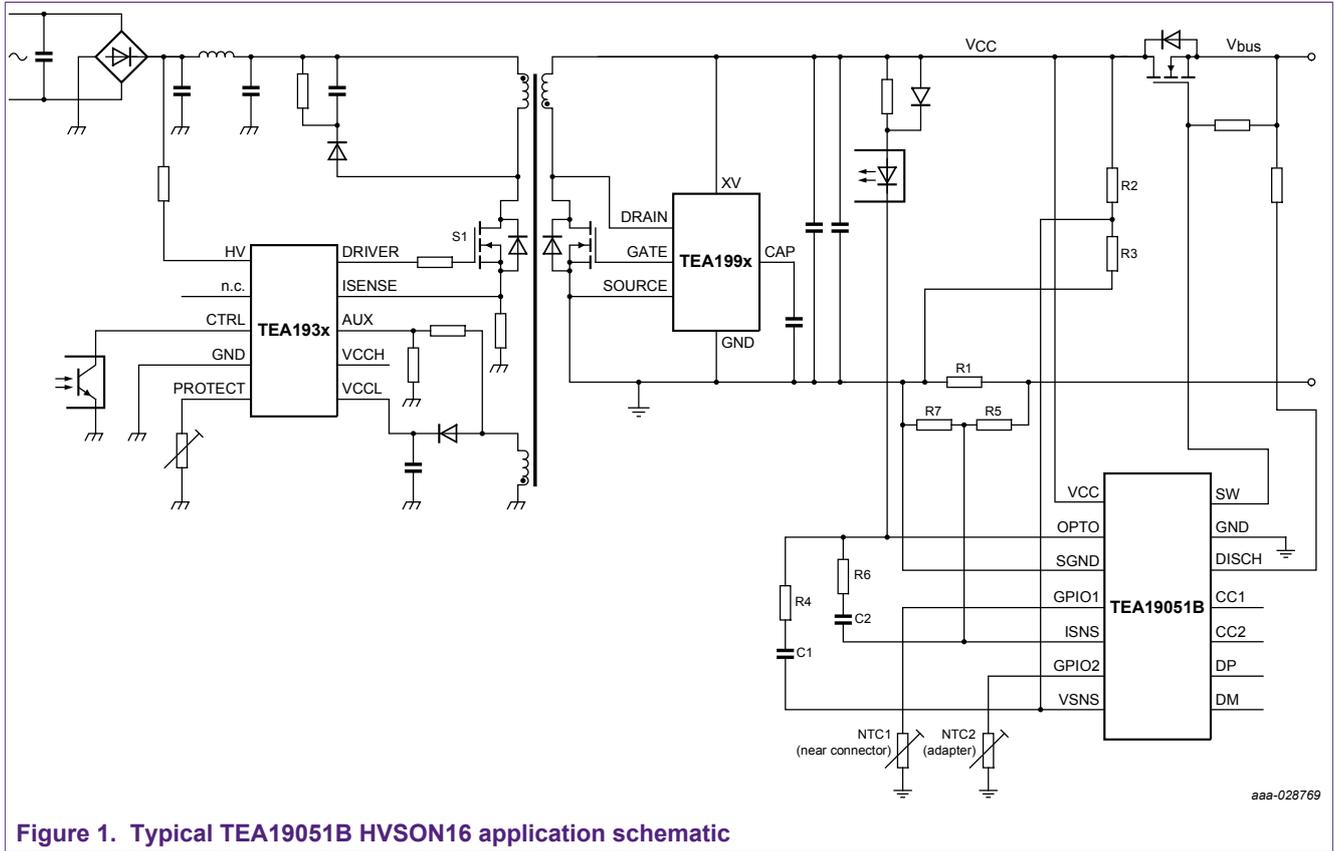## 1.1 Application diagrams and pinning information

1.1.1 TEA19051B

Figure 1. Typical TEA19051B HVSON16 application schematic

aaa-028769

Table 1. TEA19051B pin description

Symbol	Pin	Description
VCC	1	supply voltage
OPTO	2	OPTO driver
SGND	3	sense ground
GPIO1	4	general purpose input/output
ISNS	5	current sense input
GPIO2	6	general purpose input/output
VSNS	7	voltage sense input
SCL	8	I^2C clock time
SDA	9	I^2C data
DM	10	negative terminal of the data communication line
DP	11	positive terminal of the data communication line

Symbol	Pin	Description
CC2	12	type C CC2 line detection and USB-PD communication
CC1	13	type C CC1 line detection and USB-PD communication
DISCH	14	fast discharge sink
GND	15	ground
SW	16	NMOS gate drive output
EDP	17	exposed die pad

1.1.2   TEA19032B
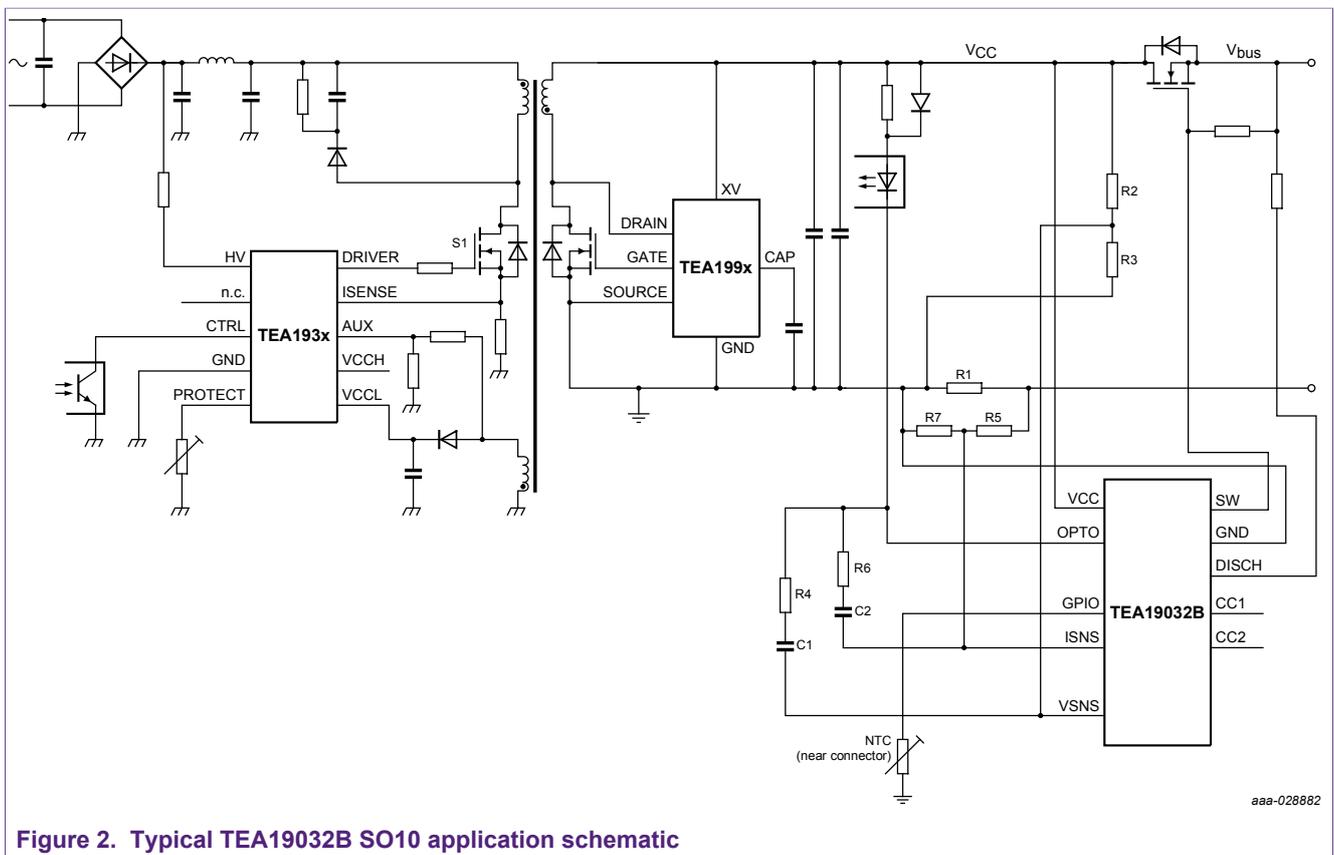
Figure 2. Typical TEA19032B SO10 application schematic

Table 2. TEA19032B pin description

Symbol	Pin	Description
VCC	1	supply voltage
OPTO	2	OPTO driver
GPIO	3	general purpose input/output
ISNS	4	current sense input
VSNS	5	voltage sense input
CC2	6	type C CC2 line detection and USB-PD communication

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Symbol	Pin	Description
CC1	7	type C CC1 line detection and USB-PD communication
DISCH	8	fast discharge sink
GND	9	ground
SW	10	NMOS gate drive output

1.2 Internal parameter settings

The TEA19032B (Ref. 3) and TEA19051B (Ref. 4) data sheet shows that multiple settings are available, making it a versatile device. Each variant targets a specific application power level. Table 3 shows, as example, the popular 27 W QC4+ settings (TEA19051BAA).

Table 3. TEA19051BAA (27 W QC4+ configuration)

Function	TEA19051BAATK
power rating	27 W
supported standards	USB-PD3[1]; QC4+
default output voltage	5 V
default maximum output current	3 A
GPIO1 function	NTC with OTP
GPIO1 protection level	90 °C
GPIO2 function	NTC with OTP
GPIO2 protection level	90 °C
chip OTP trigger level	113 °C
external sense resistor (R_{sense})	10 mΩ
external resistor divider VCC/VSNS (= DIV)	5.476
cable compensation	117 mV/A
CC mode or OCP	CC mode
OCP level/CC mode margin	5 %
PDO1	
PPS enable	FALSE
voltage	5 V
current	3 A
OVP level	125 %
UVP level	off
QC enable	TRUE
cable compensation enable	TRUE

Function	TEA19051BAATK
PDO2	
PPS enable	FALSE
voltage	9 V
current	3 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO3	
PPS enable	FALSE
voltage	12 V
current	2.25 A
OVP level	120 %
UVP level	60 %
QC enable	TRUE
cable compensation enable	TRUE
PDO4	
PPS enable	TRUE
maximum voltage	5.9 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	FALSE
OVP level	125 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

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Function	TEA19051BAATK
PDO5	
PPS enable	TRUE
maximum voltage	11 V
minimum voltage	3.3 V
maximum current	3 A
power limit enabled	TRUE
OVP level	120 %
UVP level	90 %
QC enable	FALSE
cable compensation enable	FALSE

[1] To make USB-PD3 certification possible, the DP and DM pins of the IC must not be connected. To pass BC1.2, the DP and DM pins of the connector must be connected to each other.

2   Communication protocols

The TEA19051B supports the following protocols:

- Communication via DP and DM pins:
  - BC1.2
  - Quickcharge 2.0 (QC2)
  - Quickcharge 3.0 (QC3)
- Communication via CC1 and CC2 pins:
  - USB-PD 2.0
  - USB-PD 3.0
  - Programmable Power Supply (PPS)
  - Qualcomm Quickcharge 4 Vendor Defined Messages (VDM).
- Combination of protocols:
  - QC4 = USB-PD3 + PPS + QC4 VDMs
  - QC4+ = USB-PD3 + PPS + QC4 VDMs + QC2 + QC3

The TEA19032B does not have the DP and DM pins. So, the QC2, QC3, and QC4+ protocols are not available.

3 Establishing a type-C connection

Equipped with a 330 µA pull-up current sources ($I_{CC(pu)}$) for each CC pin, the TEA19032B/TEA19051B advertises the default current capability of the converter at 3 A. A consumer with the appropriate termination resistor R_d ([Ref. 2](#)) connected to both CC lines, can detect this current capability. At the same time, the TEA19032B/TEA19051B detects the attach of a consumer. [Figure 3](#) shows a possible configuration in which the CC1 pin is used by both provider and consumer. Alternatively, the CC2 pin can be used.

a. Circuit diagram

b. Timing diagram

Figure 3. Attach and detach configuration
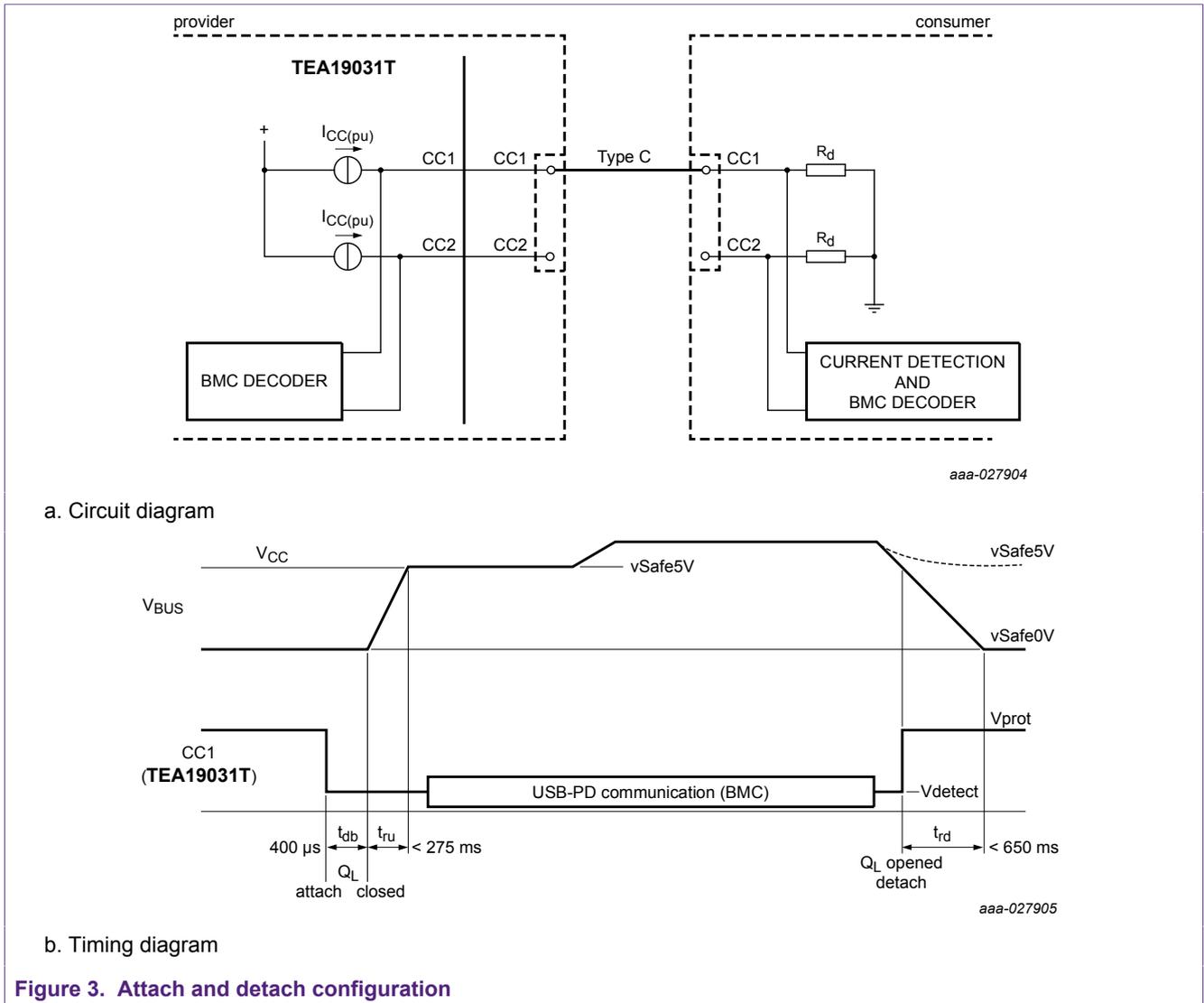
A typical attach and detach sequence starts with both the provider and consumer being unattached. Load switch QL is open and the TEA19032B/TEA19051B is waiting to detect the presence of a consumer. Detection starts when a consumer with a pull-down resistor R_d of 5.1 kΩ or 1.1 V voltage clamp is connected to one of the CC lines. Allowing ground offset in the connecting cable, the pull-down resistor or clamp in the consumer must establish a detectable voltage V_{det} between 0.85 V (V_{IL}) and 2.45 V (V_{IH}) on one of the CC pins of the TEA19032B/TEA19051B. After a debounce period t_{db} of 400 µs, but while

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an attached consumer is still detected, load switch Q_L is closed and V_{BUS} is connected to VCC.

The internally generated driver voltage on pin SW controls the load switch. This voltage exceeds V_{CC} by about 6 V. Because of the internal 80 kΩ output resistance of pin SW, the gate-source discharge resistor R_{GS} must be at least 1 MΩ. Resistor R_{GS} ensures that the load switch is in off-state in unpowered conditions.

Within 275 ms, the bus voltage must reach its 5 V level such that reliable USB-PD communication can begin. The consumer is now powered. The connected operating state lasts until the TEA19032B/TEA19051B detects a detach. Load switch Q_L opens immediately and the internal switch connected to the DISCH pin discharges V_{bus} through the external discharge resistor. The V_{bus} voltage level must return to 0 V within 650 ms which puts certain design constraints on the discharge resistor and any capacitance connected to V_{bus}. At the same time, the TEA19032B/TEA19051B ensures that the VCC level returns to 5 V by activating the internal current sink of 20 mA connected to the VCC pin.

As specified in the USB Type-C standard, alternative connection states may be present. Table 4 gives an overview of the various connection states and the corresponding TEA19032B/TEA19051B response. In all cases where a sink or Debug Accessory Mode is connected, an attach is detected.

Table 4. USB Type-C connection states and TEA19032/51B response

State	CC1 connection	CC2 connection	TEA19032/ TEA19051B response
nothing attached	open	open	no attach
sink attached	R_d[1]	open	attach
	open	R_d[1]	attach
powered cable without sink attached	R_a[2]	open	no attach
	open	R_a[2]	no attach
powered cable with sink attached	R_d[1]	R_a[2]	attach
	R_a[2]	R_d[1]	attach
	R_a[2]	R_d[1]	attach
debug accessory mode attached	R_d[1]	R_d[1]	attach
audio adapter accessory mode attached	R_a[2]	R_a[2]	-

[1] R_d = 5.1 kΩ nominal (alternatively a 1.1 V voltage clamp can be applied; Ref. 2).
[2] R_a = 1 kΩ nominal (Ref. 2)

4 USB-PD application

A TEA19032B/TEA19051B-based application in USB-PD terms, consists of a single source (provider; mains-connected charger) and a single sink (consumer; mobile device). After start-up, the TTEA19032B defaults the VCC converter output voltage to 5 V typical. It limits the current to a fixed maximum of 3 A.

After establishing a valid Type C attach, the TEA19032B/TEA19051B starts USB-PD contract negotiations by advertising its power capabilities regarding the maximum 7 PDOs (see Table 4). The consumer responds by requesting one selected PDO. When the TEA19032B/TEA19051B in return accepts this request, the contract is established. It remains in place until the consumer is detached, a hard reset occurs, or the source is unable to maintain its power level.

Table 5. Required PDO settings as function of output power

PDP (W)	5 V fixed	9 V fixed	15 V fixed	20 V fixed	5 V programmable	9 V programmable	15 V programmable	20 V programmable
x ≤ 15 W	PDP / 5	-	-	-	PDP / 5	-	-	-
15 W < x ≤ 27 W	3 A	PDP / 9	-	-	3 A or PDP / 5[2][1]	PDP / 9	-	-
27 W < x ≤ 45 W	3 A	3 A	PDP / 15	-	PDP / 5[1][2]	3 A or PDP / 9[2][1]	PDP / 15	-
45 < x ≤ 100 W	3 A	3 A	3 A	PDP / 20	-	PDP / 9[1][2]	3 A or PDP / 15[2][1]	PDP / 20[2][1]

[1] When a 5 A cable is present, the PPS may offer more than 3 A.
[2] The PPS APDO is optional.

5 USB-PD communication: PD2.0 as example

The TEA19032B/TEA19051B supports the USB-PD 2.0 and PD3.0 standard. The following sections are a limited extraction of the USB-PD2.0 standard.

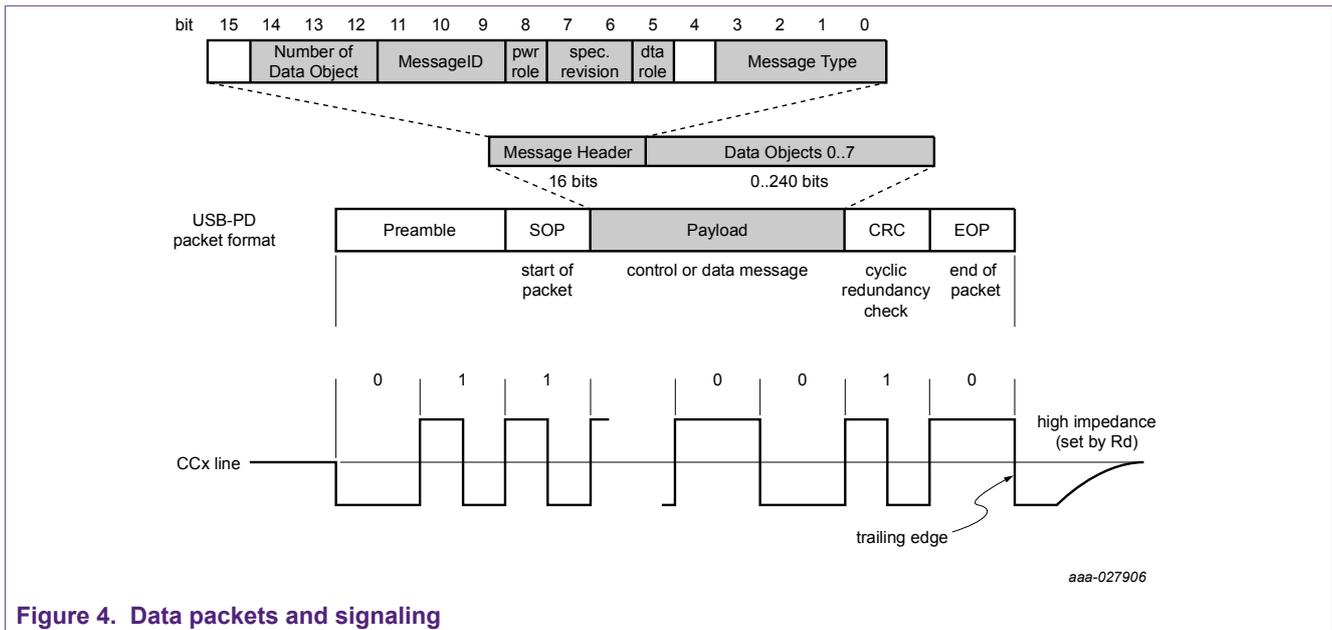## 5.1 Data packets and signaling

Figure 4. Data packets and signaling

Figure 4 shows the USB-PD2 messages. They are defined as coded packets that start with a preamble to prepare the receiver for receiving data. The preamble is followed with a Start Of Package (SOP), the actual payload, Cyclic Redundancy Check (CRC) error correction information, and finally an End Of Package (EOP).

Two kinds of packet payloads are available:

- Control message
  The payload contains only a message header in which the number of data objects (bits 14 to 12) is zero. The MessageType (bits 3 to 0) identifies the message.
- Data message
  The payload contains a message header. It is followed by one of up to seven data objects. Now, the number of data objects is non-zero.

Table 6 summarizes the supported USB-PD 2.0 messages. When the TEA19032B/TEA19051B receives an unidentified message, it responds with the reject message.

Table 6. USB-PD 2.0 supported messages

Message type	Packet payload	Send (S)/Receive (R)[1]	Description
GoodCRC	control	S/R	acknowledge that the previous message was correctly received.
Accept	control	S/R	source/sink is able meet the Request message.
Reject	control	S	source is unable to meet the Request message.

Message type	Packet payload	Send (S)/Receive (R)[1]	Description
PS_RDY	control	S	source indicates that its power supply has reached the desired operating condition.
Get_Source_Cap	control	R	sink requests a Source_Capabilities message
Soft_Reset	control	S/R	reset counters to a known state, voltage, and current settings remain unchanged.
Source_Capabilities	data	S	source exposes power capabilities with PDOs.
Request	data	R	sink response to Source_Capabilities by selecting one advertised PDO.

[1]   TEA19032B/TEA19051B (source) perspective

DC-biased Biphase Mark Code (BMC) is used for signaling the information from transmitter to receiver. BMC is self-clocked. It has at least one polarity change per bit cycle.

- 1 = polarity change at half the bit cycle
- 0 = polarity change to the next bit cycle

A packet starts by driving the active CC line to 0. To ensure that the receiver clocks the last bit before releasing the CC line to return to the DC bias level again, a packet ends with a trailing edge. The consumer pull-down resistor R_d sets the DC bias level. It includes any ground offset due to current flowing through the cable.
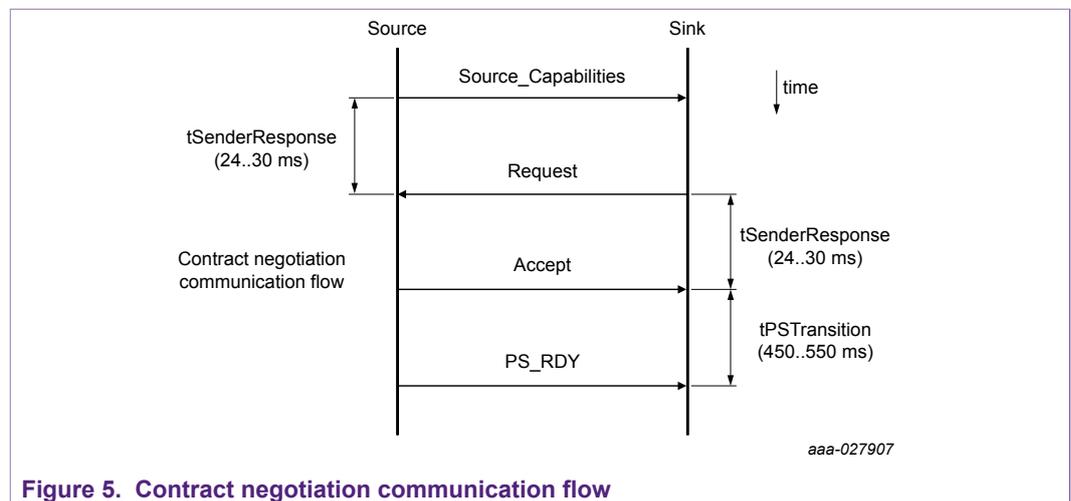
5.2   Power data object contract negotiation
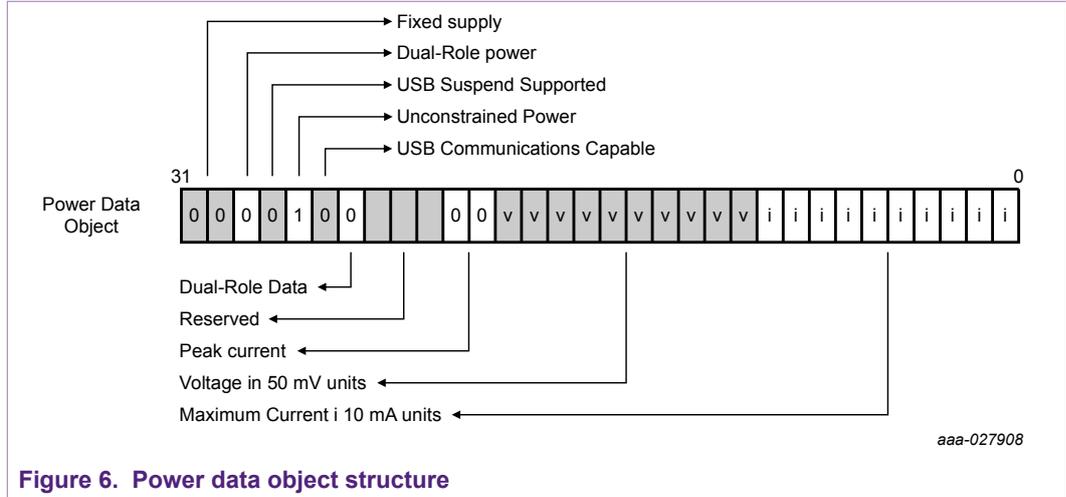

Figure 5. Contract negotiation communication flow

Figure 6. Power data object structure

After establishing a valid connection, USB-PD communication can commence. Figure 5 shows the (explicit) contract negotiation communication flow. The source initiates the negotiations by advertising a Source_Capabilities message. This message starts with a message header followed by theTEA19032B/TEA19051B-variant dependent PDOs. Each PDO contains generic information combined with the supported voltage and a maximum current level. Next, the sink selects one of the advertised PDOs and returns a Request message to the source. After validation of the Request message, the source sends an Accept message to the sink. The power control settings are changed in alignment with the request. When V_{bus} has stabilized to the newly requested level, the source sends a PS_RDY message to the sink. The contract has been established.

5.3 Hard reset

Hard reset is a USB-PD-specific ordered set of bytes recognized by the TEA19032B/TEA19051B. When detected, the result is that load switch QL is opened. To bring the converter output voltage (V_{CC}) to 5 V, the internal current sink connected to VCC is turned on. The internal switch connected to DISCH and external discharge resistor, discharges the bus voltage (V_{bus}) to 0 V for a maximum of 100 ms. Additionally, all internal counters are reset to a known state. To ensure that a new USB-PD communication sequence can start, the connection between producer and consumer remains intact. There is no limit to the number of hard reset attempts.

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6 Voltage and current sensing

In the power converter application (see Figure 2 and Figure 1), the TEA19032B/TEA19051B applies Constant-Current-Constant-Voltage (CCCV) control. It means that 2 control loops are active. The most dominant control loop determines the loop control.

6.1 Voltage divider

In voltage control mode, the voltage and the current reference levels are internally changed according to the selected PDO. To achieve the desired output voltage and current levels, some external component values must match certain criteria.

In Figure 7, the resistor divider (R3 / (R2 + R3) connected from the VCC pin to the VSNS pin, must reduce the output voltage to < 2.5 V at the maximum output voltage. To minimize undesired voltage drops, the resistor divider must be connected as close as possible to the drain of the load switch.
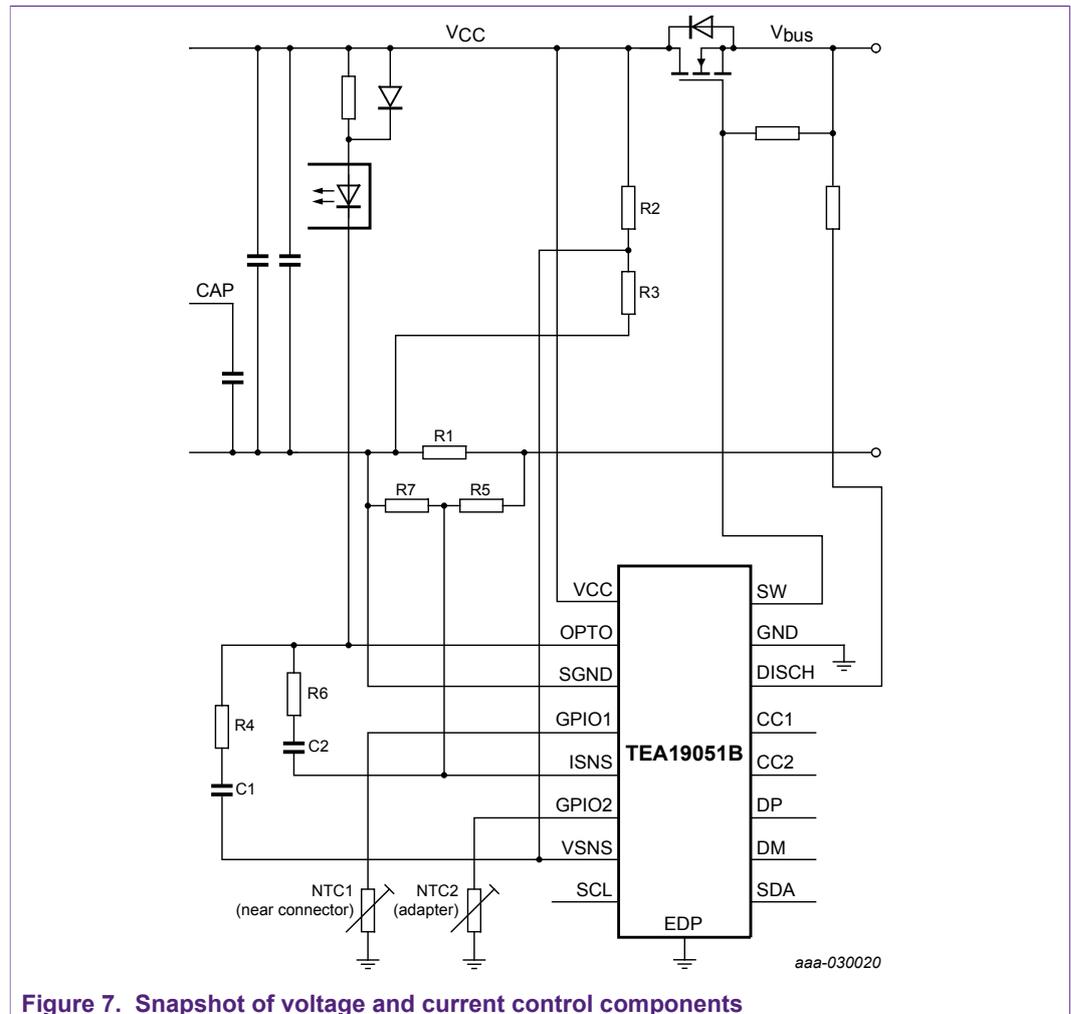
Figure 7. Snapshot of voltage and current control components

It is important that the external resistive divider exactly matches the internal value (see "external resistor divider VCC/VSNS (=DIV)" in Table 3 for the 27 W version as example).

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Internal measurements depend on it. In the resistive divider, use resistors with a 1 % or better accuracy.

6.2 Voltage loop components

In the application diagram, an integrator network is connected between the VSNS pin and the optocoupler.

The following component values are recommended:

- R2 = 160 kΩ to 180 kΩ
- R4 = 1 kΩ
- C1 = 10 nF

Magnetic coupling to this circuitry can result in offsets in the output voltage. To prevent magnetic coupling, the length and the area of the connection must be kept as small as possible.

6.3 Current sensing

In general, a sense resistor of 10 mΩ is used for applications with a maximum output current up to 3 A. When 3 A is exceeded, the value is 5 mΩ. In Figure 7, the accuracy of sense resistor R1 is very important. Any deviation from the value in the MTP gives an offset in the output current. As the sense resistor is very low-ohmic, the layout of its connections in the PCB can give major deviations from its rated value.

To overcome that, several options are available:

- Change the sense resistor value such that the complete value is matching the typical MTP value (5 mΩ or 10 mΩ).
- Trim the value with a resistor divider so that the (R7 / (R5 + R7)) × (R1 + RPCB) matches the MTP default value. RPCB is the resistance of copper wires and the resistance change of the sense resistor due to its soldering profile. After correct trimming, the current control loop meets the PPS accuracy requirements of ±150 mA.

To maximize accuracy and temperature stability, the parasitic resistance R_{pcb} must be kept very low compared to the sense resistor. The sense resistor must have a temperature coefficient that is as low as possible. To prevent magnetic coupling, the length and the area of the connections between the sense resistor and the SGND and ISNS pins, must be kept as small as possible.

Connect the exposed die pad to the GND pin. Ensure that high currents flowing through the plane below the IC are prevented.

6.4 Current loop components

For applications using the CC mode control, an integrated network is connected between the ISNS pin and the optocoupler.

The following component values are recommended:

- R5 = 330 Ω when R1 = 10 mΩ
- R5 = 160 Ω when R1 = 5 mΩ
- R6 = 5 kΩ
- C2 = 100 nF

Magnetic coupling to this circuitry can result in offsets in the output voltage. To prevent magnetic coupling, the length and the area of the connection must be kept as small as possible.

For applications that use OCP mode, these three components (R5, R6, and C2) must be omitted when the rising slope of the output voltage is longer than the 50 ms OCP blanking time.

During the rising slope of the VCC voltage, a current is injected into the current sense resistor (R7 // R5 + R_{sense}) via the optocoupler, R6 and C2. The effective current sense voltage temporarily increases the effective current sense voltage. Theoretically, it can exceed the OCP level. When the rising slope of the VCC voltage is shorter than the OCP blanking time, a possible OCP is blanked.
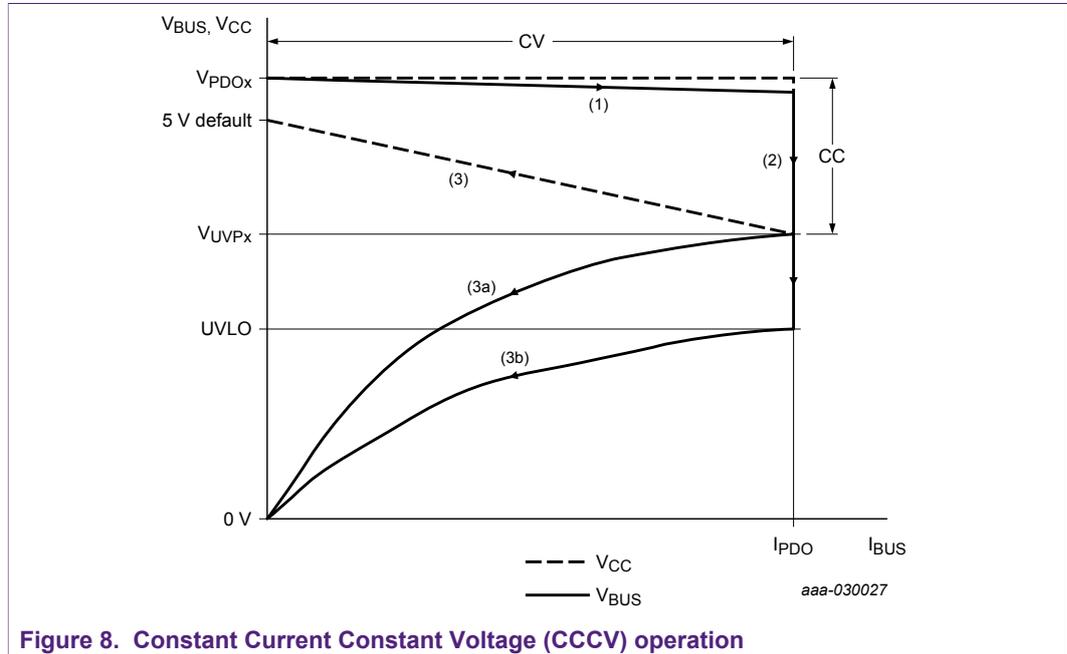
7 CCCV operation

Figure 8. Constant Current Constant Voltage (CCCV) operation

Constant Current Constant Voltage (CCCV) operation refers to a control methodology with a behavior shown in Figure 8. In region (1), the output voltage (VCC) is regulated to the selected PDO constant voltage level as long as current I_{BUS} drawn by the consumer remains below the selected maximum PDO current (IPDO).

Note: *The CC mode output current is I_{PDO}* "CC/OCP margin" that usually is 1.05 × I_{PDO} (see Table 3). It ensures that the maximum current can be delivered over the component spread. The current is only exactly as the sinks requests in PPS mode.*

Depending on the current level, the bus voltage (V_{bus}) is slightly lower because of the voltage drop over the internal channel resistance of load switch Q_L and the current sense resistor. When reaching this level and If the device is set to the Constant Current (CC) mode, the current is limited to the maximum current. The converter operates under the constant current regime (2).

The actual converter behavior now depends on the characteristics of the consumer. If the consumer behaves like a resistor or a voltage sink, the TEA19032B/TEA19051B can regulate VCC, and so also V_{bus}, to a lower voltage level. The lower voltage level balances the current supplied by the source (I_{PDO}) and the current requested by the consumer. As long as the voltage exceeds the UnderVoltage Protection (UVP) or UnderVoltage LockOut (UVLO) level, this balance can be established.

When the consumer behaves like a current sink, the balance cannot be established. The output voltage drops to the UVP or UVLO level. In either case, load switch Q_L opens and V_{CC} returns to 5 V (3). At the same time, V_{bus} returns to 0 V (3a or 3b). If the I_{bus} current drops to below I_{PDO} before reaching UVP or UVLO, the bus voltage returns to the constant voltage regime (V_{PDOx}).

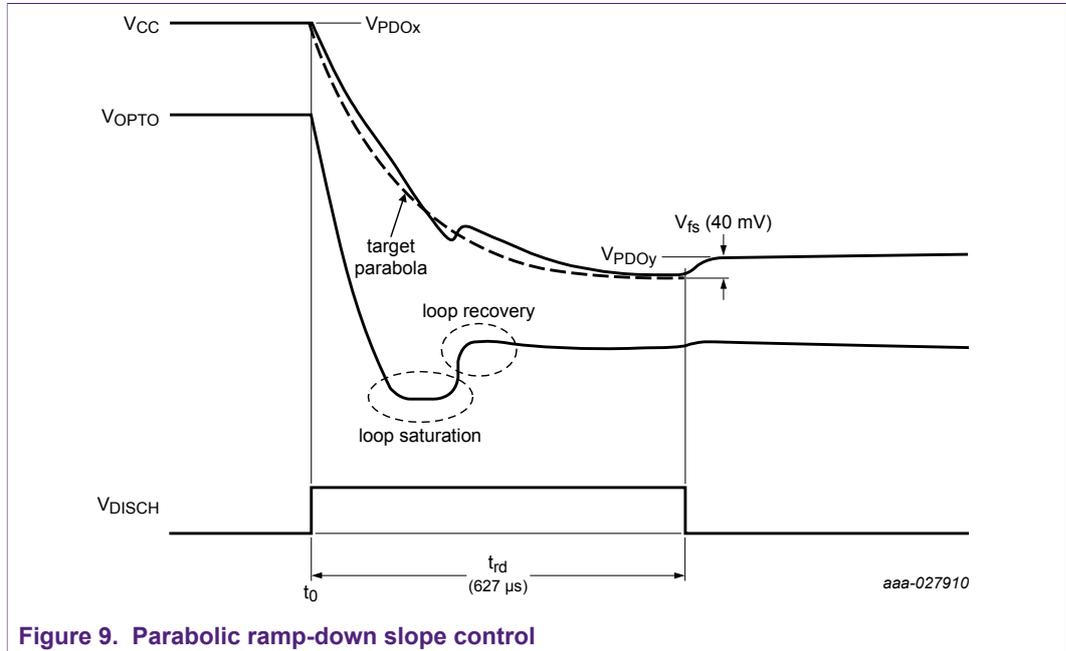# 8   Parabolic slope control

Figure 9. Parabolic ramp-down slope control

Changes in the PDO selection during USB-PD communication result in a new V_{bus} voltage (V_{PDOx}) and maximum current (I_{PDOx}) settings. The changes in the internal current set point, both up and down, are done in a single step.

When the newly requested output voltage level is higher than the currently active one, the TEA19032B/TEA19051B changes the internal control set point in a single step. When the primary side controller delivers more power to the output of the converter, the result is a ramp-up. When the new output voltage level is lower than the currently active setting, additional precautions must be taken to ensure that the control loop remains unsaturated at the end of the ramp-down transition period (t_{rd}). If not, any load step directly after the transition can result in an undesired output voltage transient.

To provide the best voltage ramp-down, an advanced parabolic ramp-down algorithm (patent pending) is implemented. The internal discharge switch connected to the DISCH pin is activated. When voltage transition is initiated at t0, it provides a discharge current sink. The TEA19032B/TEA19051B calculates a parabolic target reference level and regulates the V_{CC} output voltage accordingly. The initial steep slope of the parabola causes the internal voltage error amplifier to saturate. This effect is unavoidable. It results from the external voltage compensation network. The velocity of change in the target parabola slows down progressively and the error amplifier can "catch-up" with the reference level. The best performance is achieved by applying a small 40 mV reference step-up just before reaching the target.

In the ramp-up and ramp-down situations, the TEA19032B/TEA19051B sends a PS_RDY signal to the sink immediately after reaching respectively 95 % and 105 % of the new setting. It includes any cable compensation offset.

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8.1 PPS mode and loop saturation

In PPS mode, the requirements to the voltage loop settling time is more stringent. In this mode, the chip switches over to a linear control algorithm to meet the required timing. So, loop saturation can more easily occur, which can result in undershoot of the output voltage.

Slightly modifying the voltage sense and the optocoupler circuit as is shown in Figure 10 (R50, R55) can prevent undershoot. During an output voltage transient down, R55 gives local feedback. The increased optocoupler current induces a voltage across R55 that slightly lower the sensed voltage. As result, the voltage loop error signal and the optocurrent get lower. The decrease of the voltage loop error signal and the optocurrent results in a slower discharge of the voltage loop capacitor C38. Consequently, a lower chance for loop saturation (pin 2 getting out of the regulation range of the chip).

A second, less favorable option, is to add a diode across the resistor in series with the optocoupler. This diode is D1 in Figure 7. It limits the lowest optopin voltage to $V_{CC} - V_d - V_{opto}$. An output voltage of up to 9 V is sufficient for a single diode. When the output voltage exceed 9 V, two diodes are required. Otherwise, the control voltage remains too high and cannot drop to below the regulation range of the chip. In that case, too much power is delivered to the output when the output steps to minimum load. The result is an output voltage that is too high.

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Figure 10. Secondary side of the 65 W demo board

9 Protections

9.1 Protections overview

Table 7 gives an overview of all available protections. All protections, except UVP, are implemented in hardware. So, they are functional under all conditions, even if the internal TEA19032B/TEA19051B digital signal processor stalls. When triggered, a protection causes a safe restart with a 1 s repetition interval or a latched response.

Table 7. Protections overview

Protection[1]	Description	Design	Level	Delay	Response
UVLO	undervoltage lockout	hardware	VUVLO(f) (2.8 V) VUVLO(r) (3.0 V)	0 µs[2]	restart
OSP	output short protection	hardware	see UVLO or UVP	-	restart
OVP	overvoltage protection	hardware	V_{ovp}[3][4]	30 µs	restart
UVP	undervoltage protection	software	60 %[3][4]	-	-
OCP	overcurrent protection	hardware	I_{LIM}[5]	20 ms	restart
OSUP	open supply protection	hardware	-	0 µs[2]	_[6]
OVP-CC	cc-lines overvoltage protection[7]	hardware	4.5 V	127 µs	restart
OVP-DMDP	DP/DM overvoltage protection	hardware	115 °C	127 µs	restart
OTP	overtemperature protection (internal)	hardware	115 °C	0 µs[2]	latched
NTC-OTP	overtemperature protection (external)	hardware	90 °C	0 µs[2]	restart

[1] See data sheet (Ref. 4) for variant-specific settings.
[2] Immediate response excluding any internal circuit delay.
[3] As a percentage of the V_{PDOx} level.
[4] PDO0 and PDO1 have no UVP.
[5] As a percentage of the I_{PDOx} level.
[6] VCC supply voltage lost, load switched is opened.
[7] The active CC attach detection line only.

9.2 Safe-restart response

Figure 11 shows the safe-restart mode timing diagram. In safe-restart mode, load switch Q_L is turned off (t1) after the protection is triggered (t0) and expiration of the protection-dependent delay time. The attached consumer is decoupled from the producer.

Supported by an internal current sink of typically 20 mA, the TEA19032B/TEA19051B error amplifiers regulate the converter output voltage (V_{CC}) to 5 V typical. The internal current sink remains active until V_{CC} has dropped to below a voltage level of 5 % above the typical 5 V level (t3).

The internal switch connected to DISCH is closed. It draws a discharge current from V_{bus} through resistor R_{DISCH}. The voltage on this node drops rapidly. With an interval of 1 ms, the internal DISCH switch opens for a V_{bus} measurement period of 20 µs. During this period, the TEA19032B/TEA19051B samples the bus voltage. Resistor R_{DISCH} and

any capacitance connected to the DISCH pin must be designed such that the DISCH pin voltage returns to the V_{bus} level within this measurement period.

As long as V_{bus} remains above 0.7 V (maximum 100 ms), the DISCH function remains operational. This mechanism ensures that V_{bus} drops to 0 V (t2) within the appropriate time in alignment with the USB-PD standard.

When a protection triggers the safe-restart function, the safe-restart timer is started. All circuits are reinitialized. When the 1 s safe-restart time has elapsed (t4), a new start-up sequence commences. The load switch is closed and the USB-PD contract is negotiated (t5). After reaching the requested VCC level (t6), the converter resumes normal operation. If the fault condition persists, the TEA19032B/TEA19051B enters a new protection cycle (t7).
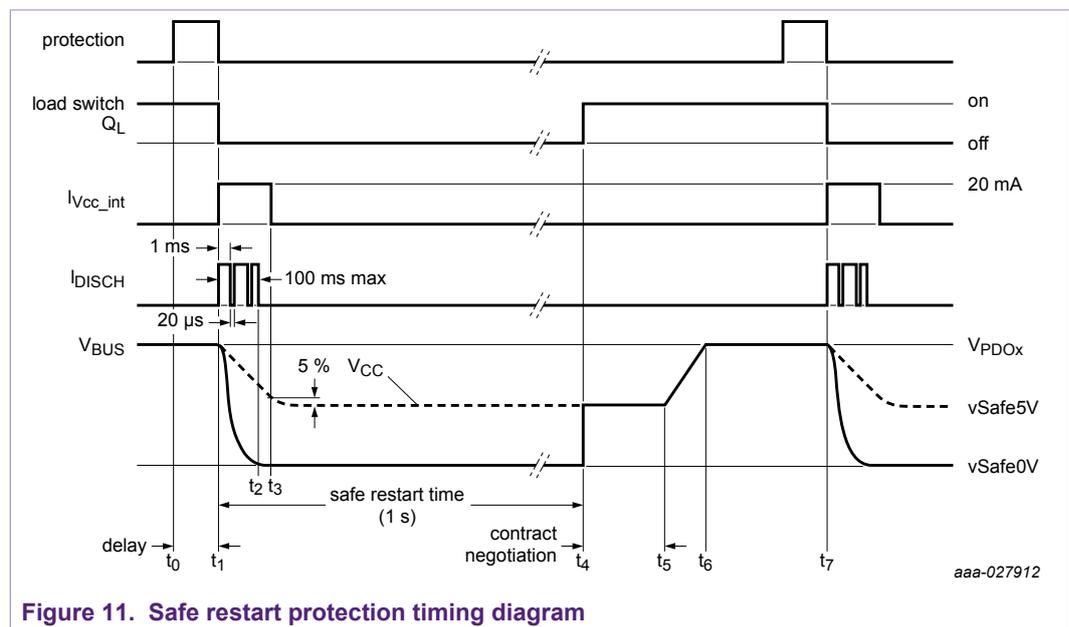
Figure 11. Safe restart protection timing diagram

9.3 Latched response
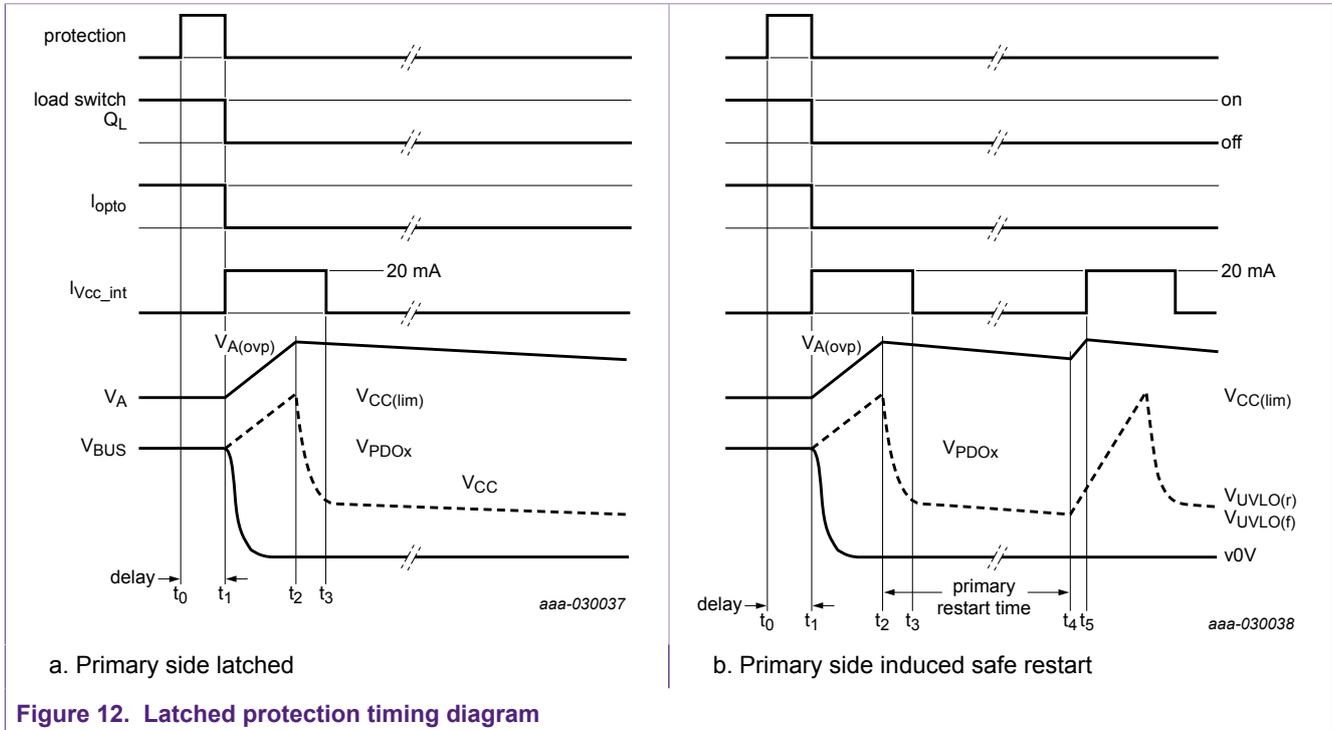
Figure 12. Latched protection timing diagram

When the actual system (primary and secondary chips) is programmed to latched response, its behavior depends on the primary-side controller behavior. Depending on the settings of the primary side controller (Ref. 4), the response is a converter latch (see Figure 12 (a)) or yet another primary-side induced save restart (see Figure 12 (b)).

After the protection is triggered (t0) and the protection-dependent delay time has expired, load switch Q_L is turned off (t1). The attached consumer is decoupled from the producer. An internal current sink current of 20 mA (typical) connected to V_{CC} is activated.

At the same time, the TEA19032B/TEA19051B reduces the optocoupler current to virtually zero. This zero optocoupler current is an indication for the primary-side controller to increase the amount of power delivered to the output of the converter so V_{CC} increases. The reflected primary-side controller supply voltage (V_A) also increases in alignment with the turns ratio of the transformer. The result is that when the controller supply voltage reaches $V_{A(ovp)}$, the overvoltage protection is triggered on the primary side (t2).

The primary-side controller stops operation of the converter. V_{CC} gradually drops to below the falling UVLO level ($V_{UVLO(f)}$) because of the TEA19032B/TEA19051B internal current sink. If there is a primary-side latched protection, the converter remains off.

When a primary-side induced safe restart is programmed, the primary-side controller initiates a new start-up cycle (t4). As soon as V_{CC} exceeds the UVLO level $V_{UVLO(r)}$, the internal current sink is turned on again (t5). The load switch remains off and the optocoupler current remains zero. This sequence is continuously repeated. The maximum V_{CC} voltage can be calculated with Equation 1. Load switch Q_L must be able to withstand this $V_{CC(lim)}$ voltage.

$$V_{CC(lim)} = \frac{n_s}{n_a} \times V_{A(ovp)} \tag{1}$$

Where:

- If a protection latches, the converter $V_{CC(lim)}$ is the maximum V_{CC} voltage.
- n_s is the number of secondary turns on the transformer.
- n_a is the number of primary-side controller supply turns on the transformer.
- $V_{A(ovp)}$ is the OVP level of the primary-side controller supply voltage (Ref. 4).

***Note:** In case of situation B (Figure 12) the output voltage (= supply voltage of the TEA19032B/TEA19051B) must not drop below ~2.7 V. If the TEA19032BTEA19051B does drop to below ~2.7 V, the Power-On Reset (POR) clears the latched protection flag. As a result, the next primary safe restart cycle causes the TEA19032B/TEA19051B to restart, basically creating a safe restart system.*

9.4 UnderVoltage LockOut (UVLO)

To ensure a well-defined internal TEA19032B/TEA19051B functionality and a proper driving of load switch Q_L, all circuits are only released when V_{CC} exceeds $V_{UVLO(r)}$. When V_{CC} drops to below $V_{UVLO(f)}$ again, the UVLO protection is triggered. This situation can occur when the connected consumer draws too much current I_{BUS} while operating in Constant Current (CC) mode (see Section 7). It can also occur when any other protection has triggered a latched response. The protection is implemented in hardware with fixed levels.
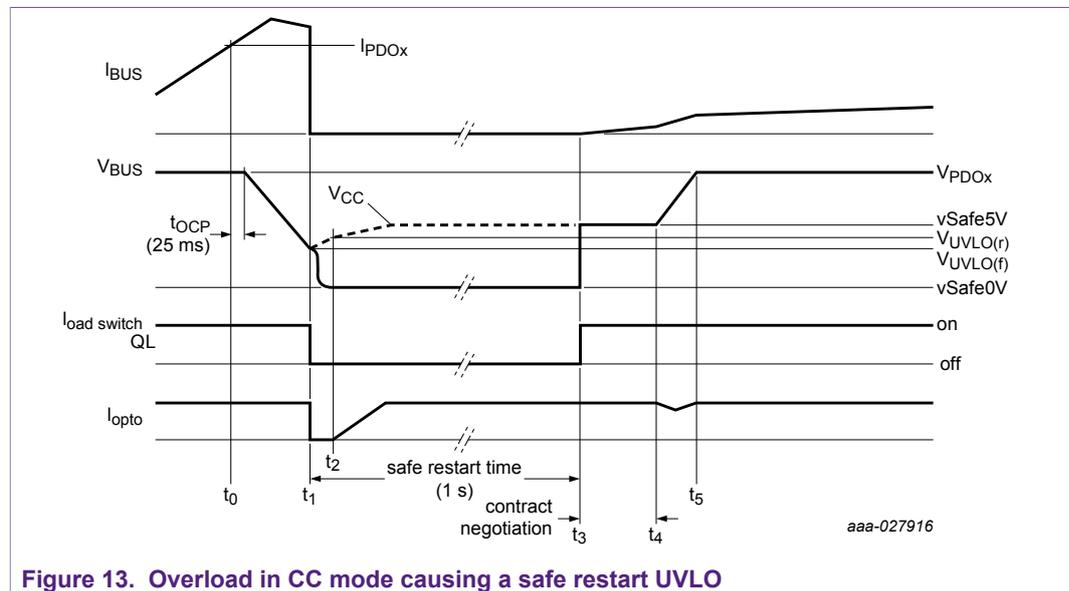
Figure 13. Overload in CC mode causing a safe restart UVLO

Figure 13 shows an overload on V_{bus} in CC mode. The overload causes V_{CC} to drop out of regulation. A safe-restart UVLO protection is triggered. The optocoupler current remains constant because of the constant current control action of the TEA19032B/TEA19051B.

The V_{CC} continues to drop. When it drops to below $V_{UVLO(f)}$, the load switch is opened immediately. It disconnects the consumer from the converter (t1). With the load disconnected and the primary side delivering full power, V_{CC} increases again. When V_{CC}

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exceeds $V_{UVLO(r)}$ (t2), the TEA19032B/TEA19051B regulates the output voltage to 5 V. After the 1 s safe restart time has elapsed, the load switch closes again (t3).

The controller awaits new contract negotiations. These negotiations must be concluded (t4) before regulation can continue toward the final V_{PDOx} level (t5). If the overload condition persists, the converter enters a new safe-restart cycle.

9.5 Preventing UVLO or overvoltage at the primary side controller

The primary converter is supplied from the auxiliary winding on the power transformer (see Figure 2). Under all load conditions, the auxiliary supply voltage must remain below the maximum voltage rating of the primary supply voltage pin and above the UVLO level. Generally, the lowest auxiliary supply voltage occurs at the lowest output voltage at no-load. The highest voltage occurs at the highest output voltage at full load.

In the TEA1936x application notes (Ref. 7), tips are given to make a proper auxiliary supply design, including the calculation for the number of auxiliary transformer turns.

9.6 Output Short Protection (OSP)

Short circuit is a special case of overload. UVLO and UVP protect against short circuits. A short circuit can occur during operation or prior to converter start-up. In both cases, when the load switch is closed, the current drawn from VCC increases rapidly. To endure this condition, the selection of the load switch must handle the worst case energy dissipation (see Equation 2) until the switch opens after the UVLO protection is triggered. The PCB tracks must sustain the corresponding high current determined by the total impedance of the load switch channel resistance, sense resistor RS, and any PCB track resistance. Careful layout must ensure that the load switch drain does not suffer from an inductive voltage spike when the load switch is turned off while carrying this high current. Similarly, a negative voltage may be induced at the source of the load switch. To avoid inductive turn-on of the load switch, which could be detrimental for the converter, this voltage must be restrained.

$$E_{QL(max)} = \frac{1}{2} \cdot C_O \cdot \left(V^2_{CC(0)} - V^2_{UVLO(f)} \right)$$
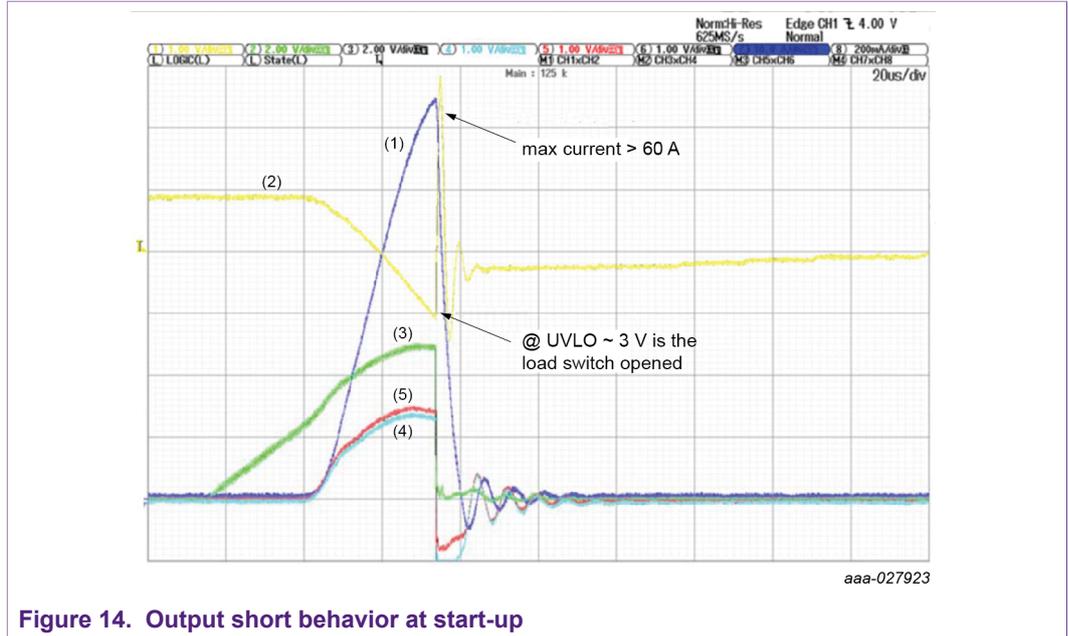
(2)

Figure 14. Output short behavior at start-up

Figure 14 shows a measured waveform of a short circuit occurrence. The maximum current increases rapidly and a sharp voltage spike can be observed on V_{CC}. The source of Q_L (V_{bus}) briefly dips to a negative level. However, it does not drop low enough to turn on the switch again, which is undesired.

The TEA19032B (Ref. 3)/TEA19051B (Ref. 1) pin voltages must never exceed the absolute maximum ratings as specified in the TEA19032 and TEA19051B data sheets.

9.7 OverVoltage Protection (OVP)
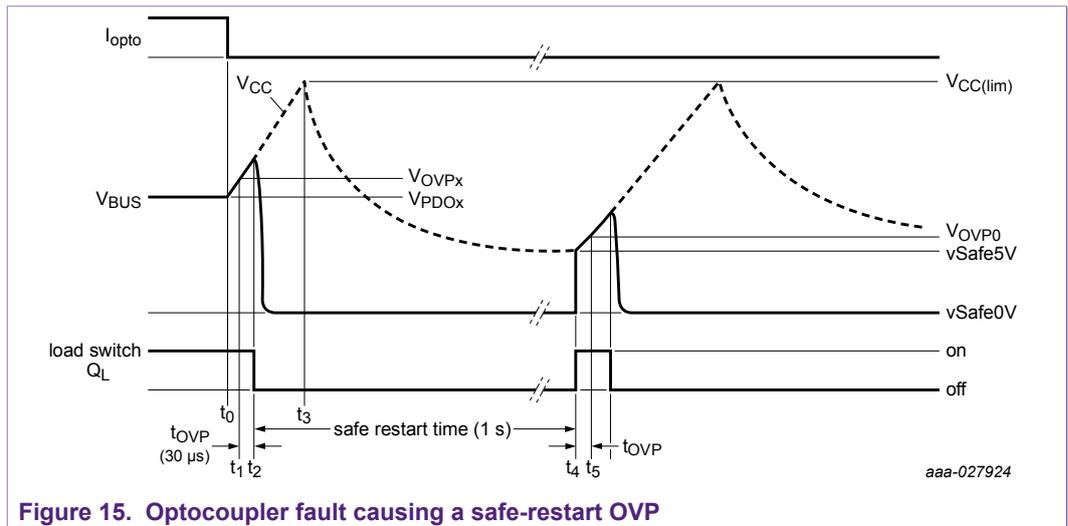
Figure 15. Optocoupler fault causing a safe-restart OVP

If the optocoupler feedback path to the primary side controller gets disrupted, the OVP, measured on pin VCC, prevents further damage to the consumer by opening load switch Q_L. Figure 15 shows an example of the OVP sequence (due to an open connection in the optofeedback path) with safe-restart response.

At t0, the optocoupler unexpectedly seizes to conduct current due to a fault condition. Although V_{CC} and V_{bus} are programmed at V_{PDOx}, both voltages start to increase. When V_{CC} reaches the corresponding protection trip level at V_{OVPx} (t1) and after a 30 μs blanking time ($t_{OVP:}$; t2), the load switch opens. The bus voltage rapidly drops to 0 V.

However, V_{CC} increases to $V_{CC(lim)}$ (t3), which depends on the primary OVP voltage (see Equation 1). When the 1 s safe-restart timer has elapsed, a new safe-restart attempt is made.

Before any USB-PD communication has taken place, the control and protection levels are reset to V_{PDO0}, which is equivalent to 5 V. It means that the new OVP trip level is at V_{OVP}. It is related to 5 V. If the optocoupler fault condition persists, a new safe restart cycle starts at t5.

9.8 UnderVoltage Protection (UVP)

When the output voltage drops too much during an overload condition, an additional UVP protection level, measured on pin VCC, can be triggered. For all PDOs except PDO0 and PDO1, this UVP level is at 60 % of the programmed V_{PDOx} level. When V_{CC} reaches UVP, a safe-restart response follows. PDO0 and PDO1 have no UVP. They rely on the UVLO protection.

Ensure that the primary converter can supply the worst case power that is including the (5 %) CC/OCP margin level. If it cannot, the UVP or UVLO is triggered under this condition.

9.9 OverCurrent Protection (OCP)

When the consumer draws a current that exceeds the limiting current level (I_{lim}), the TEA19032B/TEA19051B allows the power converter to operate in CC mode or to respond with an OCP.

Note: *The CC mode output current and the OCP level are I_{PDO} × "CC/OCP margin". Usually, it is 1.05 × I_{PDO} (see* Table 3*). In this way, the maximum current can be delivered over the component spread. Only in PPS mode, the current is exactly equal to what the sink requests.*

The limiting current level is variant-dependent (see Table 3). For details on CC mode operation and protection, see Section 7.

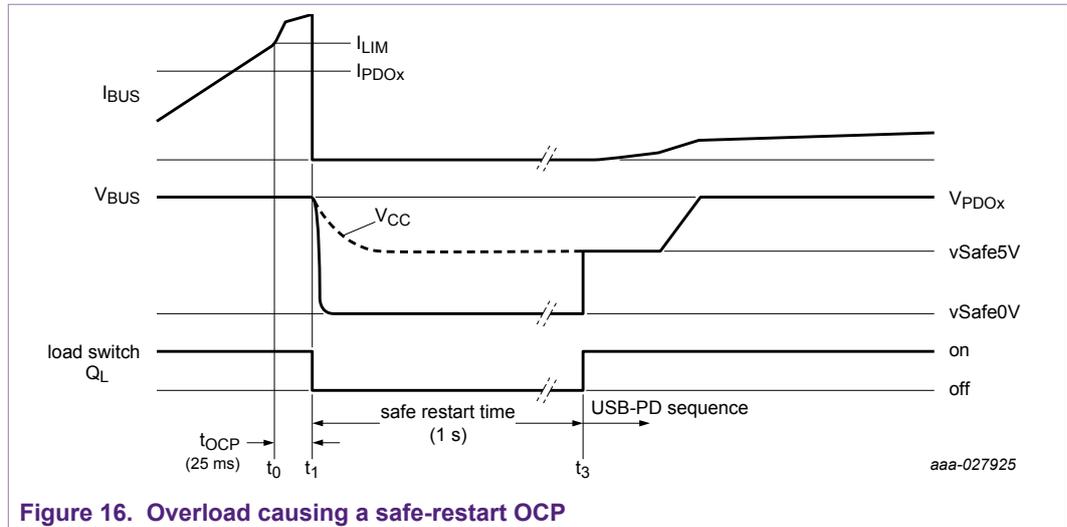Figure 16 shows the timing sequence when OCP is active.

Figure 16. Overload causing a safe-restart OCP

When a current exceeding the limiting current (I_{lim}) triggers OCP, the protection sequence is initiated (t0). The protection only becomes effective after t_{OCP} (25 ms) at t1. Load switch Q_L is opened. V_{CC} is regulated to 5 V. V_{BUS} drops to 0 V. OCP results in a safe restart. So, after the safe-restart timer has elapsed, a new USB-PD initiation cycle commences (t3).

9.10 Open-SUpply Protection (OSUP)

To ensure unconditional protection of the consumer, the TEA19032B/TEA19051B uses the available voltage on the OPTO pin to turn off load switch Q_L immediately if there is an unexpected supply voltage (V_{CC}) failure. When V_{CC} is restored, the controller resumes normal operation.

9.11 Internal OverTemperature Protection (OTP)

If the internal temperature of the TEA19032B/TEA19051Bexceeds 115 °C (see Table 3), a latched protection is triggered.

9.12 NTC thermal protection (external OTP)

In addition to the internal temperature protection, an external temperature protection is available via the NTC pin. A 47 kΩ NTC resistor with a β-constant of 4050 (e.g. EPCOS B57321V2473J060 or Murata NCU18WB473F60RB) must be connected to the NTC pin of the TEA19032B/TEA19051B. When the external temperature exceeds the NTC-OTP trip level of 90 °C (t0; see Table 3), a safe restart is initiated. When the safe restart timer has elapsed (t1) and while the external temperature remains above 78 °C, the TEA19032B/TEA19051B suspends converter start-up. Figure 17 shows the relation between Beta(NTC) and the OTP trip level.

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Figure 17. External OTP via NTC resistor
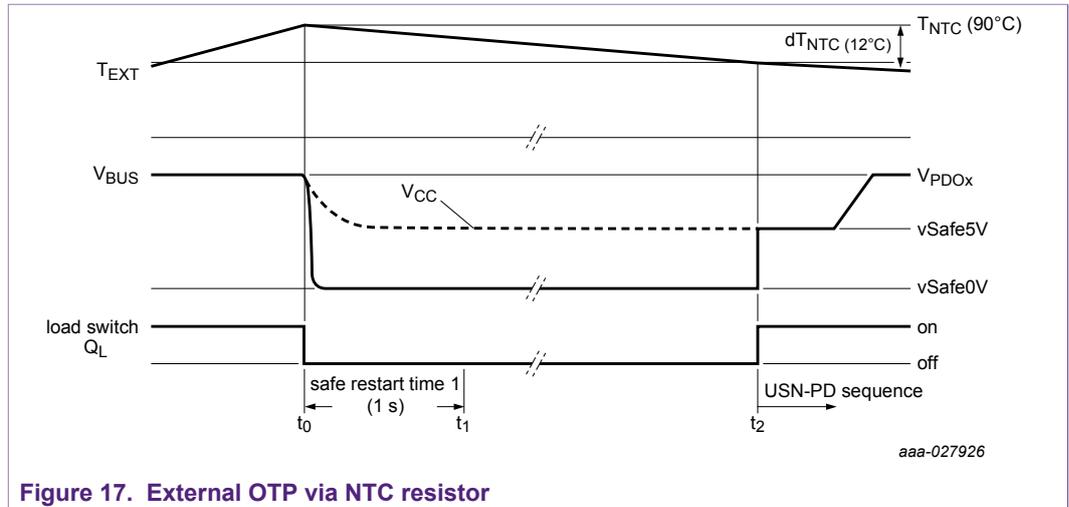
When the external temperature drops to below this lower temperature boundary (t2), the TEA19032B/TEA19051B releases the converter for a new USB-PD communication sequence. At this lower temperature level, the NTC value has decreased to about 4 kΩ.

The TEA19051B has 2 pins available for NTC connections, GPIO1 and GPIO2. NTC1 (connected to GPIO1) must be placed close to the connector. NTC2 (connected to GPIO2) must be placed on a spot that carries the average adapter temperature. In QC4 mode, the sink (e.g. cell phone) can request these temperatures from the adapter. In the TEA19032B, only the connector temperature is measured.

If temperature measuring is not required, a 47 kΩ resistor can replace the NTC. In that situation, the adapter reports back a temperature of 25 °C.

The nominal level (β = 4108) is set to 90 °C.

Figure 18. OTP trip level as a function of Beta(NTC)
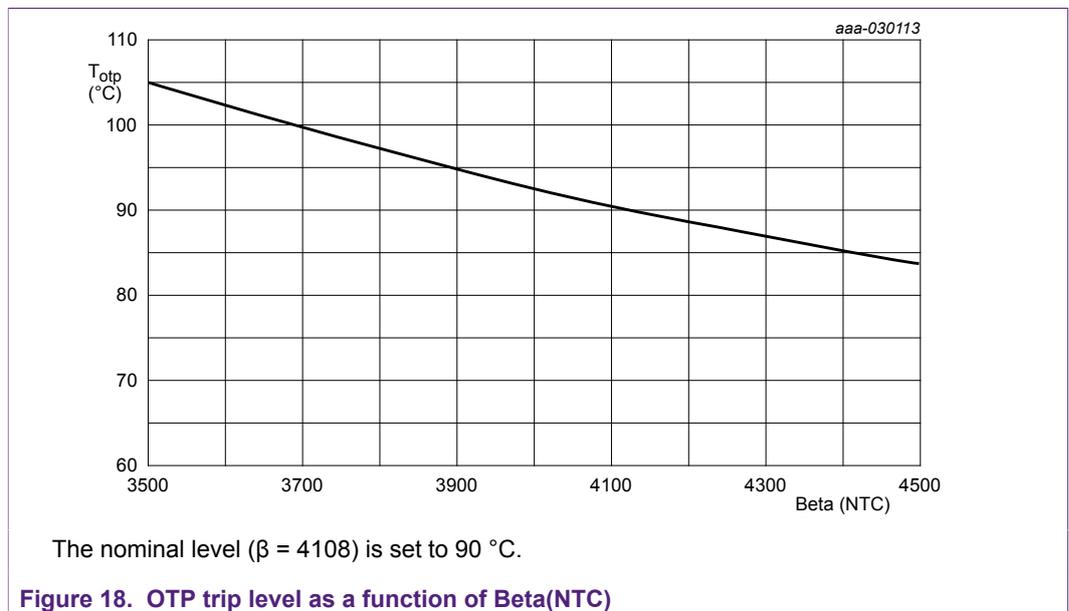
9.13 Communication interface protection

Immediately after attach detection, the active CC detection line trigger the OVP at 4.5 V. When the protection is triggered, a safe-restart cycle is initiated. The second CC line is not protected.

9.14 Protection counter

In PD mode, every time a protection is triggered, the TEA19051B/3 increases the protection counter by 1. When the counter reaches 7 (= 7 safe restarts), the load switch is opened. The output voltage remains 0 V. When either the type-C cable is unplugged or the mains voltage is removed, the protection counter is reset.

9.15 ESD diode and resistors

To prevent damage during board level ESD events, ESD diodes must be placed on the board as is shown in Figure 19.
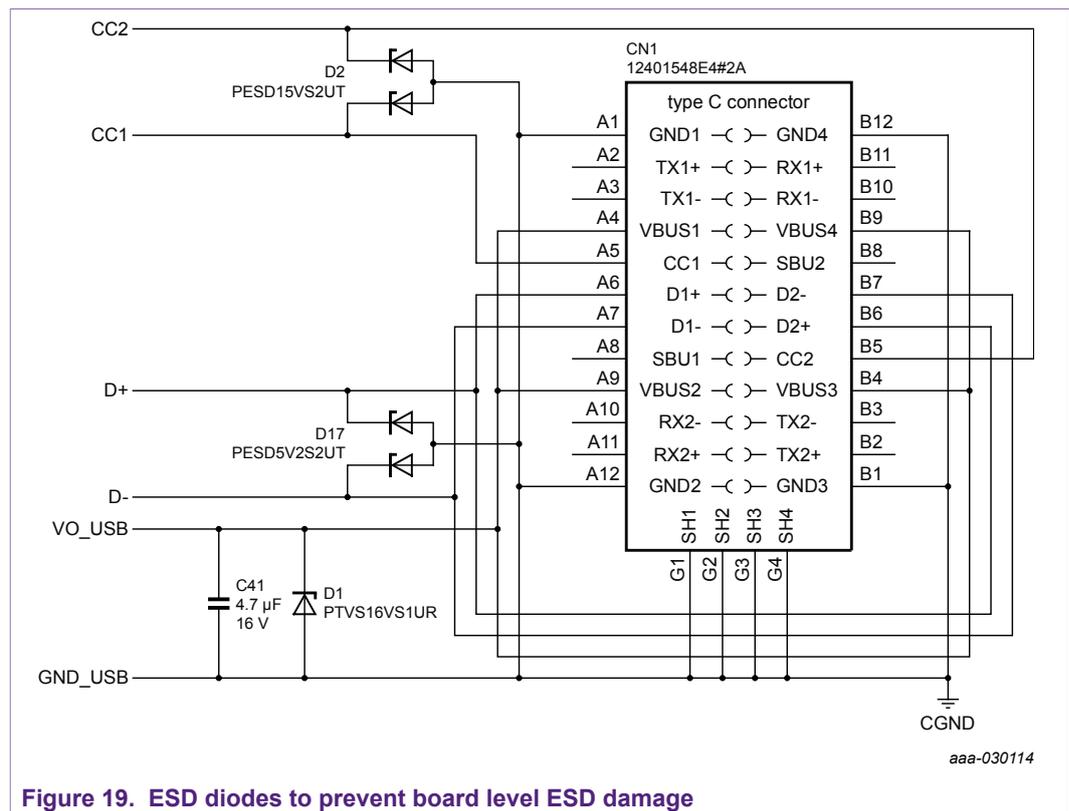
Figure 19. ESD diodes to prevent board level ESD damage

For further protection, behind these ESD diodes, a series resistance of 22 Ω must be placed to the CC1 and CC2 pins, and 10 Ω toward the DM and DP pins (see Figure 20).

In a board level ESD event, the high peak current finds the lowest impedance route between the Type-C connector and the Line/Neutral mains lines. So, the desired ESD patch must be low ohmic and not contain any inductors. Inductors have a high impedance for these fast ESD events. A good example is depicted in Figure 21 and Figure 22. A board level ESD zap at the output voltage terminal of the USB-PD

connector, flows directly via the spark gap to the Neutral connection of the mains. When the low ohmic and low inductance connections are not obeyed, fast rising, high peak voltages occur that can cause malfunctioning or worst-case component failure.
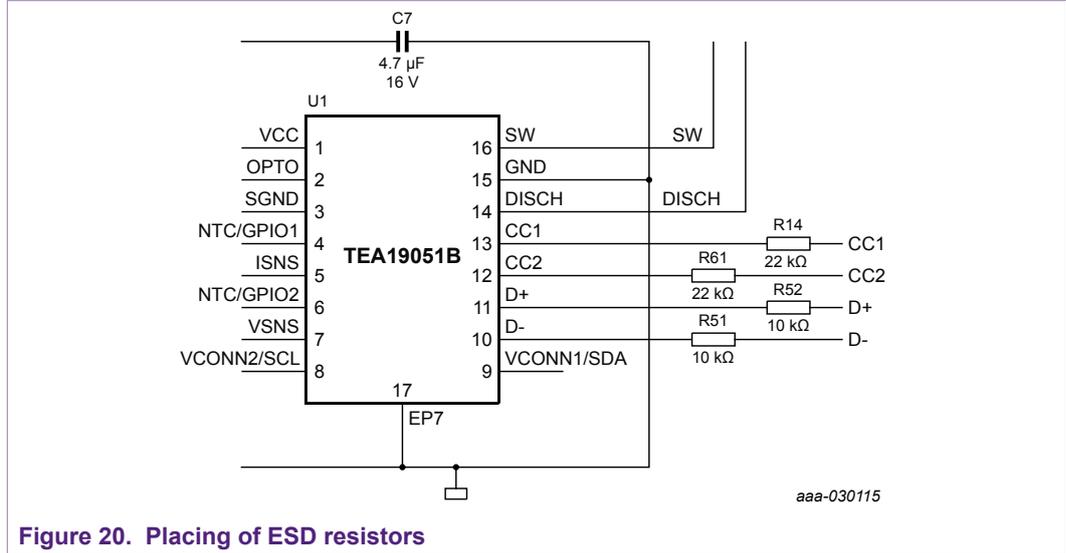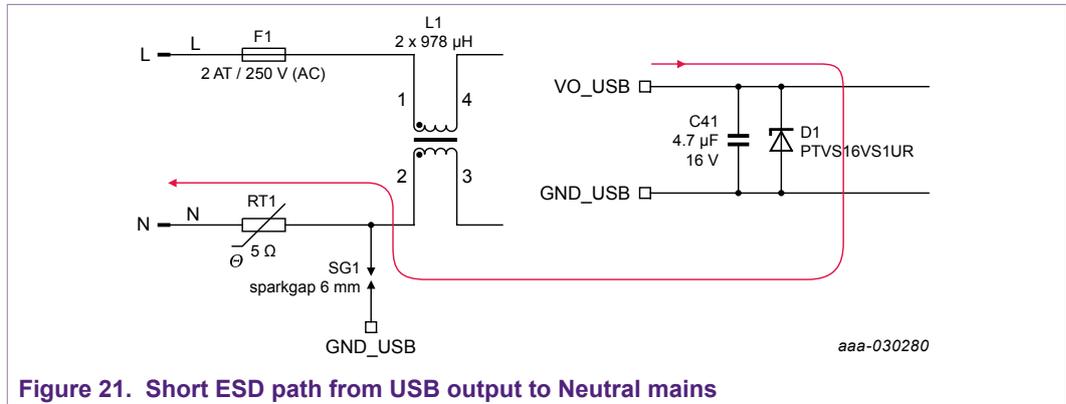

Figure 20. Placing of ESD resistors

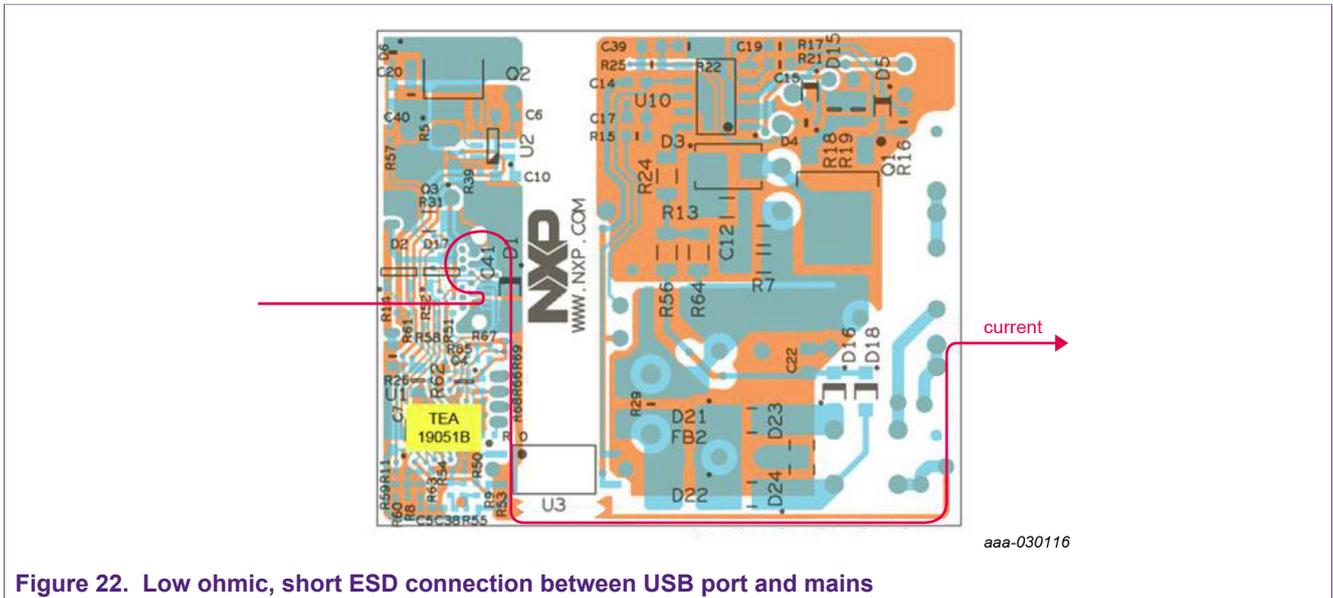
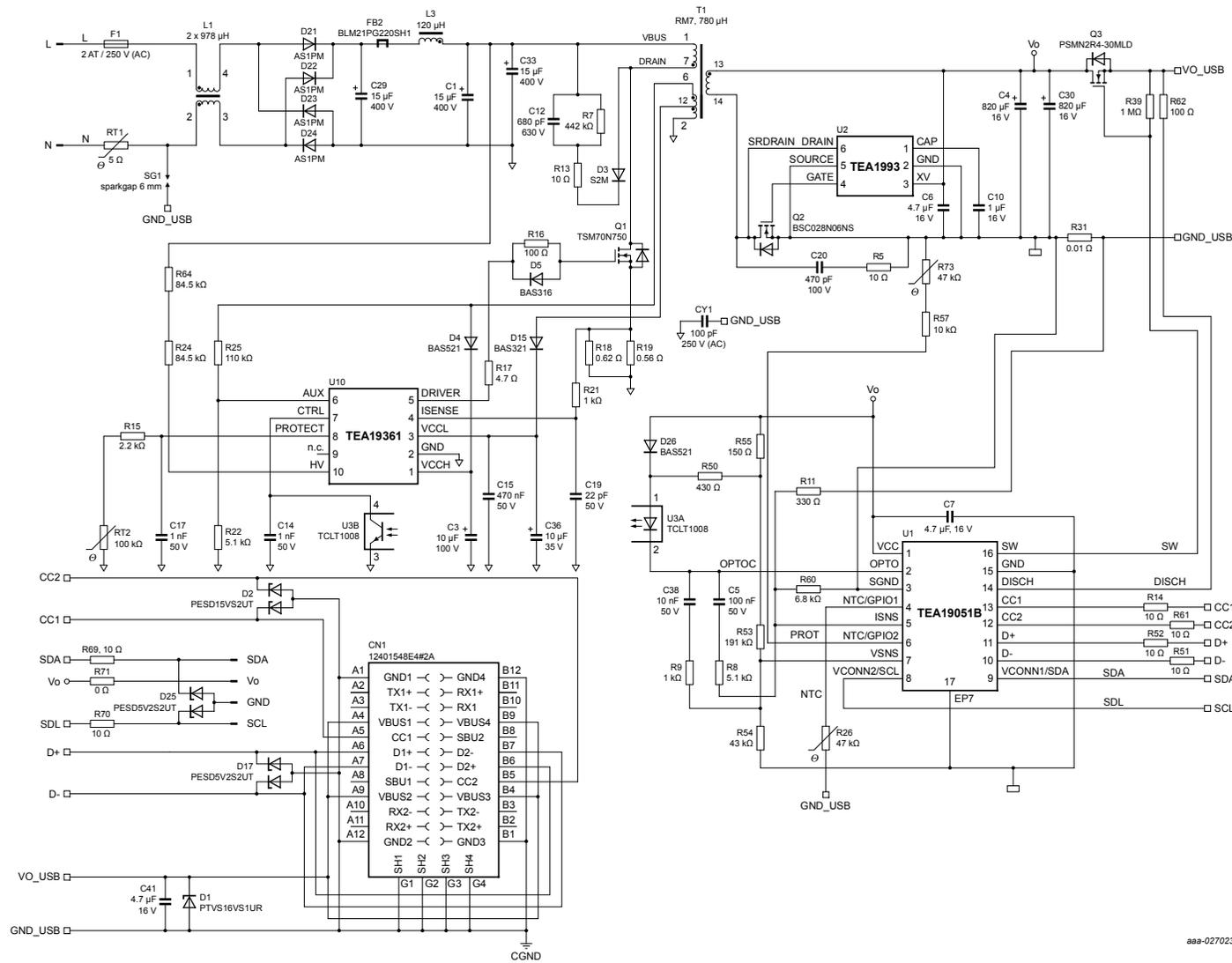**Figure 21. Short ESD path from USB output to Neutral mains**

aaa-030116

Figure 22. Low ohmic, short ESD connection between USB port and mains
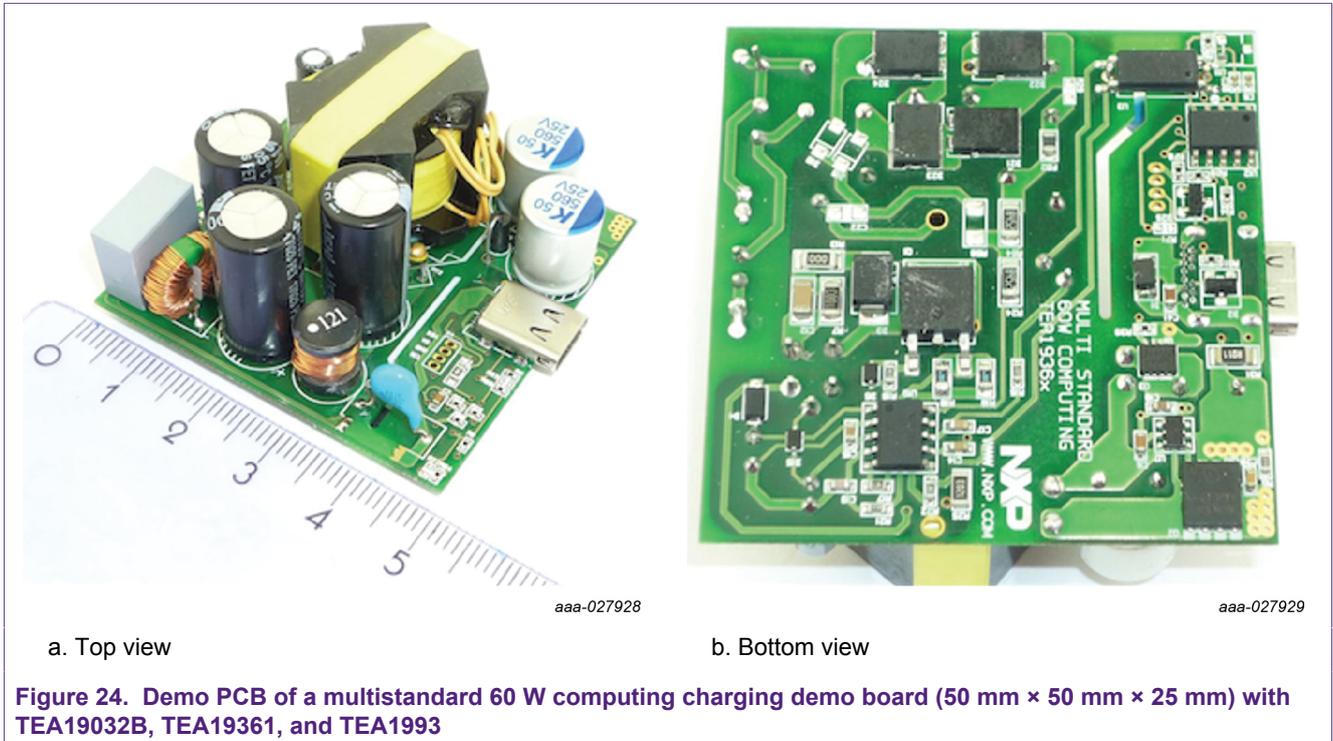
10 QC4+ 27 W demo design

Figure 23 shows the 27 W QC4+ reference design. More information on components, layout, performance etc. can be found in related user manual *"TEA1936xDB1475 multistandard 27 W HV mobile charging demo board"* (Ref. 8) on the NXP website. This website also shows more reference designs for e.g. 45 W and 60 W USB-PD/QC4 applications.

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Figure 23. TEA1936DB1475 27 W QC4+ reference design

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11 Demo Printed-Circuit Board (PCB)

aaa-027928

aaa-027929

a. Top view

b. Bottom view

Figure 24. Demo PCB of a multistandard 60 W computing charging demo board (50 mm × 50 mm × 25 mm) with TEA19032B, TEA19361, and TEA1993

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12 Abbreviations

Table 8. Abbreviations

Acronym	Description
BMC	Biphase Mark Code
CC-OVP	CC-lines OverVoltage Protections
CCCV	Constant-Current Constant-Voltage
CCM	Constant Current Mode
DFP	Down-stream Facing Port[1]
EOP	End Of Packet
NTC	Negative Temperature Coefficient
OCP	OverCurrent Protection
OSP	Output Short Protection
OSUP	Open_SUpply Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PDO	Power Data Object
SMPS	Switched-Mode Power Supply
SOP	Start Of Packet
UFP	Upstream Facing Port[2]
USB-PD	USB Power Delivery (Ref. 1)
UVLO	UnderVoltage LockOut
UVP	UnderVoltage Protection
vSafe0V	Safe operating voltage at 0 V[3]
vSafe5V	Safe operating at 5 V[4]

[1]   DFP indicates the position of the port in the USB topology, typically corresponding to a USB host root port or hub downstream port as defined in USB Type-C (Ref. 2).
[2]   UFP indicates the position of the port in the USB topology, typically a port on a device as defined in USB Type-C (Ref. 2).
[3]   0 V ≤ vSafe0V ≤ 0.8 V.
[4]   4.75 V ≤ vSafe5V ≤ 5.5 V.

13 References

[1]   **USB Power Delivery Specification** — Rev. 2.0, version 1.3; January 12, 2017

[2]   **USB Type-C Cable and ConnectorSpecification** — Revision 1.2; March 25, 2016 and ECNs

[3]   **TEA19032BT data sheet** — USB-PD 2.0/USB-PD 3.0/QC 4 controller for SMPS; 2018, NXP Semiconductors

[4]   **TEA19051BT data sheet** — USB-PD 2.0/USB-PD 3.0/QC 2.0/QC 3.0/QC 4 (+) controller for SMPS; 2018, NXP Semiconductors

[5]   **TEA193x data sheets** — GreenChip primary-side control IC; 2016/2017, NXP Semiconductors

[6]   **TEA199x data sheets** — GreenChip synchronous rectifier controller; 2016/2017, NXP Semiconductors

[7]   **TEA1396x application notes (AN11878; AN11879; AN11931)** — TEA1936x GreenChip SMPS control IC; 2017, NXP Semiconductors

[8]   **UM11048 user manual** — TEA1936xDB1475 multistandard 27 W HV mobile charging demo board; 2018, NXP Semiconductors

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