

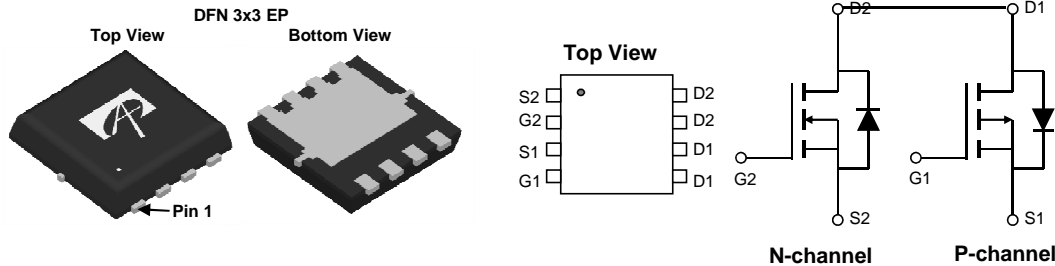
### General Description

The AON7611 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in inverter and other applications.

### Product Summary

N-channel	P-channel	
$V_{DS}$ (V) = 30V	$V_{DS}$ (V) = -30V	
$I_D$ = 9.0A	$I_D$ = -18.5A	( $V_{GS} = \pm 10V$ )
$R_{DS(ON)} < 50m\Omega$	$R_{DS(ON)} < 38m\Omega$	( $V_{GS} = \pm 10V$ )
$R_{DS(ON)} < 70m\Omega$	$R_{DS(ON)} < 62m\Omega$	( $V_{GS} = \pm 4.5V$ )

100% UIS Tested  
100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max N-channel	Max P-channel	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$	9	A
		$T_A=100^\circ\text{C}$	5.5	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	20	-35	A
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	$T_A=25^\circ\text{C}$	4	A
		$T_A=70^\circ\text{C}$	3	
Avalanche Current <sup>C</sup>	$I_{AR}$	7	-17	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	2	14	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_A=25^\circ\text{C}$	7	W
		$T_A=100^\circ\text{C}$	2.8	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	1.5	W
		$T_A=70^\circ\text{C}$	0.9	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics: N-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	70	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	15	18	$^\circ\text{C/W}$

### Thermal Characteristics: P-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	70	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	5	6	$^\circ\text{C/W}$

**N-channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.5	2	2.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	20			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =4A T <sub>J</sub> =125°C		40 64	50 80	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A		53	70	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =4A		11		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.79	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				9.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		170		pF
C <sub>oss</sub>	Output Capacitance			35		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			23		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.7	3.5	5.3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =4A		4.05	10	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			2	6	nC
Q <sub>gs</sub>	Gate Source Charge			0.55		nC
Q <sub>gd</sub>	Gate Drain Charge			1		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =3.75Ω, R <sub>GEN</sub> =3Ω		4.5		ns
t <sub>r</sub>	Turn-On Rise Time			1.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			18.5		ns
t <sub>f</sub>	Turn-Off Fall Time			15.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =4A, dI/dt=100A/μs		7.5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =4A, dI/dt=100A/μs		2.5		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

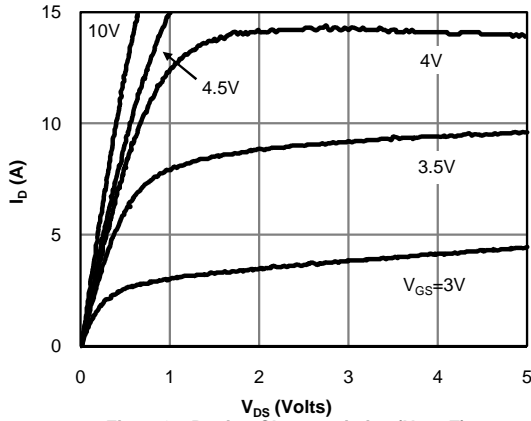
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C.

G. The maximum current rating is limited by bond-wires.

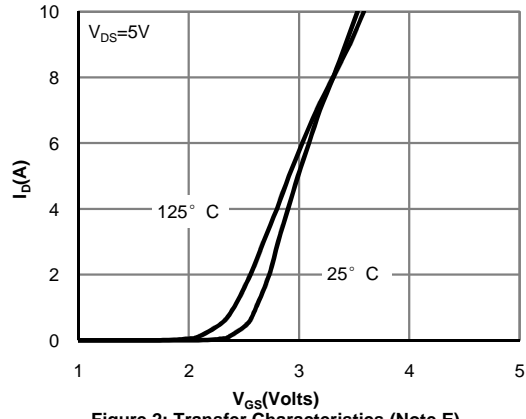
H. These tests are performed with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The SOA curve provides a single pulse rating.

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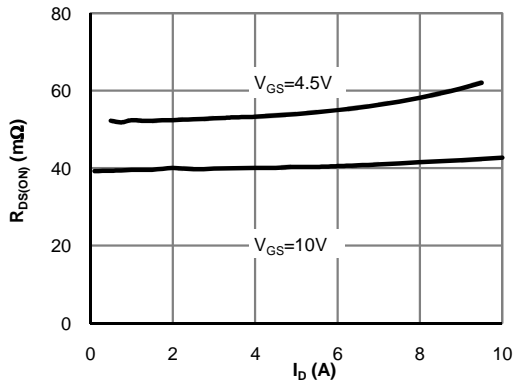
**N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



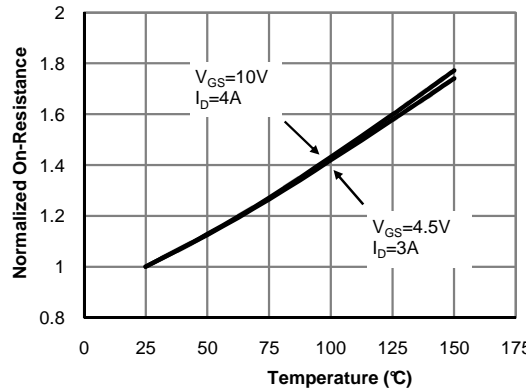
**Figure 1: On-Region Characteristics (Note E)**



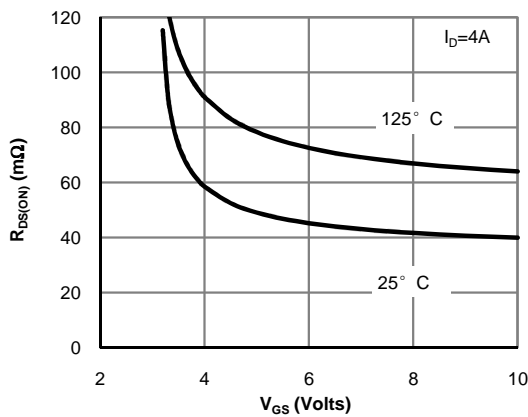
**Figure 2: Transfer Characteristics (Note E)**



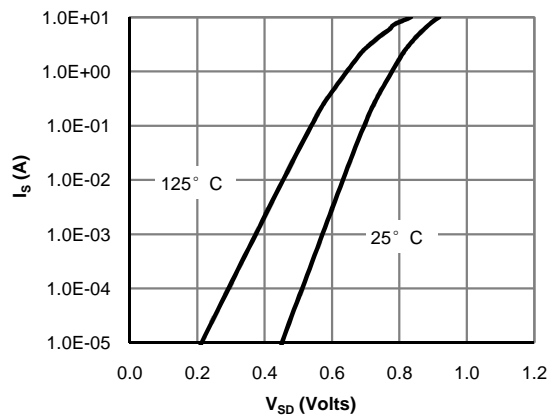
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

**N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

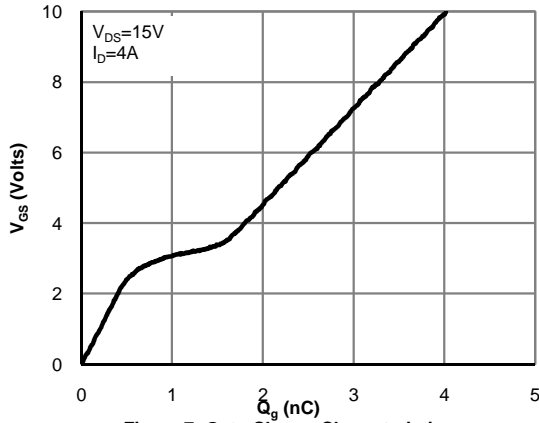


Figure 7: Gate-Charge Characteristics

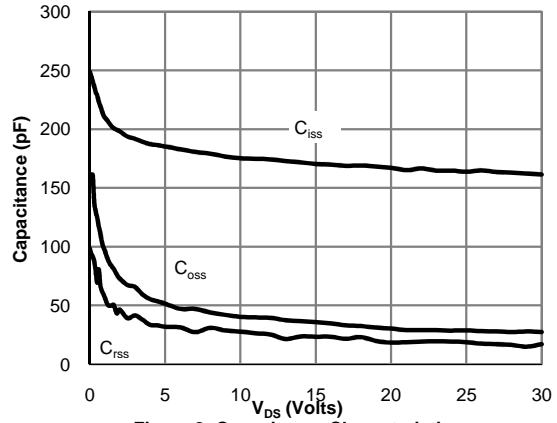


Figure 8: Capacitance Characteristics

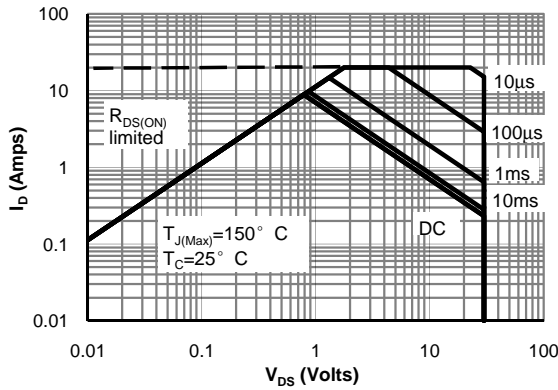


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

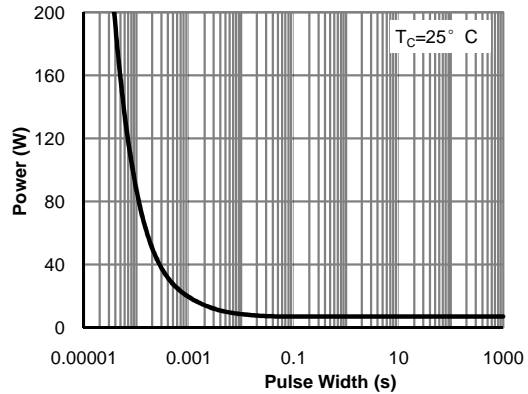


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

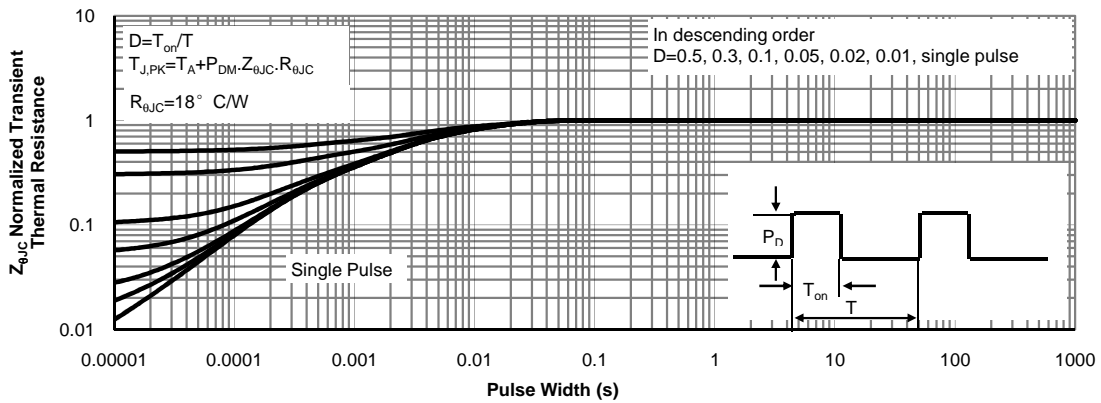


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

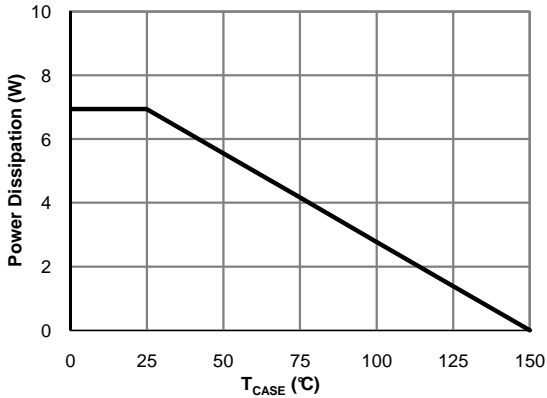


Figure 12: Power De-rating (Note F)

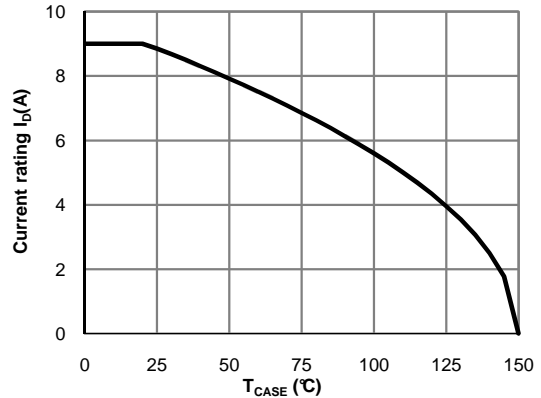


Figure 13: Current De-rating (Note F)

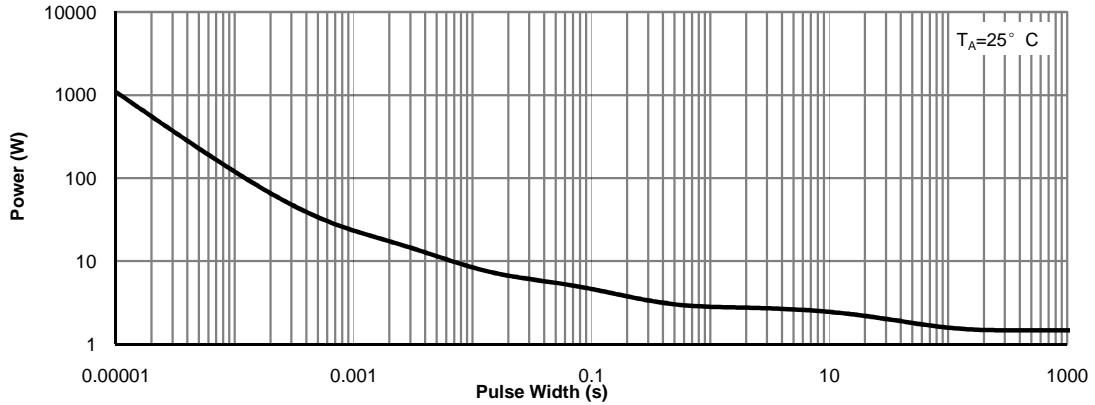


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

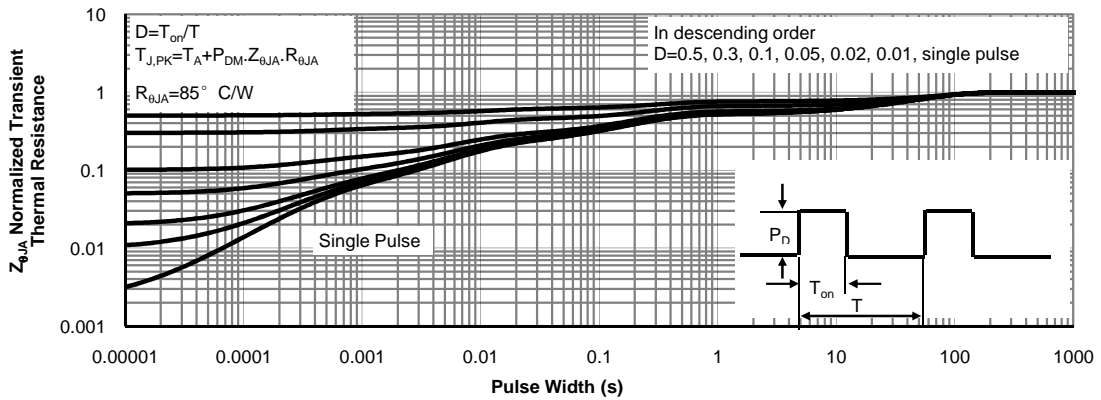
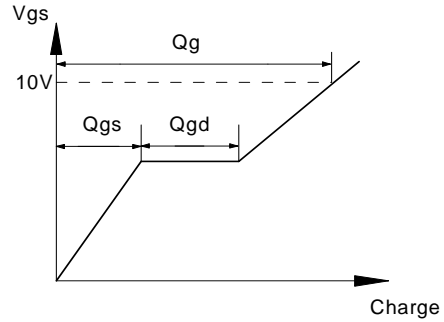
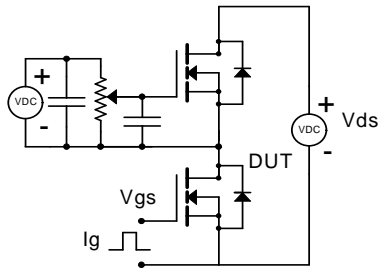
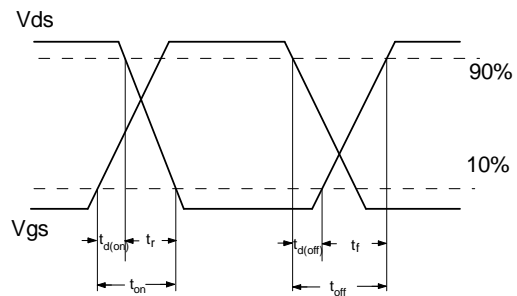
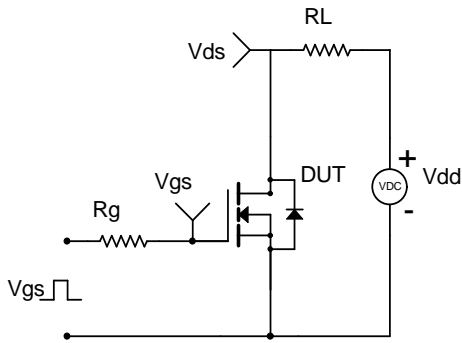


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

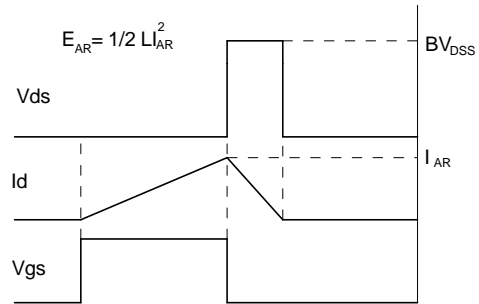
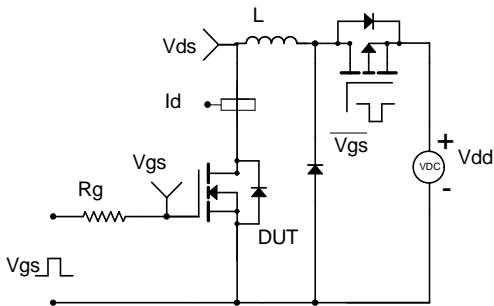
Gate Charge Test Circuit & Waveform



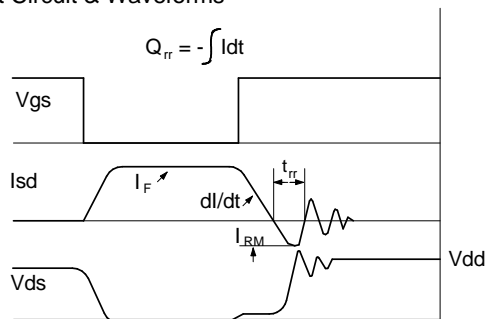
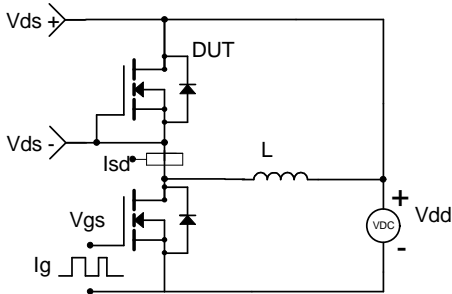
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



**P-channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.4	-1.9	-2.4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-35			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5A T <sub>J</sub> =125°C		30 45	38 57	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A		46	62	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-5A		10		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.76	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-20	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		520		pF
C <sub>oss</sub>	Output Capacitance			100		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			65		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	3.5	7.5	11.5	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-5A		9.2	20	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			4.6	10	nC
Q <sub>gs</sub>	Gate Source Charge			1.6		nC
Q <sub>gd</sub>	Gate Drain Charge			2.2		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =3.0Ω, R <sub>GEN</sub> =3Ω		7.5		ns
t <sub>r</sub>	Turn-On Rise Time			5.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			19		ns
t <sub>f</sub>	Turn-Off Fall Time			7		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-5A, di/dt=100A/μs		11		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-5A, di/dt=100A/μs		5.3		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

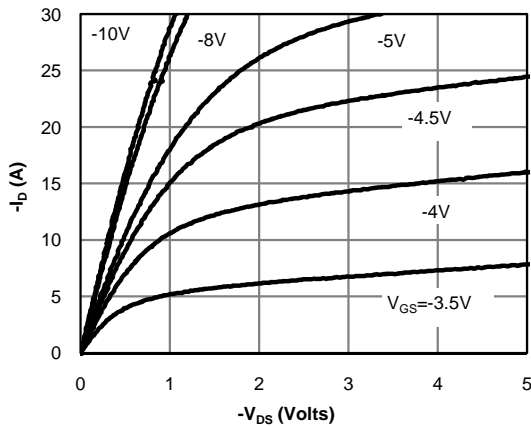
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C.

G. The maximum current rating is limited by bond-wires.

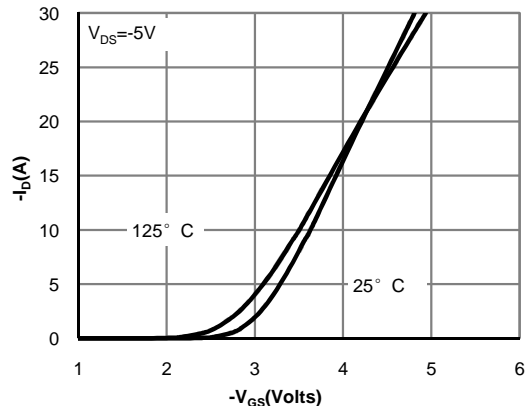
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The SOA curve provides a single pulse rating.

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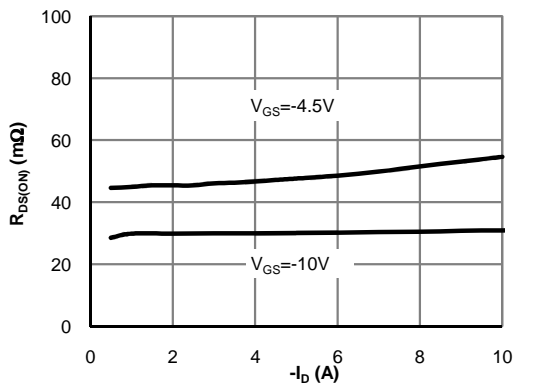
**P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



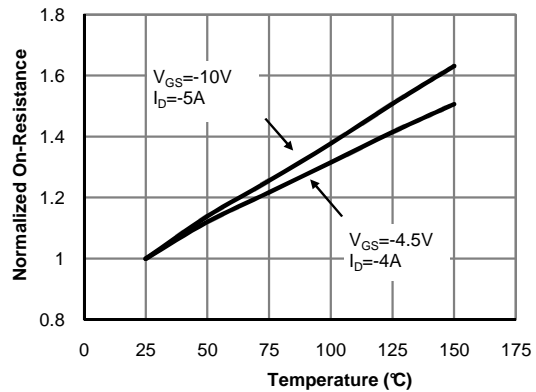
**Figure 1: On-Region Characteristics (Note E)**



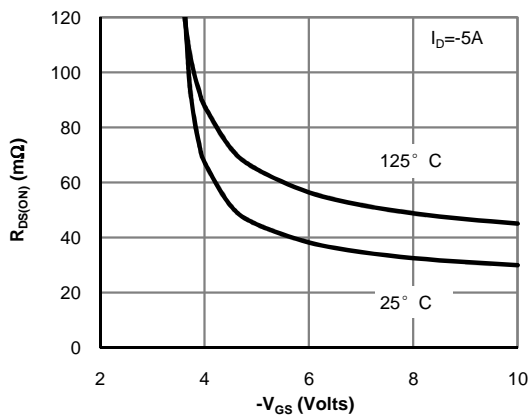
**Figure 2: Transfer Characteristics (Note E)**



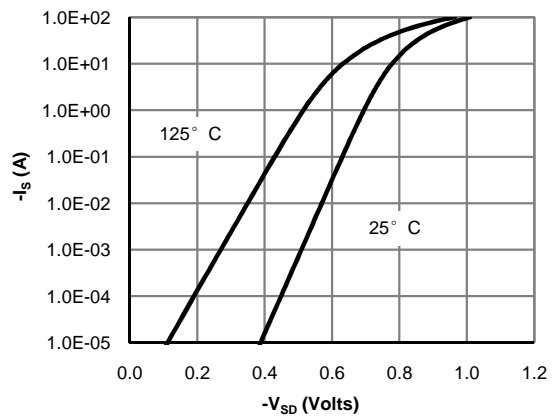
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



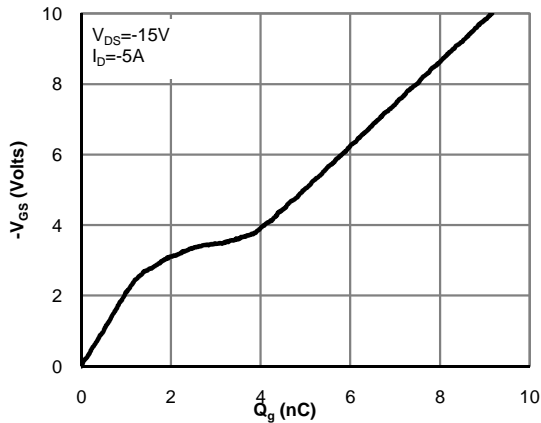
**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



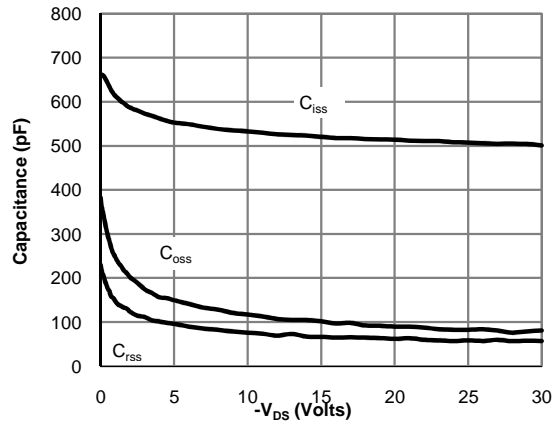
**Figure 6: Body-Diode Characteristics (Note E)**



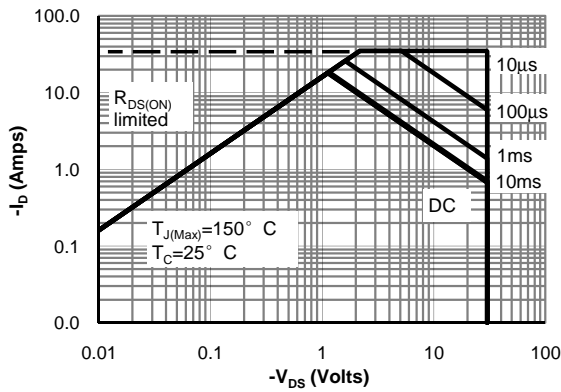
**P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



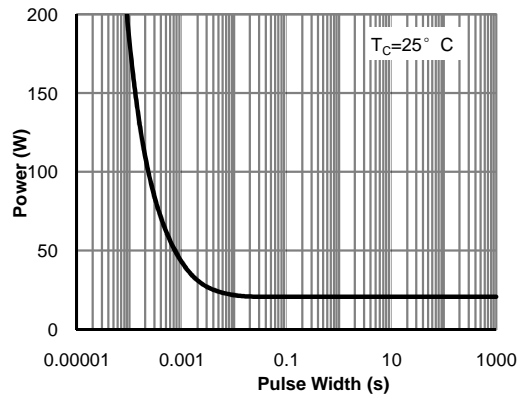
**Figure 7: Gate-Charge Characteristics**



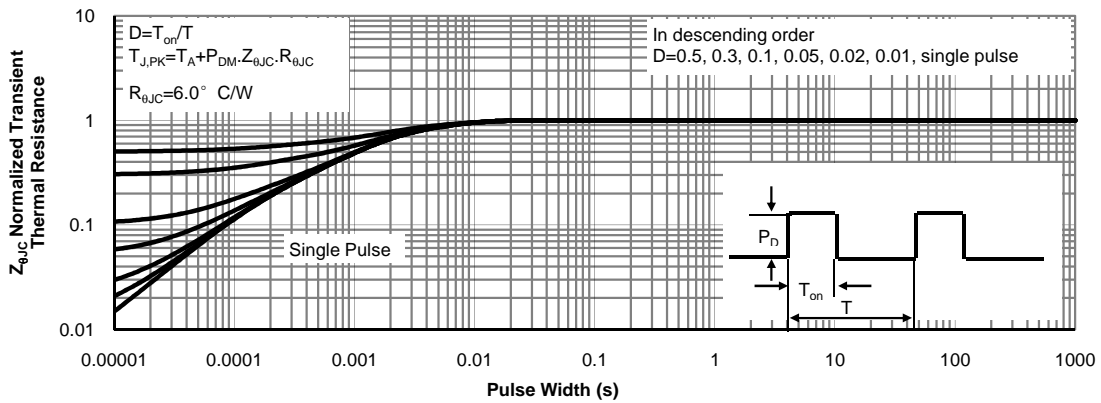
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

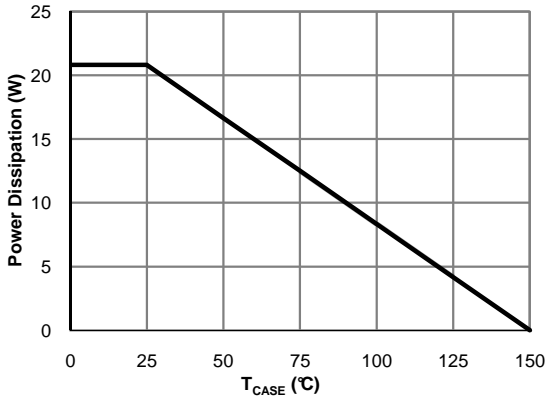


Figure 12: Power De-rating (Note F)

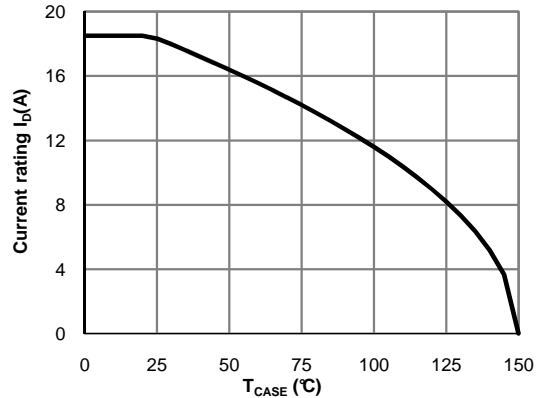


Figure 13: Current De-rating (Note F)

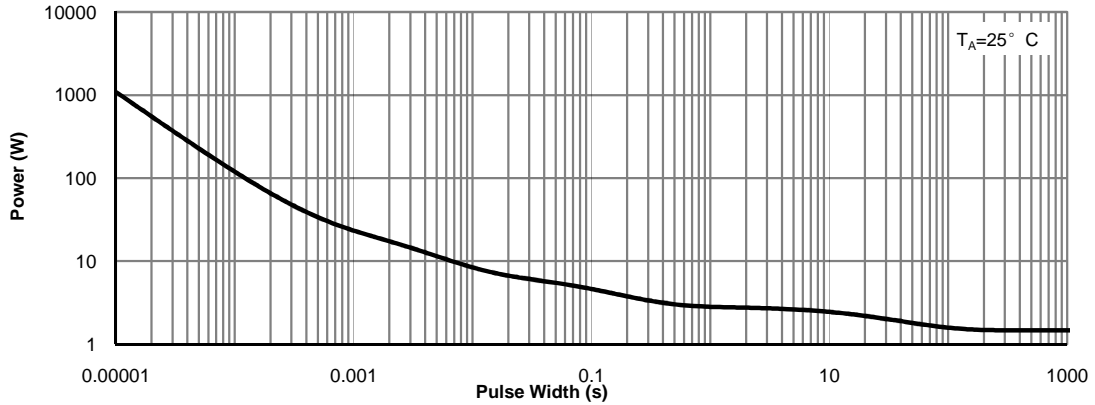


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

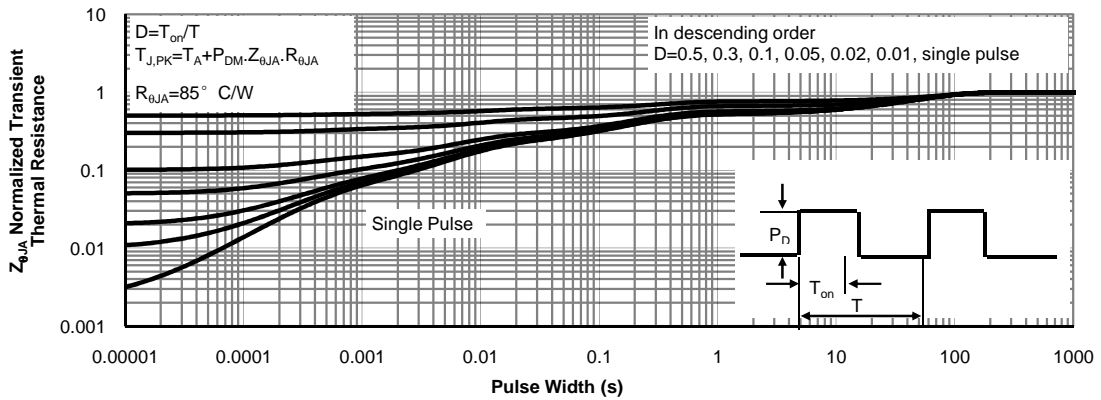
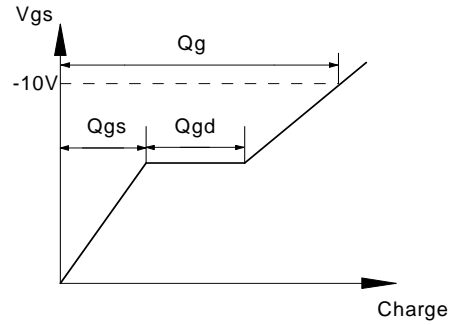
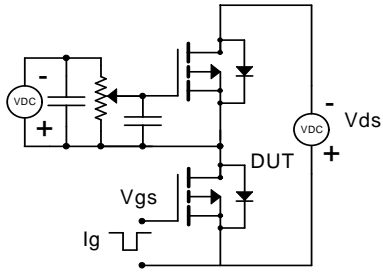
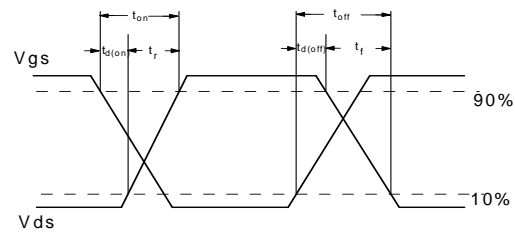
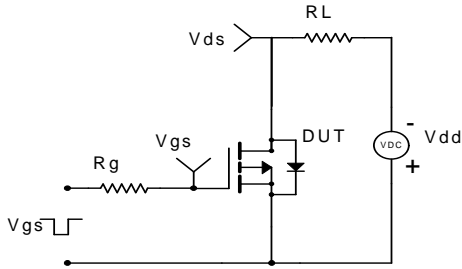


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

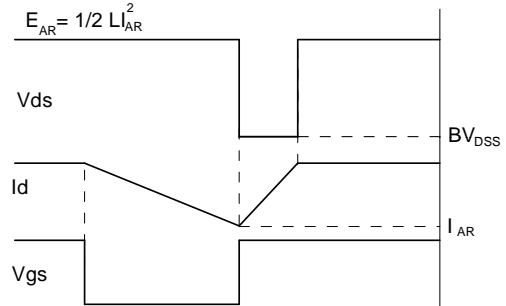
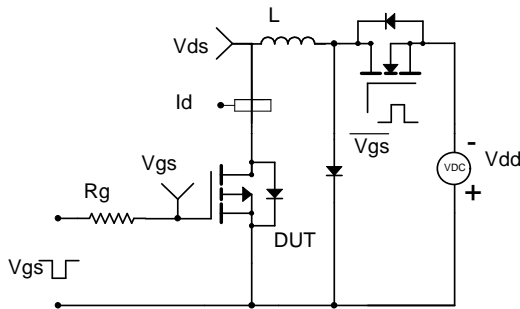
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**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

