True Zero-Speed, High Accuracy Gear Tooth Sensor IC

Features and Benefits

- Optimized robustness against magnetic offset variation
- Small signal lockout for immunity against vibration
- Tight duty cycle and timing accuracy over full operating temperature range
- True zero-speed operation
- Air gap independent switchpoints
- Large operating air gaps achieved through use of gain adjust and offset adjust circuitry
- Defined power-on state (POS)
- Wide operating voltage range
- Digital output representing target profile
- Single chip sensing IC for high reliability
- Small mechanical size
- Optimized Hall IC magnetic system
- Fast start-up
- Undervoltage lockout (UVLO)

Package: 4-pin SIP (suffix SG)

Not to scale

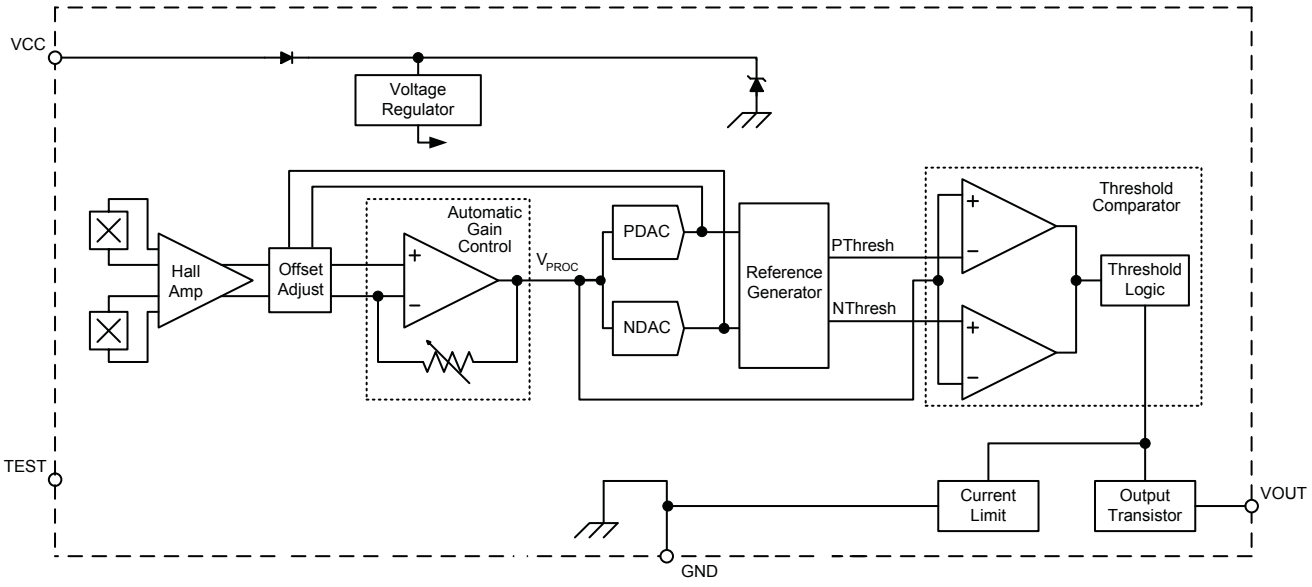
Description

The ATS667 is a true zero-speed gear tooth sensor IC consisting of an optimized Hall IC-rare earth pellet configuration in a single overmolded package. The unique IC and package design provides a user-friendly solution for digital gear tooth sensing applications. This small package can be easily assembled and used in conjunction with gears of various shapes and sizes.

The device incorporates a dual element Hall IC that switches in response to differential magnetic signals created by a ferro-magnetic target. The IC contains a sophisticated compensating circuit designed to eliminate the detrimental effects of magnet and system offsets. Digital processing of the analog signal provides zero-speed performance independent of air gap and also dynamic adaptation of device performance to the typical operating conditions found in automotive applications (reduced vibration sensitivity). High-resolution peak detecting DACs are used to set the adaptive switching thresholds of the device. Hysteresis in the thresholds reduces the negative effects of any anomalies in the magnetic signal associated with the targets used in many automotive applications.

The ATS667 is optimized for transmission applications. It is available in a lead (Pb) free 4-pin SIP package with a 100% matte tin plated leadframe.

Functional Block Diagram



Selection Guide

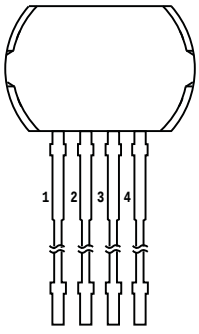
Part Number	Packing*
ATS667LSGTN-T	13-in. reel, 800 pieces/reel

*Contact Allegro™ for additional packing options

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	See Power Derating section	26.5	V
Reverse Supply Voltage	V_{RCC}		–18	V
Reverse Supply Current	I_{RCC}		–50	mA
Reverse Output Voltage	V_{ROUT}		–0.5	V
Output Sink Current	I_{OUT}		25	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-out Diagram



Terminal List

Number	Name	Function
1	VCC	Supply voltage
2	VOUT	Device output
3	TEST	Tie to GND or float
4	GND	Ground

OPERATING CHARACTERISTICS Valid over operating voltage and temperature ranges; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
Electrical Characteristics						
Supply Voltage[2]	V_{CC}	Operating, $T_J < T_J$(max)	4.0	–	24	V
Undervoltage Lockout (UVLO)	$V_{CC(UV)}$		–	3.5	3.95	V
Reverse Supply Current	I_{RCC}	V_{CC} = –18 V	–	–	– 10	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 15 mA, T_A = 25 °C	26.5	–	–	V
Supply Zener Current	I_Z	T_A = 25°C, $T_J < T_J$(max), continuous, V_Z = 26.5 V	–	–	15	mA
Supply Current	I_{CC}	Output off	4	7	12	mA
		Output on	4	7	12	mA
Power-On State Characteristics						
Power-On State	POS	Connected as in figure 6	–	High	–	–
Power-On Time[3]	t_{PO}	S_{ROT} < 200 rpm; $V_{CC} > V_{CC}$(min)	–	–	2	ms
OUTPUT STAGE						
Low Output Voltage	$V_{OUT(SAT)}$	I_{OUT} = 10 mA, Output = on	–	100	250	mV
Output Zener Clamp Voltage	V_{ZOUT}	I_{OUT} = 3 mA, T_A = 25°C	26.5	–	–	V
Output Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 12 V, $T_J < T_J$(max)	25	45	70	mA
Output Leakage Current	$I_{OUT(OFF)}$	Output = off, V_{OUT} = 24 V	–	–	10	µA
Output Rise Time	t_r	R_{PULLUP} = 1 kΩ, C_L = 4.7 nF, V_{PULLUP} = 12 V, 10% to 90%, connected as in figure 6	–	10	–	µs
Output Fall Time	t_f	R_{PULLUP} = 1 kΩ, C_L = 4.7 nF, V_{PULLUP} = 12 V, 90% to 10%, connected as in figure 6	–	0.6	2	µs
D-to- A Converter (DAC) Characteristics						
Allowable User Induced Differential Offset[4,5]	$B_{DIFFEXT}$	User induced differential offset	–	±60	–	G
Calibration						
Initial Calibration[6]	CAL_I	Possible reduced edge detection accuracy, duty cycle not guaranteed	–	1	6	edge
Update Method		Running mode operation, bounded for increasing AG, unlimited for decreasing AG	–	Continuous	–	–
Operating Characteristics (with Allegro 60-0 Reference Target)						
Operational Air Gap Range[7]	AG_{OP}	Repeatability and duty cycle within specification	0.5	–	2.5	mm
Maximum Operational Air Gap Range	AG_{OPMAX}	Output switching only (no missing edges)	–	–	3.1	mm
Relative Repeatability[8]	$T_{\theta E}$	100 G_{pk-pk} ideal sinusoidal signal, T_A = 150°C, S_{ROT} = 1000 rpm (f = 1000 Hz)	–	0.06	–	deg.
Maximum Single Outward Sudden Air Gap Change[9]	ΔAG_{MAX}	Percentage of most recent AG_{pk-pk}, single instantaneous air gap increase, f < 500 Hz, $V_{PROC(pk-pk)} > V_{LOE}$ after sudden AG change	–	40	–	%
Duty Cycle	D	Measured as V_{OUT}, connected as in figure 6; Wobble < 0.5 mm, $AG_{OP} < AG_{OP}$(max), direction of target rotation pin 4 to pin 1	42	47	52	%

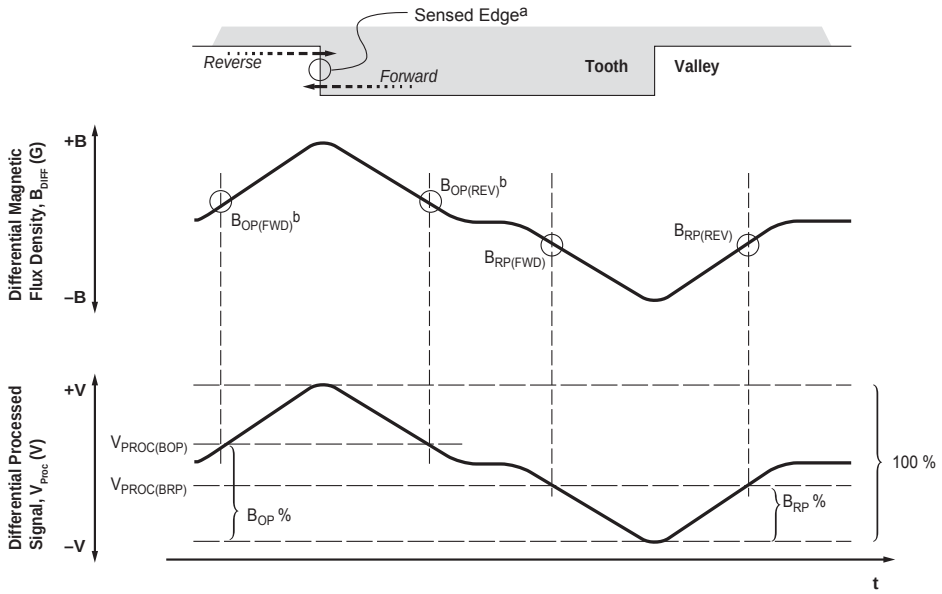
Continued on the next page…

OPERATING CHARACTERISTICS (continued) Valid over operating voltage and temperature ranges; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
Switchpoint Characteristics						
Operational Speed	S_{ROT}	Allegro 60–0 Reference Target	0	–	12000	rpm
Bandwidth	f_{-3dB}	Cutoff frequency for low-pass filter	15	20	–	kHz
Operate Point	B_{OP}	% of peak-to-peak V_{PROC} referenced from PDAC to NDAC, AG < AG_{max}, V_{OUT} high to low	–	70	–	%
Release Point	B_{RP}	% of peak-to-peak V_{PROC} referenced from PDAC to NDAC, AG < AG_{max} , V_{OUT} low to high	–	30	–	%
Running Mode Lockout Enable (LOE)	$V_{LOE(RM)}$	$V_{PROC(PK-PK)}$ < $V_{LOE(RM)}$ = output switching disabled	–	100	–	mV
Running Mode Lockout Release (LOR)	$V_{LOR(RM)}$	$V_{PROC(PK-PK)}$ < $V_{LOR(RM)}$ = output switching enabled	–	220	–	mV

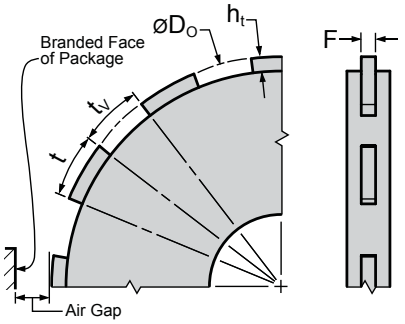
[1]Typical data is at V_{CC} = 12 V and T_A = 25°C, unless otherwise noted. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see Power Derating section.
[3] Power-On Time is the time required to complete the internal Automatic Offset Adjust; the DACs are then ready for peak acquisition.
[4]1 G (gauss) = 0.1 mT (millitesla).
[5]The device compensates for magnetic and installation offsets. Offsets greater than specification in gauss may cause inaccuracies in the output.
[6]For power-on S_{ROT} ≤ 200 rpm, edges are sensed target mechanical edges (see figure Definitions of Terms for Switchpoints).
[7]Operational Air Gap Range is dependent on the available magnetic field. The available field is target geometry and material dependent and should be independently characterized. The field available from the Allegro 60-0 reference target is given in the reference target parameter section.
[8]The repeatability specification is based on statistical evaluation of a sample population, evaluated at 1000 Hz. Repeatability is measured at 150°C because the lowest signal-to-noise ratio for the V_{PROC} signal occurs at elevated temperatures. Therefore, the worst-case repeatability for the device will also occur at elevated temperatures.
[9]Single maximum allowable air gap change in outward direction (increase in air gap).

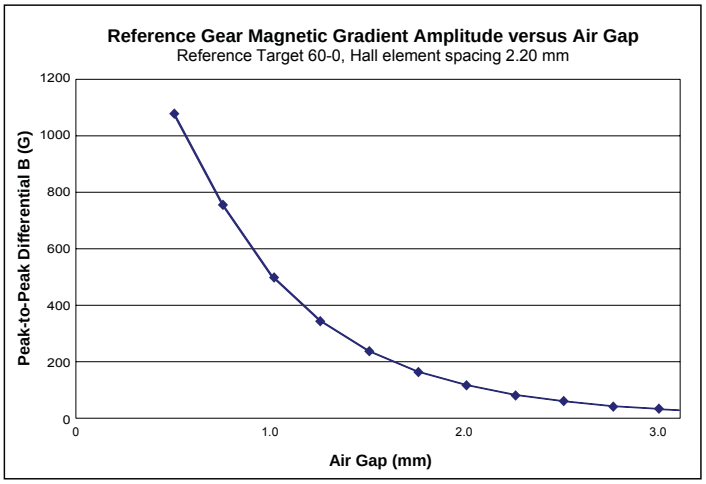
Definitions of Terms for Switchpoints

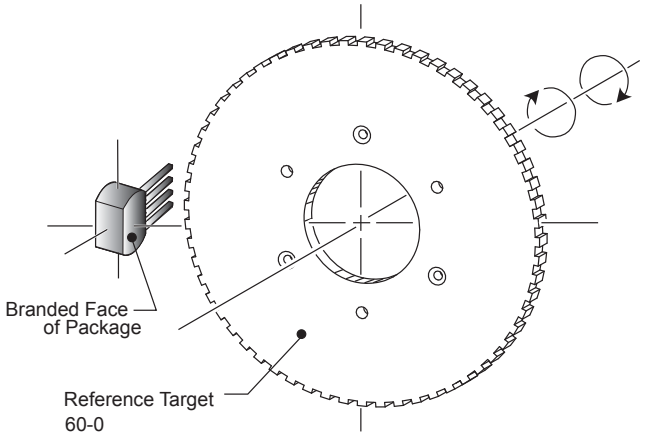


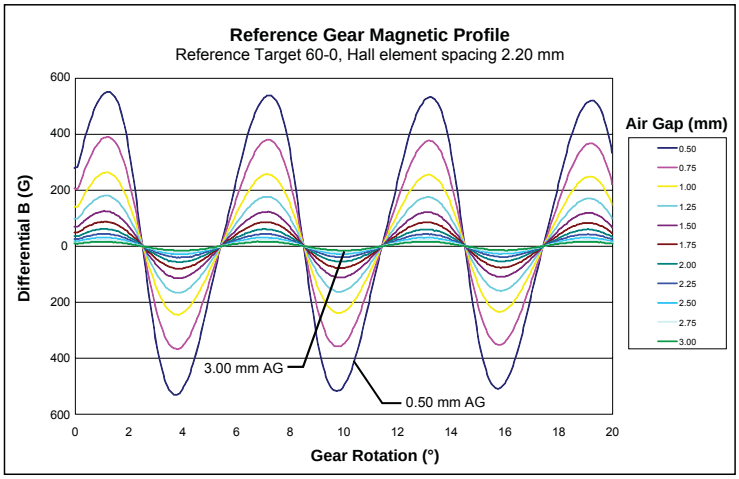
[a]Sensed Edge: leading (rising) mechanical edge in forward rotation, trailing (falling) mechanical edge in reverse rotation
[b]$B_{OP(FWD)}$ triggers the output transition during forward rotation, and $B_{OP(REV)}$ triggers the output transition during reverse rotation

Reference Target 60-0 (60 Tooth Target)

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Angular Tooth Thickness	t	Length of tooth, with respect to branded face	3	deg.	
Angular Valley Thickness	t_v	Length of valley, with respect to branded face	3	deg.	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	

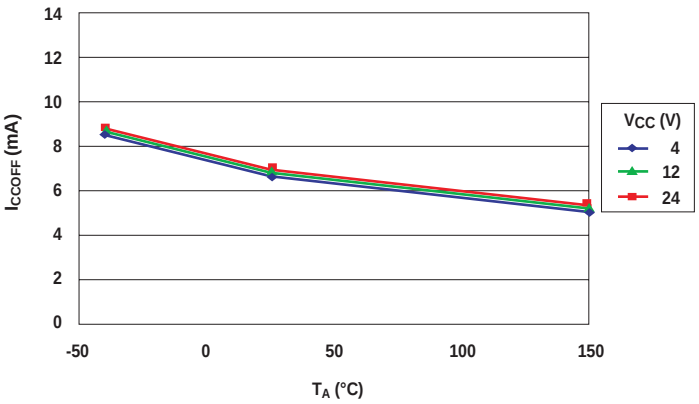




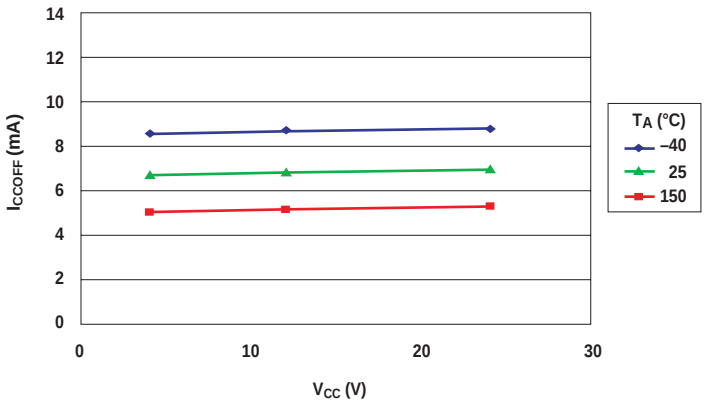


Characteristic Performance

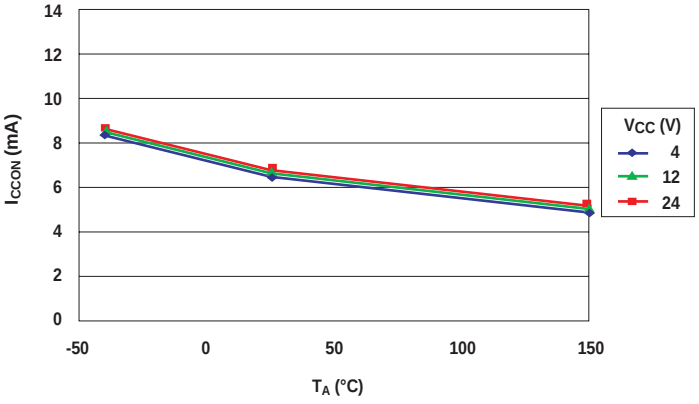
Supply Current (Off) versus Ambient Temperature



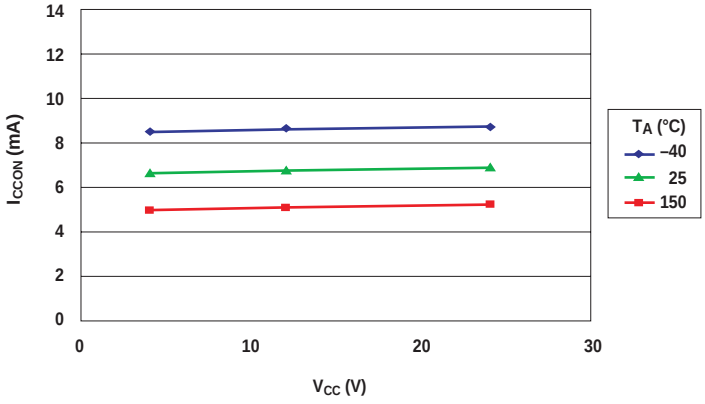
Supply Current (Off) versus Supply Voltage



Supply Current (On) versus Ambient Temperature

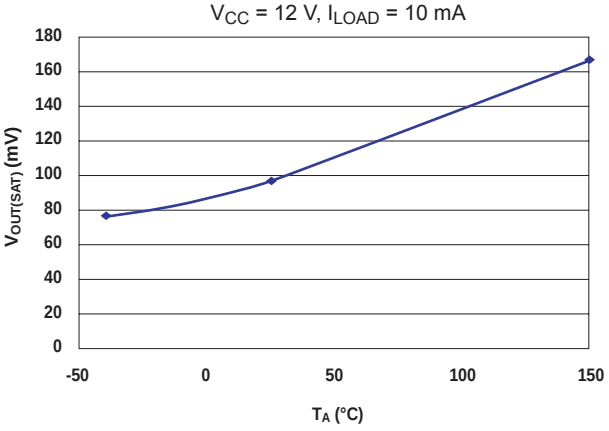


Supply Current (On) versus Supply Voltage



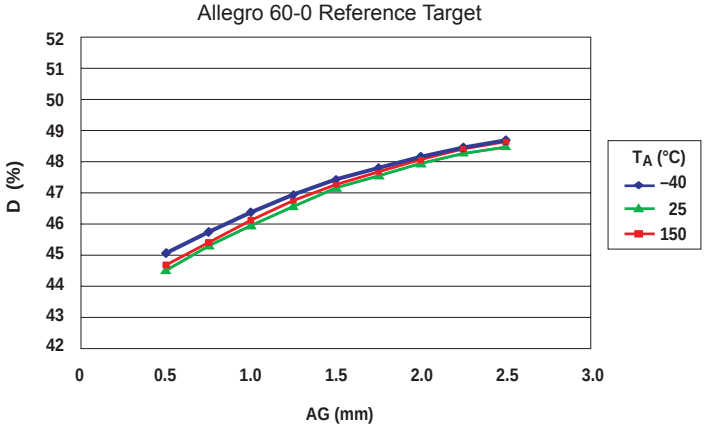
Output Voltage versus Ambient Temperature

V_{CC} = 12 V, I_{LOAD} = 10 mA



Duty Cycle versus Air Gap

Allegro 60-0 Reference Target

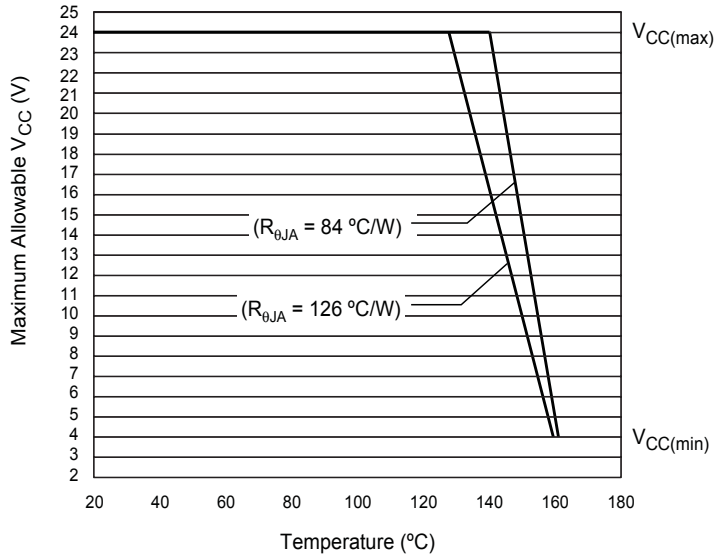


THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

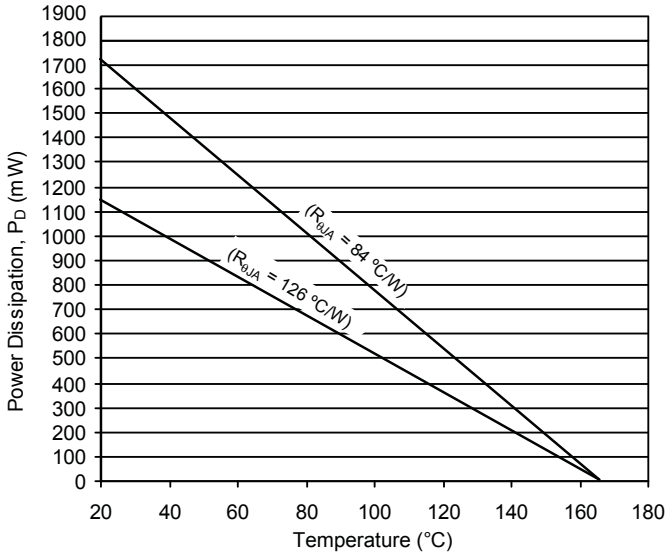
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Single-sided PCB with copper limited to solder pads	126	°C/W
		Two-sided PCB with copper limited to solder pads and 3.57 in.^{2} (23.03 cm^2) of copper area each side, connected to GND pin	84	°C/W

*Additional information is available on the Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



Functional Description

Hall Technology

The ATS667 contains a single-chip differential Hall-effect sensor IC, a samarium cobalt pellet, and a flat ferrous pole piece (concentrator). As shown in figure 1, the Hall IC supports two Hall elements, which sense the magnetic profile of the ferrous gear target simultaneously, but at different points (spaced at a 2.2 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset compensation circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling During Operation

An operating device is capable of providing digital information that is representative of the mechanical features of a rotating gear. The waveform diagram in figure 3 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the ATS667. No additional optimization is needed and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

Determining Output Signal Polarity

In figure 3, the top panel, labeled Mechanical Position, represents the mechanical features of the target gear and orientation to the device. The bottom panel, labeled IC Output Signal, displays the square waveform corresponding to the digital output signal that results from a rotating gear configured as shown in figure 2, and electrically connected as in figure 6. That direction of rotation (of the gear side adjacent to the package face) is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 4 side. This results in the IC output switching from low state to high state as the leading edge of a tooth (a rising mechanical edge, as detected by the IC) passes the package face. In this configuration, the device output switches to its high polarity when a tooth is the target feature nearest to the package. If the direction of rotation is reversed, so that the gear rotates from the pin 4 side to the pin 1 side, then the output polarity inverts. That is, the output signal goes high when a falling edge is detected, and a valley is nearest to the package.

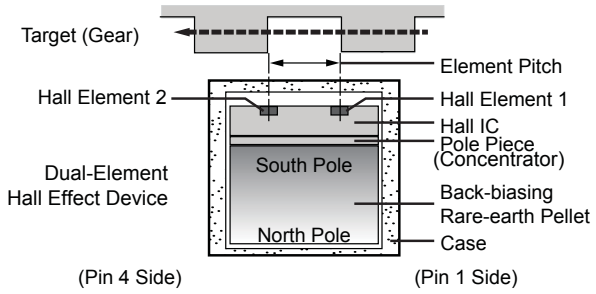


Figure 1. Relative motion of the target is detected by the dual Hall elements mounted on the Hall IC.

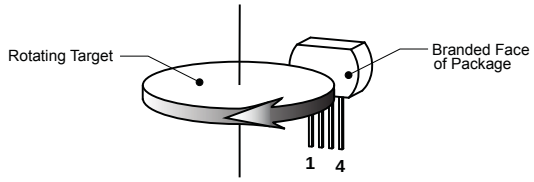


Figure 2. This left-to-right (pin 1 to pin 4) direction of target rotation results in a high output state when a tooth of the target gear is nearest the package face (see figure 3). A right-to-left (pin 4 to pin 1) rotation inverts the output signal polarity.

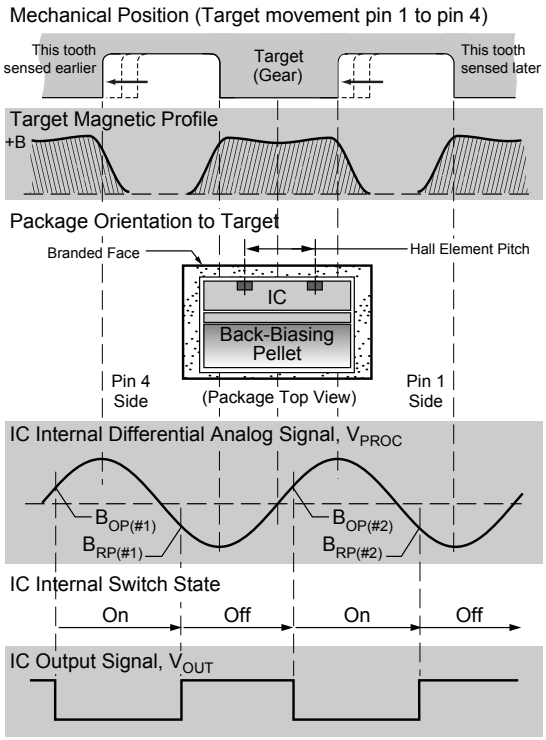
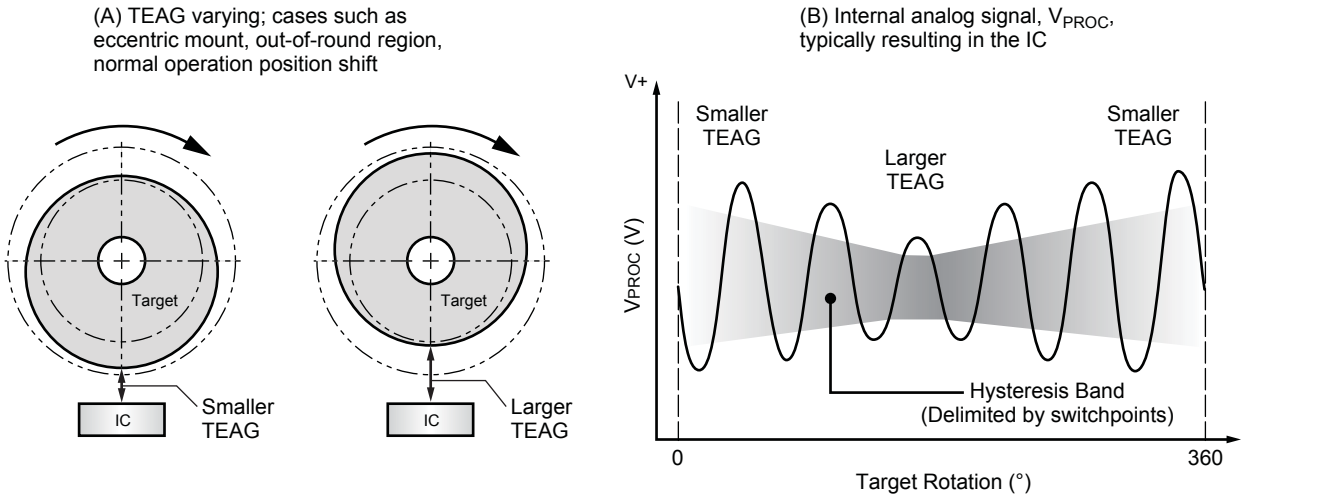


Figure 3. The magnetic profile reflects the geometry of the target, allowing the ATS667 to present an accurate digital output response.

Continuous Update of Switchpoints

Switchpoints are the threshold levels of the differential internal analog signal, V_{PROC}, at which the device changes output signal state. The value of V_{PROC} is directly proportional to the magnetic flux density, B, induced by the target and sensed by the Hall elements. As V_{PROC} rises through a certain limit, referred to as the operate point, B_{OP}, the output state changes from high to low. As V_{PROC} falls below B_{OP} to a certain limit, the release point, B_{RP}, the output state changes from low to high.

As shown in panel C of figure 4, threshold levels for the ATS667 switchpoints are established as a function of the peak input signal levels. The ATS667 incorporates an algorithm that continuously monitors the input signal and updates the switching thresholds accordingly with limited inward movement of V_{PROC}. The switchpoint for each edge is determined by the detection of the previous two signal edges. In this manner, variations are tracked in real time.



(C) Referencing the internal analog signal, V_{PROC}, to continuously update device response

B_{HYS}	Switchpoint	Determinant Peak Values
1	$B_{OP(\#1)}$ $B_{RP(\#1)}$	$Pk_{(\#1)}$, $Pk_{(\#2)}$ $Pk_{(\#2)}$, $Pk_{(\#3)}$
2	$B_{OP(\#2)}$ $B_{RP(\#2)}$	$Pk_{(\#3)}$, $Pk_{(\#4)}$ $Pk_{(\#4)}$, $Pk_{(\#5)}$
3	$B_{OP(\#3)}$ $B_{RP(\#3)}$	$Pk_{(\#5)}$, $Pk_{(\#6)}$ $Pk_{(\#6)}$, $Pk_{(\#7)}$
4	$B_{OP(\#4)}$ $B_{RP(\#4)}$	$Pk_{(\#7)}$, $Pk_{(\#8)}$ $Pk_{(\#8)}$, $Pk_{(\#9)}$

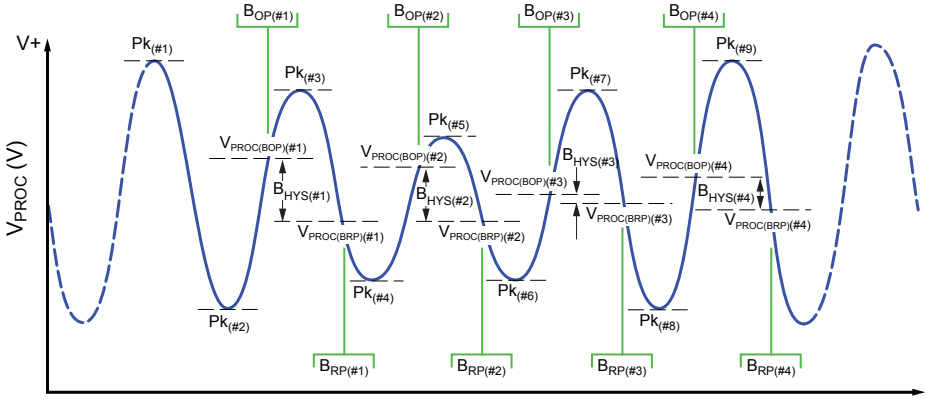


Figure 4. The Continuous Update algorithm allows the Allegro IC to interpret and adapt to variances in the magnetic field generated by the target as a result of eccentric mounting of the target, out-of-round target shape, and similar dynamic application problems that affect the TEAG (Total Effective Air Gap). Not detailed in the figure are the boundaries for peak capture DAC movement which intentionally limit the amount of inward signal variation the IC is able to react to over a single transition. The algorithm is used to establish and subsequently update the device switchpoints (B_{OP} and B_{RP}). The hysteresis, $B_{HYS(\#x)}$, at each target feature configuration results from this recalibration, ensuring that it remains properly proportioned and centered within the peak-to-peak range of the internal analog signal, V_{PROC}.
As shown in panel A, the variance in the target position results in a change in the TEAG. This affects the IC as a varying magnetic field, which results in proportional changes in the internal analog signal, V_{PROC}, shown in panel B. The Continuous Update algorithm is used to establish switchpoints based on the fluctuation of V_{PROC}, as shown in panel C.

Start Mode Hysteresis

This feature helps to ensure optimal self-calibration by rejecting electrical noise and low-amplitude target vibration during initialization. This prevents AGC from calibrating the IC on such spurious signals. Calibration can be performed using the actual target features.

A typical scenario is shown in figure 5. The Start Mode Hysteresis, PO_{HYS}, is a minimum level of the peak-to-peak amplitude of the internal analog electrical signal, V_{PROC}, that must be exceeded before the ATS667 starts to compute switchpoints.

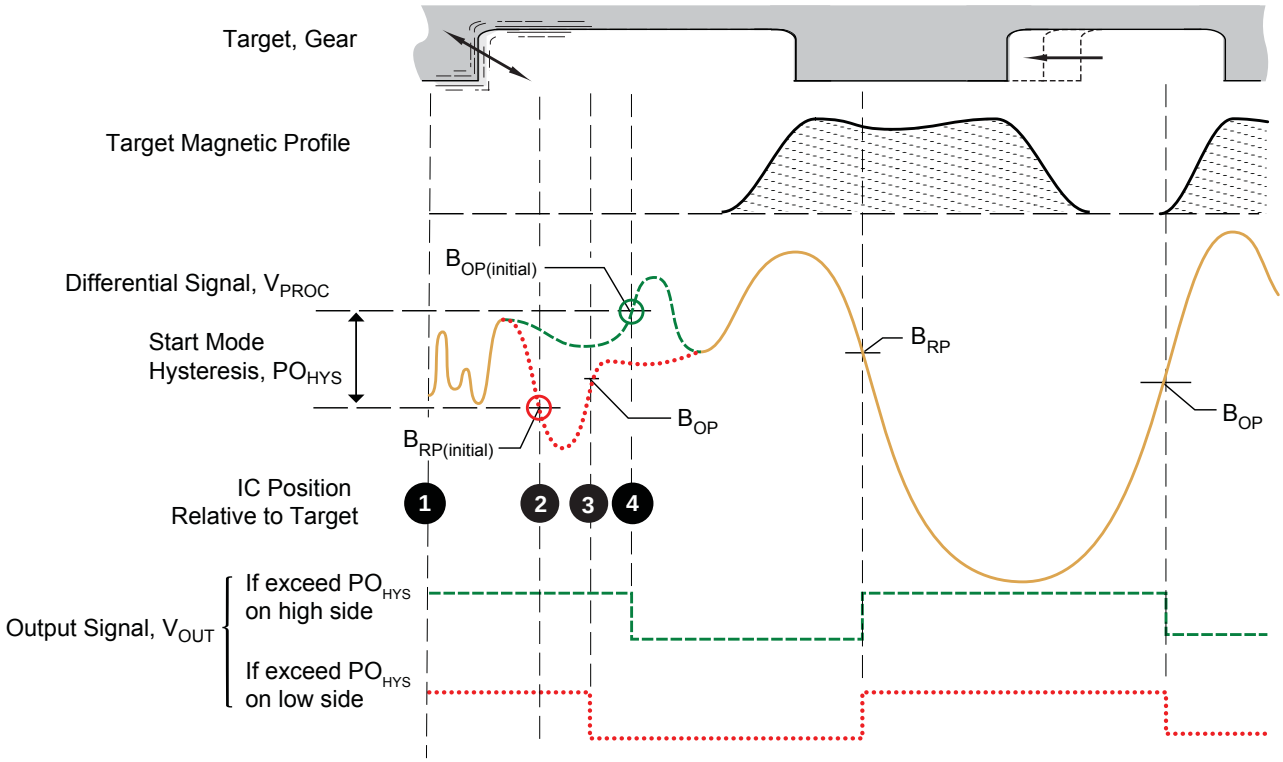


Figure 5. Operation of Start Mode Hysteresis

- At power-on (position 1), the ATS667 begins sampling V_{PROC}.
- At the point where the Start Mode Hysteresis, PO_{HYS}, is exceeded, the device establishes an initial switching threshold, by using the Continuous Update algorithm. If V_{PROC} is falling through the limit on the low side (position 2), the switchpoint is B_{RP}, and if V_{PROC} is rising through the limit on the high side (position 4), it is B_{OP}. After this point, Start Mode Hysteresis is no longer a consideration. Note that a valid V_{PROC} value exceeding the Start Mode Hysteresis can be generated either by a legitimate target feature or by excessive vibration.
- In either case, because the switchpoint is immediately passed as soon as it is established, the ATS667 enables switching:
  --If on the low side, at B_{RP} (position 2) the output would switch from low to high. However, because output is already high, no output switching occurs. At the next switchpoint, where B_{OP} is passed (position 3), the output switches from high to low.
  --If on the high side, at B_{OP} (position 4) the output switches from high to low.

As this example demonstrates, initial output switching occurs with the same polarity, regardless of whether the Start Mode Hysteresis is exceeded on the high side or on the low side.

Undervoltage Lockout

When the supply voltage falls below the undervoltage lockout voltage, $V_{CC(UV)}$, the device enters Reset, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied. I_{CC} levels may not meet datasheet limits when $V_{CC} < V_{CC}(min)$. This lockout feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the IC.

Power Supply Protection

The device contains an on-chip regulator and can operate over a wide V_{CC} range. For devices that must operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro for information on the circuitry needed for compliance with various EMC specifications. Refer to figure 6 for an example of a basic application circuit.

Automatic Gain Control (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). At power-on, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain of the IC is then automatically adjusted. Figure 7 illustrates the effect of this feature.

Automatic Offset Adjust (AOA)

The AOA circuitry automatically compensates for the effects of chip, magnet, and installation offsets. This circuitry is continuously active, including during both power-on mode and running mode, compensating for any offset drift (within the Allowable User Induced Differential Offset). Continuous operation also allows it to compensate for offsets induced by temperature variations over time.

Running Mode Lockout

The ATS667 has a running mode lockout feature to prevent switching in response to small signals that are characteristic of vibration signals. The internal logic of the chip considers small signal amplitudes below a certain level to be vibration. The output is held to the state prior to lockout until the amplitude of the signal returns to normal operational levels.

Assembly Description

The ATS667 is integrally molded into a plastic body that has been optimized for size, ease of assembly, and manufacturability. High operating temperature materials are used in all aspects of construction.

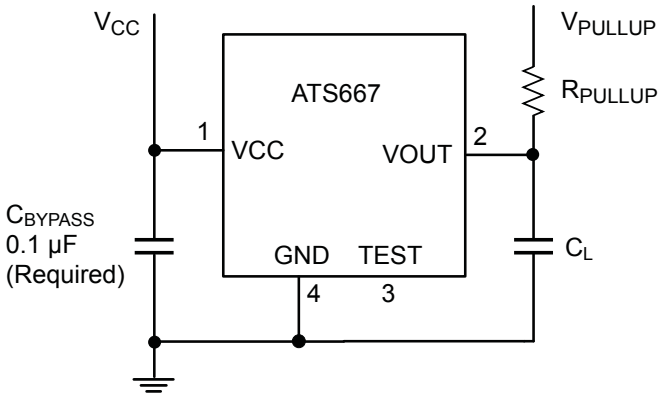


Figure 6. Typical circuit for proper device operation.

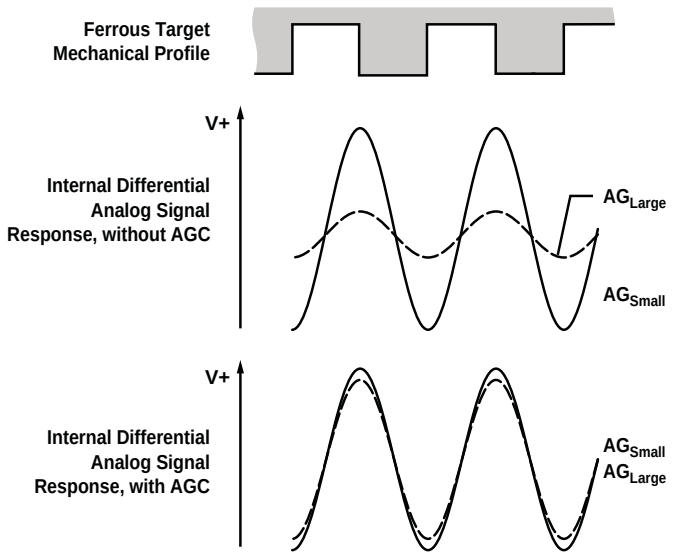


Figure 7. Automatic Gain Control (AGC). The AGC function corrects for variances in the air gap. Differences in the air gap cause differences in the magnetic field at the device, but AGC prevents that from affecting device performance, as shown in the lowest panel.

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 7.5 mA, and $R_{\theta JA}$ = 126 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 7.5\ mA = 90\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 90\ mW \times 126\ °C/W = 11.3°C$$

$$T_J = T_A + \Delta T = 25°C + 11.3°C = 36.3°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level ($V_{CC}(max)$, $I_{CC}(max)$), without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package SG, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=126 °C/W, $T_J(max)$=165°C, $V_{CC}(max)$ =24 V, and $I_{CC}(max)$ = 12 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 126\ °C/W = 119\ mW$$

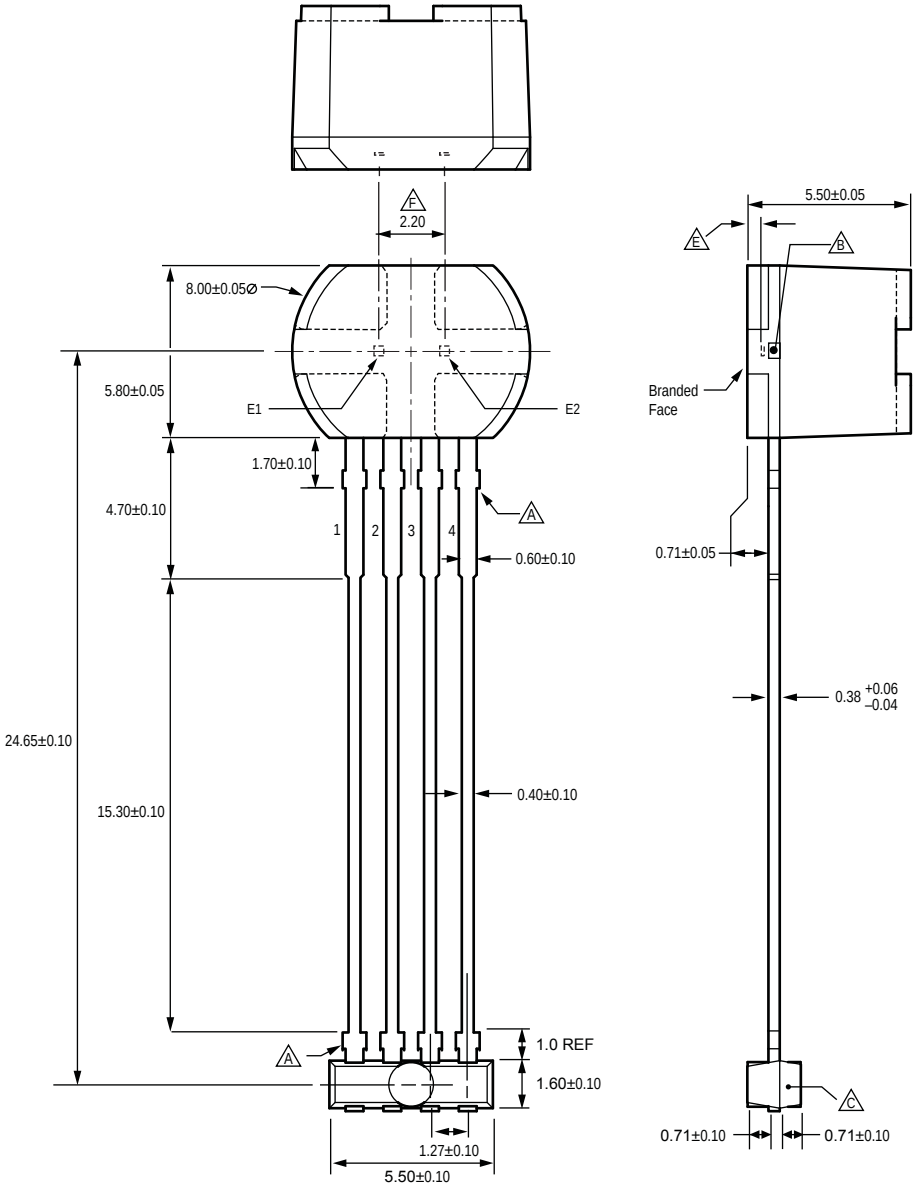
Finally, invert equation 1 with respect to voltage:

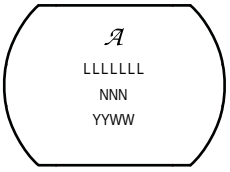
$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 119\ mW \div 12\ mA = 9.9\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC}(est)$.

Compare $V_{CC}(est)$ to $V_{CC}(max)$. If $V_{CC}(est) \leq V_{CC}(max)$, then reliable operation between $V_{CC}(est)$ and $V_{CC}(max)$ requires enhanced $R_{\theta JA}$. If $V_{CC}(est) \geq V_{CC}(max)$, then operation between $V_{CC}(est)$ and $V_{CC}(max)$ is reliable under these conditions.

Package SG, 4-Pin SIP





D Standard Branding Reference View

A = Supplier emblem
L = Lot identifier
N = Last three numbers of device part number
Y = Last two digits of year of manufacture
W = Week of manufacture

For Reference Only, not for tooling use (reference DWG-9002)
Dimensions in millimeters

A Dambar removal protrusion (16X)

B Metallic protrusion, electrically connected to pin 4 and substrate (both sides)

C Thermoplastic Molded Lead Bar for alignment during shipment

D Branding scale and appearance at supplier discretion

E Active Area Depth, 0.43 mm

F Hall elements (E1, E2), not to scale

Revision History

Revision	Current Revision Date	Description of Revision
Rev. 5	April 14, 2011	Update $T_{\theta E}$

For the latest version of this document, visit our website:

www.allegromicro.com