

NB4L52

2.5 V/3.3 V/5.0 V Differential Data/Clock D Flip-Flop with Reset

Multi-Level Inputs to LVPECL Translator w/ Internal Termination

The NB4L52 is a differential Data and Clock D flip-flop with a differential asynchronous Reset. The differential inputs incorporate internal 50 Ω termination resistors and will accept PECL, LVPECL, LVCMOS, LVTTTL, CML, or LVDS logic levels. When Clock transitions from Low to High, Data will be transferred to the differential LVPECL outputs. The differential Clock inputs allow the NB4L52 to also be used as a negative edge triggered device. The device is housed in a small 3x3 mm 16 pin QFN package.

Features

- Maximum Input Clock Frequency > 4 GHz Typical
- 330 ps Typical Propagation Delay
- 145 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 750 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 2.375\text{ V to }5.5\text{ V}$ with $V_{EE} = 0\text{ V}$
- Internal Input Termination Resistors, 50 Ω
- Functionally Compatible with Existing 2.5 V/3.3 V/5.0 V LVPECL, LVEP, EP, and SG Devices
- $-40^{\circ}\text{C to }+85^{\circ}\text{C}$ Ambient Operating Temperature
- These are Pb-Free Devices



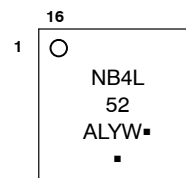
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



QFN-16
MN SUFFIX
CASE 485G



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

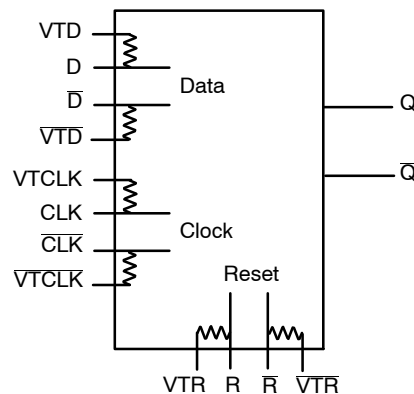


Figure 1. Logic Diagram

Table 1. TRUTH TABLE

R	D	CLK	Q
H	x	x	L
L	L	Z	L
L	H	Z	H

Z = LOW to HIGH Transition
x = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NB4L52

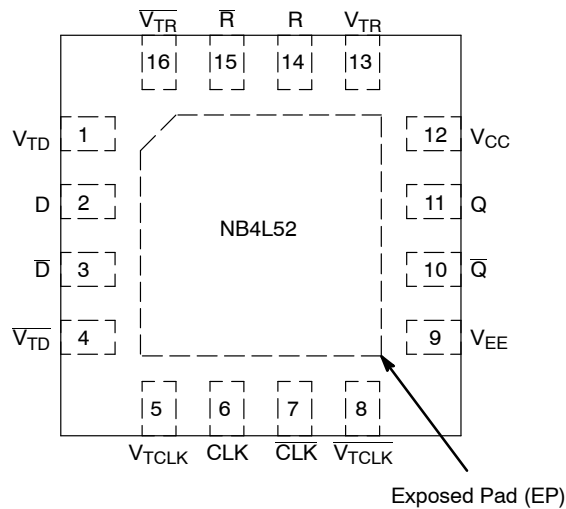


Figure 2. Pinout (Top View)

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{V_{TD}}$	-	Internal 50 Ω Termination Pin. (See Table 4)
2	D	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input. (Note 1)
3	\overline{D}	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input. (Note 1)
4	$\overline{V_{TD}}$	-	Internal 50 Ω Termination Pin. (See Table 4)
5	$\overline{V_{TCLK}}$	-	Internal 50 Ω Termination Pin. (See Table 4)
6	CLK	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input. (Note 1)
7	\overline{CLK}	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input. (Note 1)
8	$\overline{V_{TCLK}}$	-	Internal 50 Ω Termination Pin. (See Table 4)
9	V_{EE}	-	Negative Supply Voltage
10	\overline{Q}	ECL Output	Inverted Differential Output. Typically terminated with 50 Ω resistor to $V_{CC} - 2.0$ V.
11	Q	ECL Output	Noninverted Differential Output. Typically terminated with 50 Ω resistor to $V_{CC} - 2.0$ V.
12	V_{CC}	-	Positive Supply Voltage
13	$\overline{V_{TR}}$	-	Internal 50 Ω Termination Pin. (See Table 4)
14	R	LVECL, LVCMOS, LVTTTL Input	Noninverted Differential Reset Input. (Note 1)
15	\overline{R}	LVECL, LVCMOS, LVTTTL Input	Inverted Differential Reset Input. (Note 1)
16	$\overline{V_{TR}}$	-	Internal 50 Ω Termination Pin. (See Table 4)
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to V_{EE} on the PC board.

1. In the differential configuration when the input termination pin ($\overline{V_{TD}}$, $\overline{V_{TD}}$, $\overline{V_{TR}}$, $\overline{V_{TR}}$, $\overline{V_{TCLK}}$, $\overline{V_{TCLK}}$) are connected to a common termination voltage or left open, and if no signal is applied on D/ \overline{D} , CLK/ \overline{CLK} , R/ \overline{R} input then the device will be susceptible to self-oscillation.

NB4L52

Table 3. ATTRIBUTES

Characteristic	Value	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 1 kV
Moisture Sensitivity (Note 2)	Pb Pkg	Pb-Free Pkg
	QFN-16	Level 1 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count	164	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	V _{EE} = 0 V		6.0	V
V _{EE}	Negative Power Supply	V _{CC} = 0 V		-6.0	V
V _{IO}	Positive Input/Output Negative Input/Output	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6.0 -6.0	V V
I _{IN}	Input Current Through R _T (50 Ω Resistor)	Static Surge		45 80	mA mA
I _{out}	Output Current	Continuous Surge		25 50	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	16 QFN 16 QFN	42 35	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 3)	16 QFN	4.0	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB4L52

Table 5. DC CHARACTERISTICS, CLOCK INPUTS, LVPECL OUTPUTS

($V_{CC} = 2.375\text{ V to }5.5\text{ V}$, $V_{EE} = 0\text{ V or }V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ to }-5.5\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{EE}	Power Supply Current (Inputs and Outputs Open)		16	25	mA
V_{OH}	Output HIGH Voltage (Note 4, 5) $V_{CC} = 5.0\text{ V}$ $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1145$ 3855 2155 1355	$V_{CC} - 1020$ 3980 2280 1480	$V_{CC} - 895$ 4105 2405 1605	mV
V_{OL}	Output LOW Voltage (Note 4, 5) $V_{CC} = 5.0\text{V}$ $V_{CC} = 3.3\text{V}$ $V_{CC} = 2.5\text{V}$	$V_{CC} - 1945$ 3055 1355 555	$V_{CC} - 1770$ 3230 1530 730	$V_{CC} - 1600$ 3400 1700 900	mV

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 4 & 7)

V_{th}	Input Threshold Reference Voltage Range (Note 6)	1050		$V_{CC} - 150$	mV
V_{IH}	Single-ended Input HIGH Voltage	$V_{th} + 150$		V_{CC}	mV
V_{IL}	Single-ended Input LOW Voltage	V_{EE}		$V_{th} - 150$	mV

DIFFERENTIAL INPUT DRIVEN DIFFERENTIALLY (Figures 5, 6 & 8)

V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		$V_{CC} - 150$	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 7)	1125		$V_{CC} - 75$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	150		V_{CC}	mV
I_{IH}	Input HIGH Current D / \bar{D} , CLK / \bar{CLK} , R / \bar{R} (V_{Tx}/\bar{V}_{Tx} Open)	-150		150	μA
I_{IL}	Input LOW Current D / \bar{D} , CLK / \bar{CLK} , R / \bar{R} (V_{Tx}/\bar{V}_{Tx} Open)	-150		150	μA
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. LVPECL outputs loaded with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$ for proper operation.
5. Input and output parameters vary 1:1 with V_{CC} .
6. V_{th} is applied to the complementary input when operating in single-ended mode.
7. V_{CMRMIN} varies 1:1 with V_{EE} , V_{CMRMAX} varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

NB4L52

Table 6. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }5.5\text{ V}$; $V_{EE} = 0\text{ V or }V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ to }-5.5\text{ V}$ (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 10) (See Figure 4) $f_{in} \leq 2.0\text{ GHz}$ $f_{in} \leq 3.0\text{ GHz}$ $f_{in} \leq 4.0\text{ GHz}$	530	770		530	780		530	760		mV
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential CLK to Q, R to Q	300	400	500	300	400	500	300	400	500	ps
t_s	Setup Time	100			100			100			ps
t_h	Hold Time	50			50			50			ps
t_{RR}	Reset Recovery	400			400			400			ps
t_{PW}	Minimum Pulse Width R/R	250			250			250			ps
t_{JITTER}	RMS Random Clock Jitter (Note 9) $f_{in} \leq 2.0\text{ GHz}$ $f_{in} \leq 3.0\text{ GHz}$ $f_{in} \leq 4.0\text{ GHz}$		1			1			1		ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 10)	150		2800	150		2800	150		2800	mV
t_r t_f	Output Rise/Fall Times @ 0.5 GHz (20% – 80%)	80	135	190	80	145	190	80	155	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. All loading with an external $R_L = 50\ \Omega$ to $V_{CC} - 2.0\text{ V}$. Input edge rates 40 ps (20% – 80%).
9. Additive RMS jitter with 50% duty cycle clock signal.
10. Input and output voltage swing is a single-ended measurement operating in differential mode.

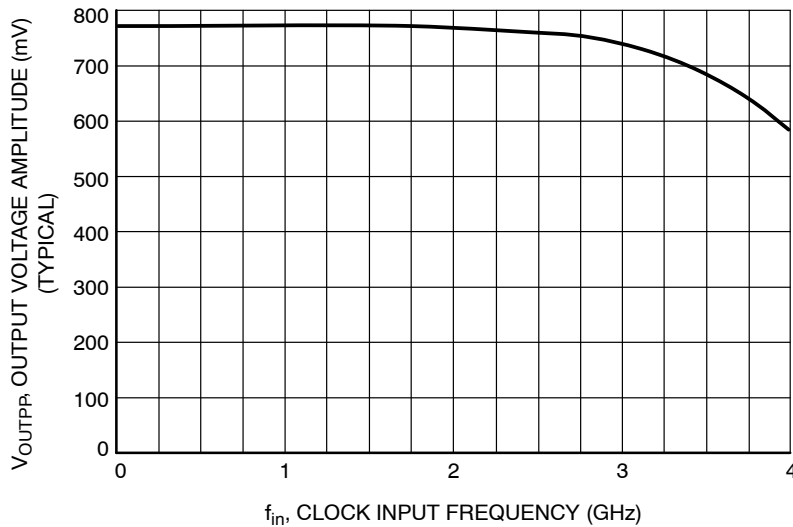


Figure 3. Output Voltage Amplitude (V_{OUTPP}) vs. Clock Input Frequency at Ambient Temperature (Typical).

NB4L52

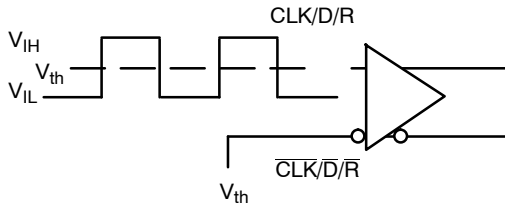


Figure 4. Differential Input Driven Single-Ended

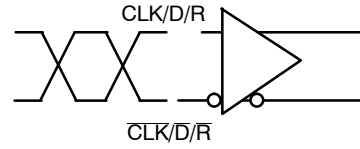


Figure 5. Differential Inputs Driven Differentially

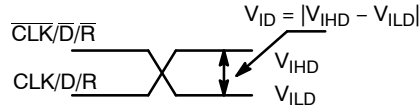


Figure 6. Differential Inputs Driven Differentially

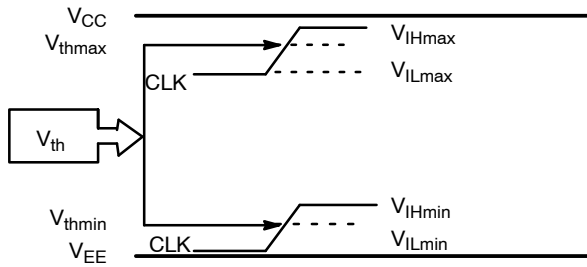


Figure 7. V_{th} Diagram

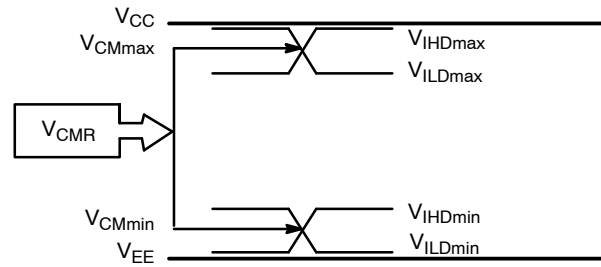


Figure 8. V_{CM} Diagram

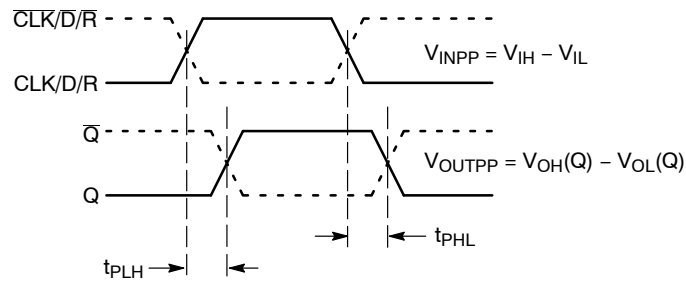


Figure 9. AC Reference Measurement

NB4L52

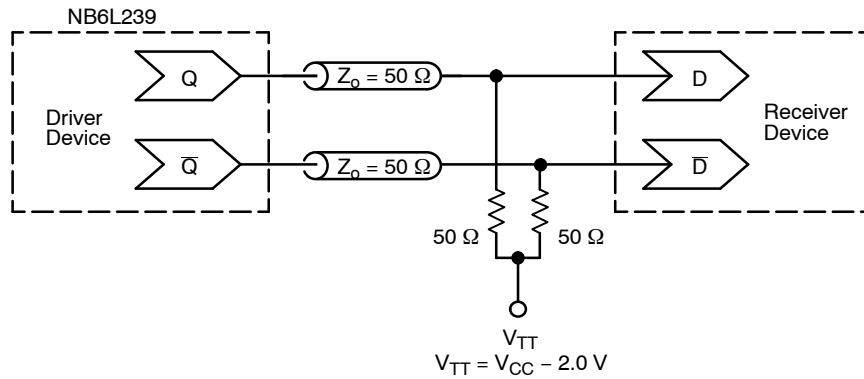


Figure 10. Typical Termination for Output Driver and Device Evaluation
 (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
NB4L52MNG	QFN-16, 3 x 3 mm (Pb-Free)	123 Units / Rail
NB4L52MNR2G	QFN-16, 3 x 3 mm (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

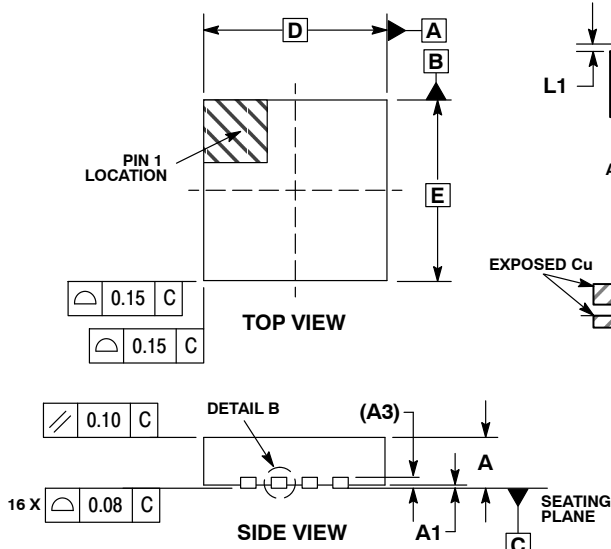
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

NB4L52

PACKAGE DIMENSIONS

16 PIN QFN CASE 485G-01 ISSUE D

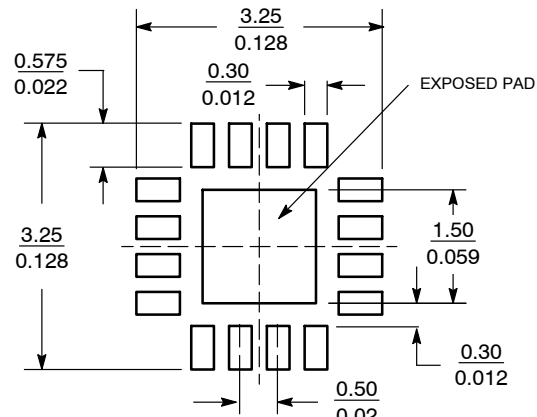
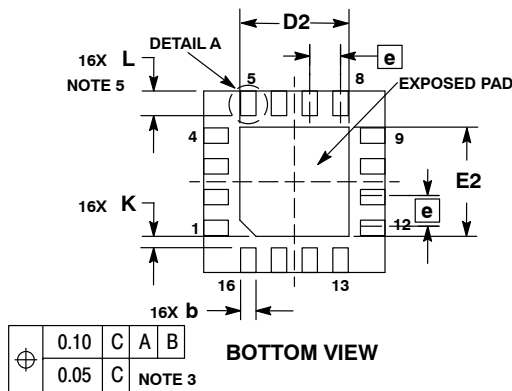


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.18	TYP
L	0.30	0.50
L1	0.00	0.15

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NB4L52), may be covered by U.S. patents including 6,362,644. There may be other patents pending.

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