

Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
Channel-1	30	0.022 at V _{GS} = 10 V	10
		0.030 at V _{GS} = 4.5 V	8
Channel-2		0.022 at V _{GS} = 10 V	10
		0.028 at V _{GS} = 4.5 V	8

SCHOTTKY PRODUCT SUMMARY		
V _{DS} (V)	V _{SD} (V) Diode Forward Voltage	I _F (A)
30	0.50 V at 1.0 A	3.0

FEATURES

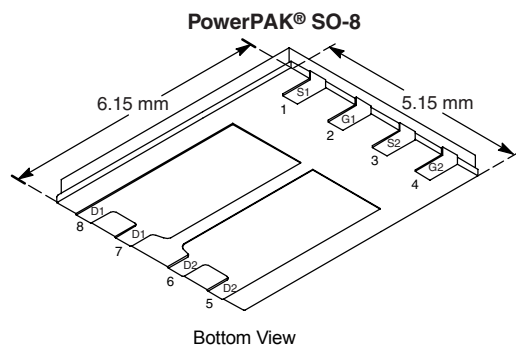
- Halogen-free Option Available
- LITTLE FOOT® Plus Schottky
- PWM Optimized
- New Low Thermal Resistance PowerPAK® Package with low 1.07 mm Profile



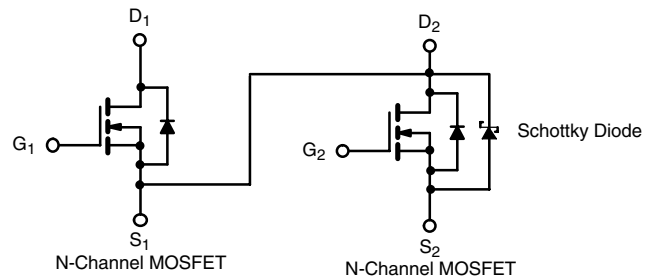
RoHS
COMPLIANT

APPLICATIONS

- Asymmetrical Buck-Boost DC/DC Converter



Ordering Information: Si7872DP-T1-E3 (Lead (Pb)-free)
Si7872DP-T1-GE3 (Lead (Pb)-free and Halogen-f



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter	Symbol	10 s		Steady State		Unit	
		Channel-1	Channel-2	Channel-1	Channel-2		
Drain-Source Voltage	V _{DS}	30				V	
Gate-Source Voltage	V _{GS}	± 20	± 12	± 20	± 12		
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	10	6.4		A	
		T _A = 70 °C	7	5.1			
Pulsed Drain Current	I _{DM}	30				A	
Continuous Source Current (Diode Conduction) ^a	I _S	2.9		1.1			
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.5		1.4		W
		T _A = 70 °C	2.2		0.9		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	
Soldering Recommendations (Peak Temperature) ^{b,c}		260					

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	MOSFET		Schottky		Unit	
		Typical	Maximum	Typical	Maximum		
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	26	35	26	35	°C/W
		Steady State	60	85	60	85	
Maximum Junction-to-Case (Drain)	R _{thJC}	4.1	6.0	4.1	6.0		

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. ^b	Max.	Unit		
Static								
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.0		3.0	V	
			Ch-2	0.8		2.0		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			± 100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	Ch-2			± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	μA	
			Ch-2			100		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$	Ch-1			15		
			Ch-2			2000		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20			A	
			Ch-2	20				
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$	Ch-1		0.017	0.022	Ω	
			Ch-2		0.016	0.022		
		$V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$	Ch-1		0.024	0.030		
			Ch-2		0.020	0.028		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 7.5\text{ A}$	Ch-1		19		S	
			Ch-2		21			
Diode Forward Voltage ^b	V_{SD}	$I_S = 1\text{ A}, V_{GS} = 0\text{ V}$	Ch-1		0.75	1.2	V	
			Ch-2		0.47	0.5		
Dynamic^a								
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}$	Ch-1		7	11	nC	
			Ch-2		11.5	18		
Gate-Source Charge	Q_{gs}		Ch-1		2.9			
			Ch-2		3.8			
Gate-Drain Charge	Q_{gd}		Ch-1		2.5			
			Ch-2		3.5			
Gate Resistance	R_G		Ch-1		1.5		Ω	
			Ch-2		1.8			
Turn-On Delay Time	$t_{d(on)}$		$V_{DD} = 15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\text{ }\Omega$	Ch-1		9	15	ns
				Ch-2		12	20	
Rise Time	t_r	Ch-1			10	17		
		Ch-2			10	17		
Turn-Off Delay Time	$t_{d(off)}$	Ch-1			19	30		
		Ch-2			40	66		
Fall Time	t_f	Ch-1			9	15		
		Ch-2			9	15		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		Ch-1		35	55	
				Ch-2		28	45	

Notes:

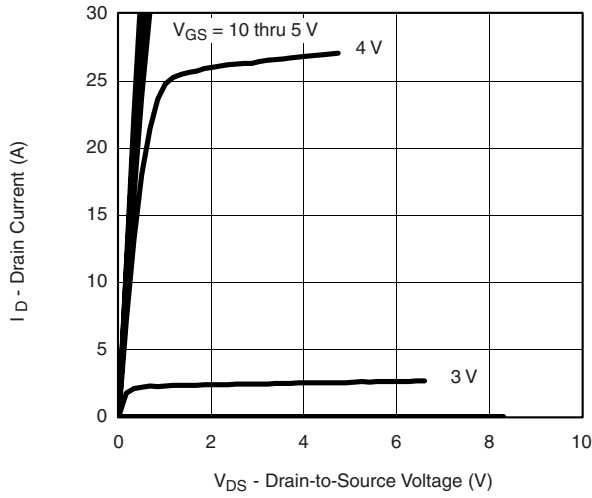
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

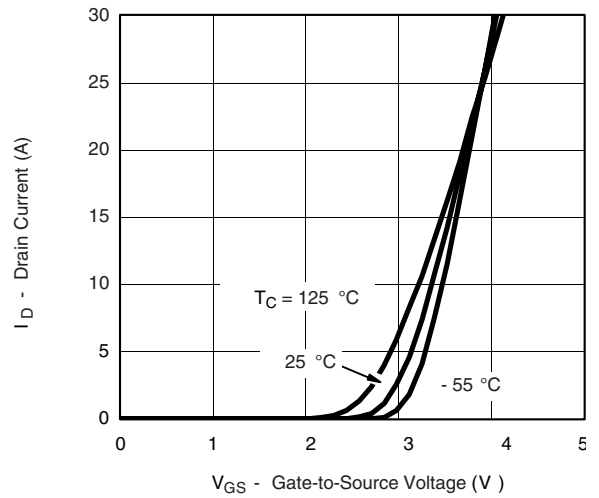
SCHOTTKY SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	$I_F = 1.0\text{ A}$		0.47	0.50	V
		$I_F = 1.0\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.36	0.42	
Maximum Reverse Leakage Current	I_{rm}	$V_r = 30\text{ V}$		0.004	0.100	mA
		$V_r = 30\text{ V}, T_J = 100\text{ }^\circ\text{C}$		0.7	10	
		$V_r = -30\text{ V}, T_J = 125\text{ }^\circ\text{C}$		3.0	20	
Junction Capacitance	C_T	$V_r = 10\text{ V}$		50		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

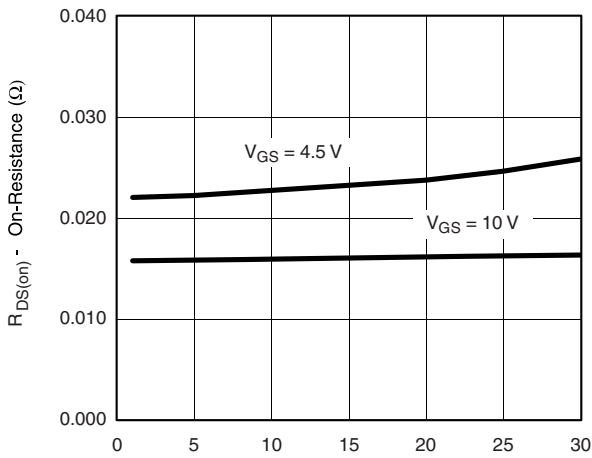
MOSFET CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



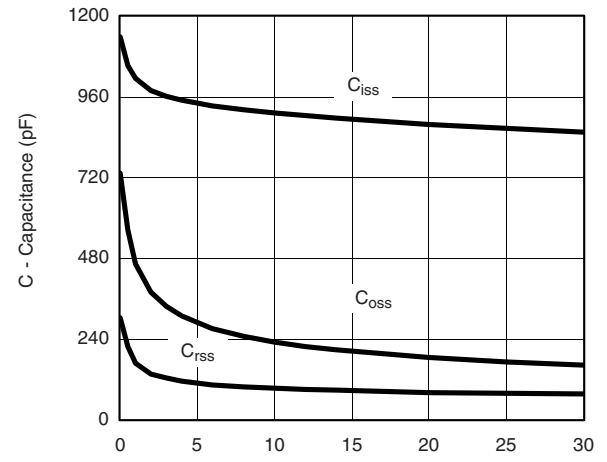
Output Characteristics



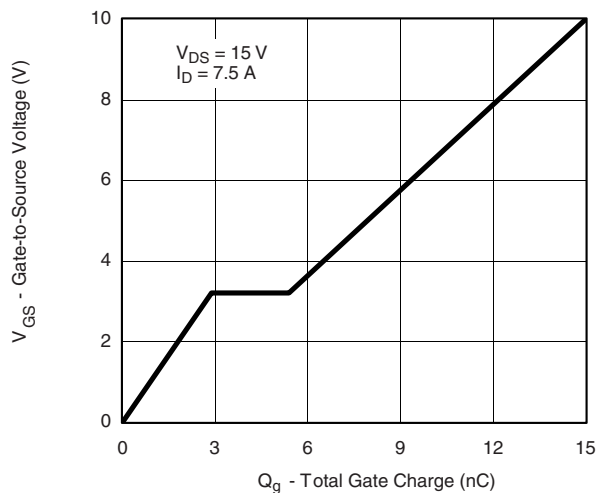
Transfer Characteristics



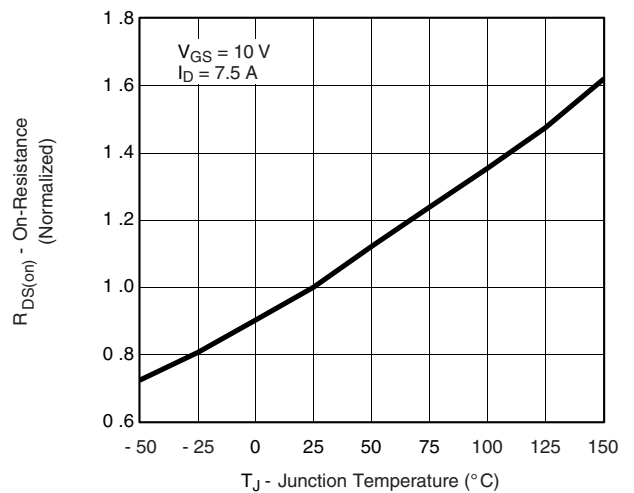
On-Resistance vs. Drain Current



Capacitance

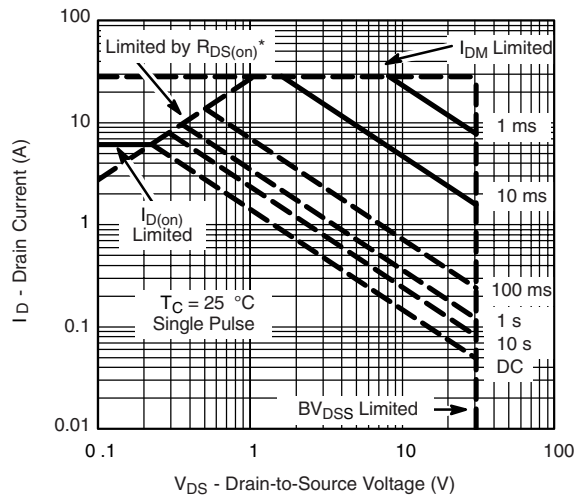
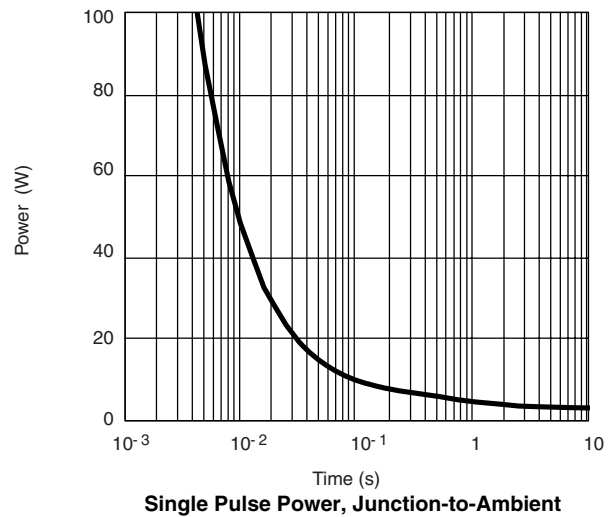
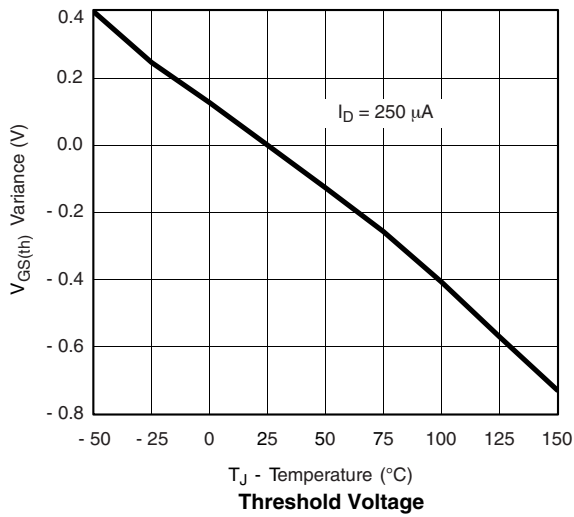
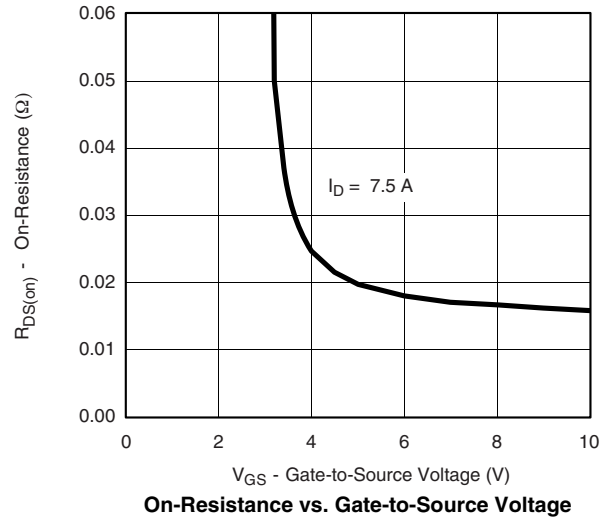
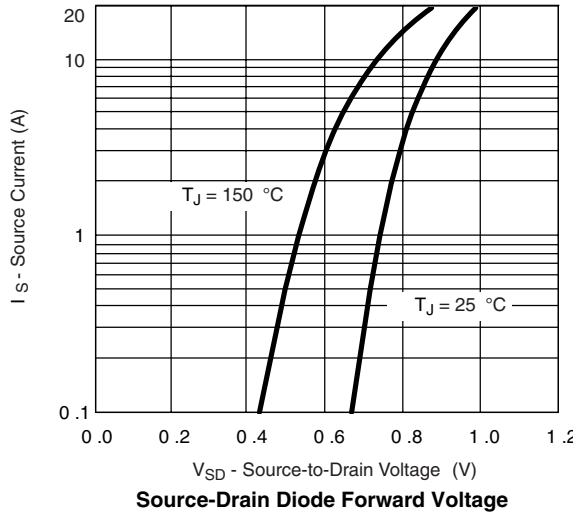


Gate Charge



On-Resistance vs. Junction Temperature

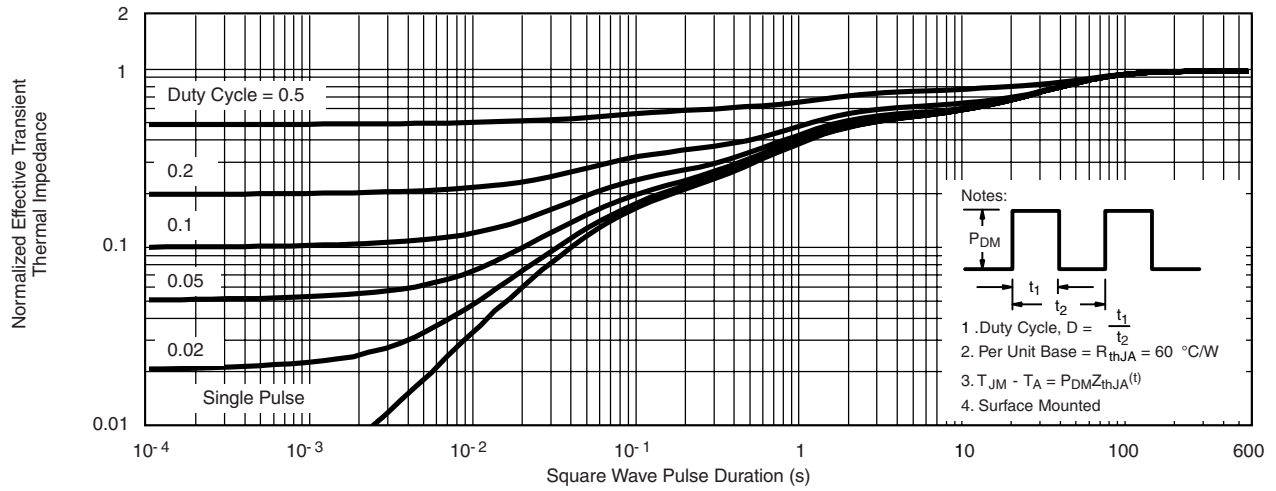
MOSFET CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



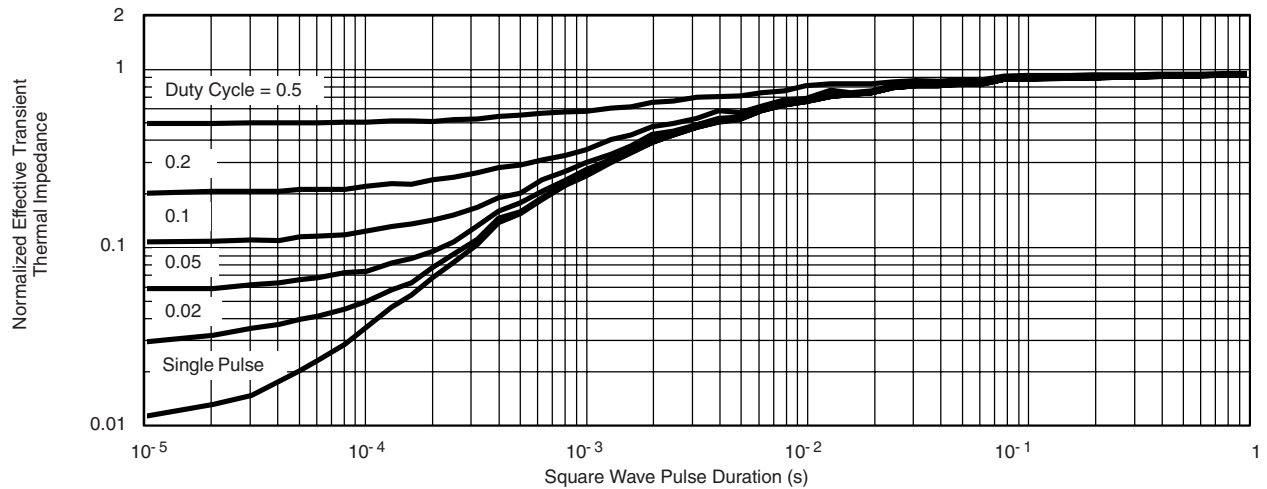
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Foot

MOSFET CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

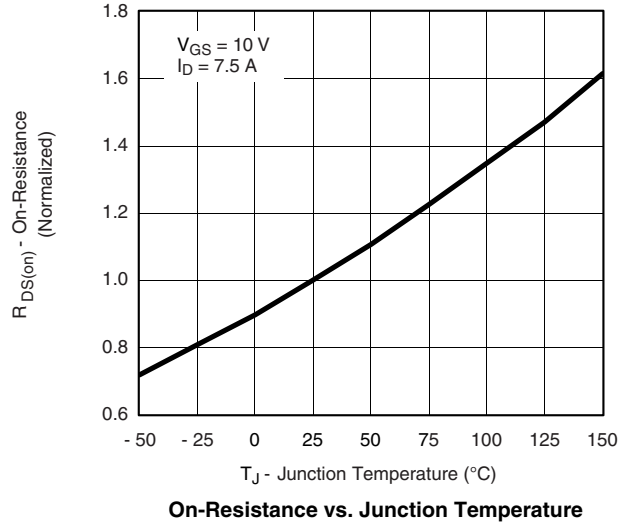
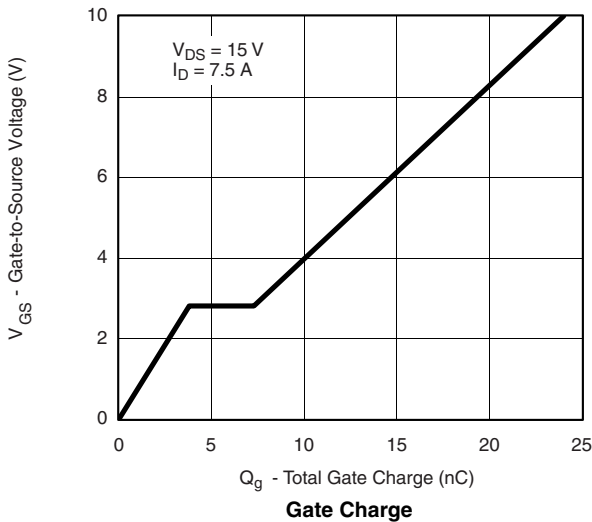
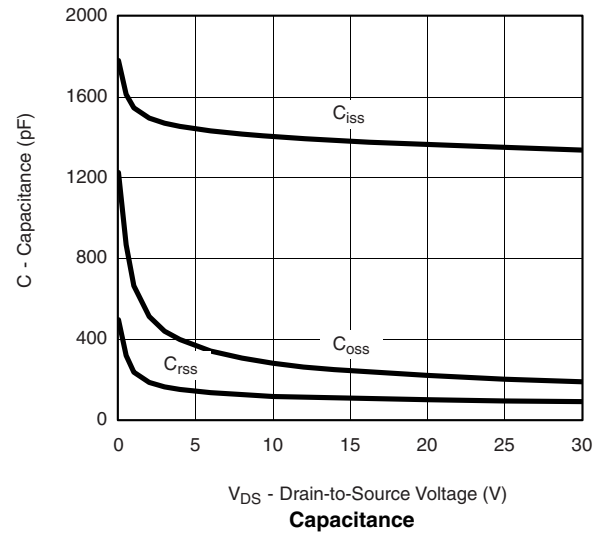
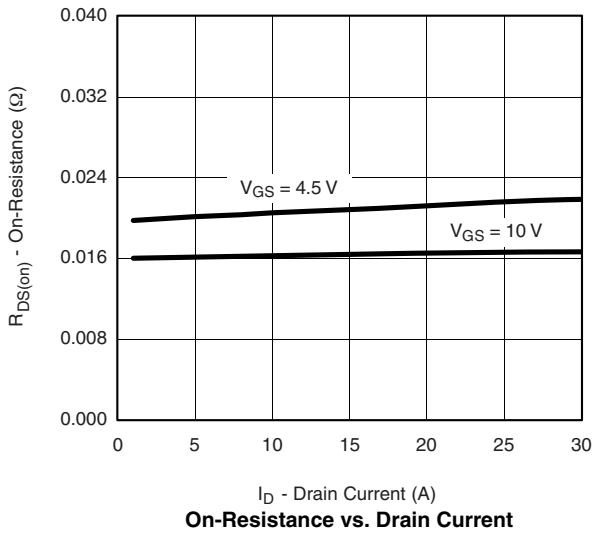
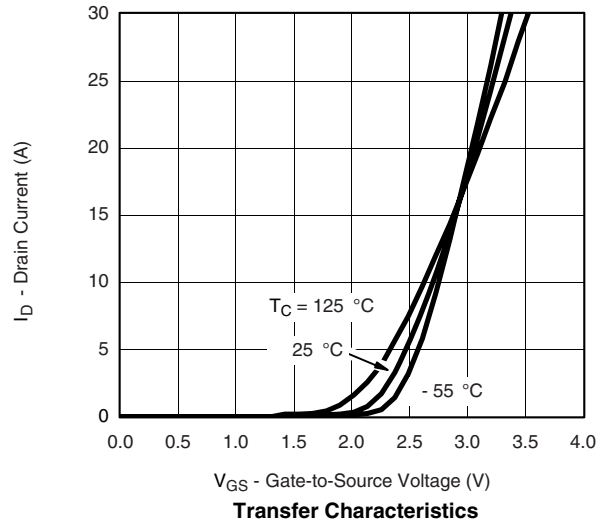
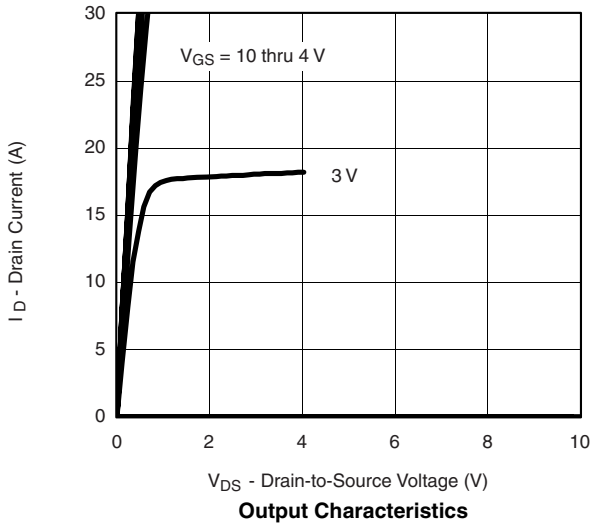


Normalized Thermal Transient Impedance, Junction-to-Ambient

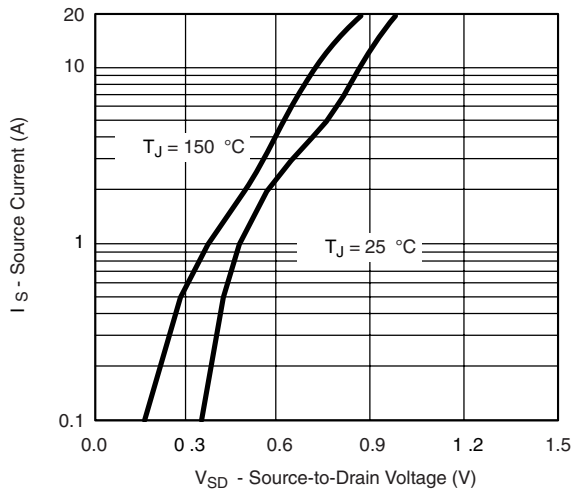


Normalized Thermal Transient Impedance, Junction-to-Case

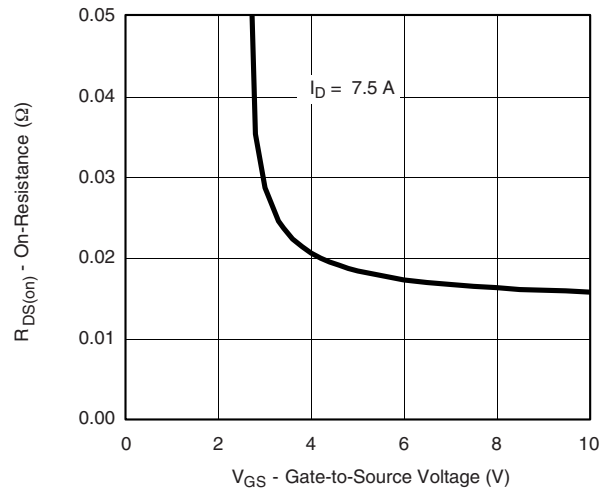
MOSFET CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



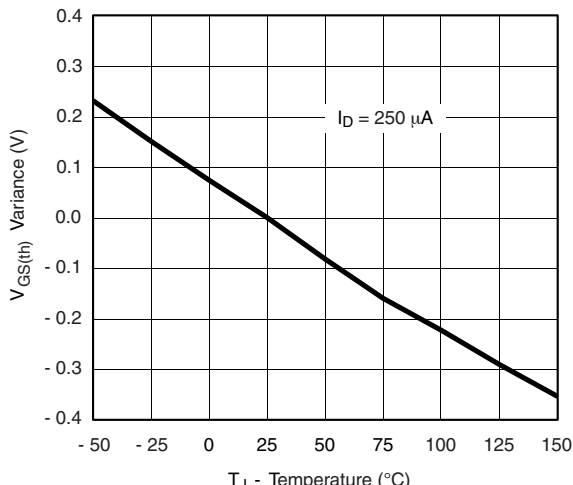
MOSFET CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



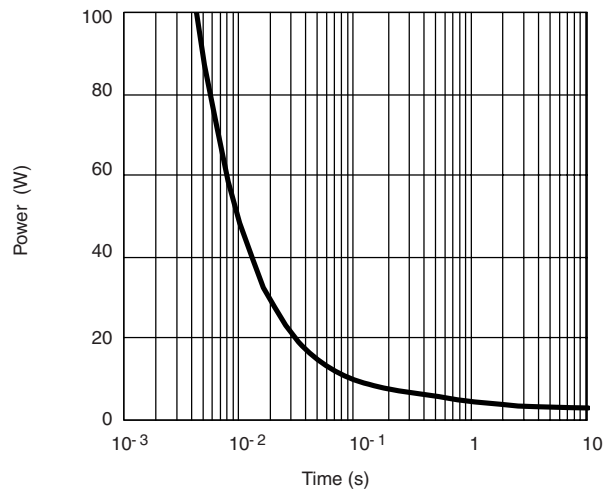
Source-Drain Diode Forward Voltage



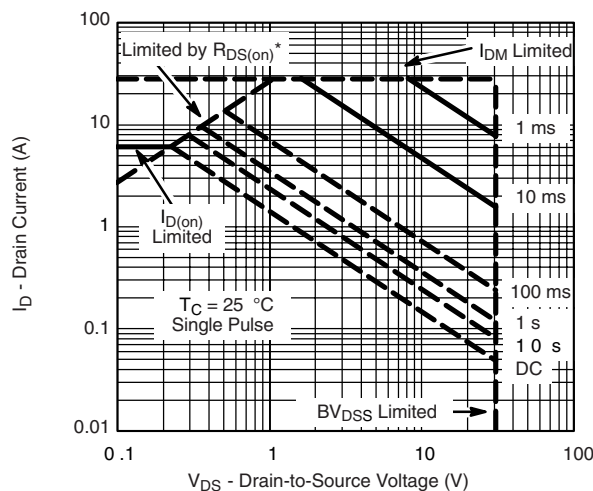
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



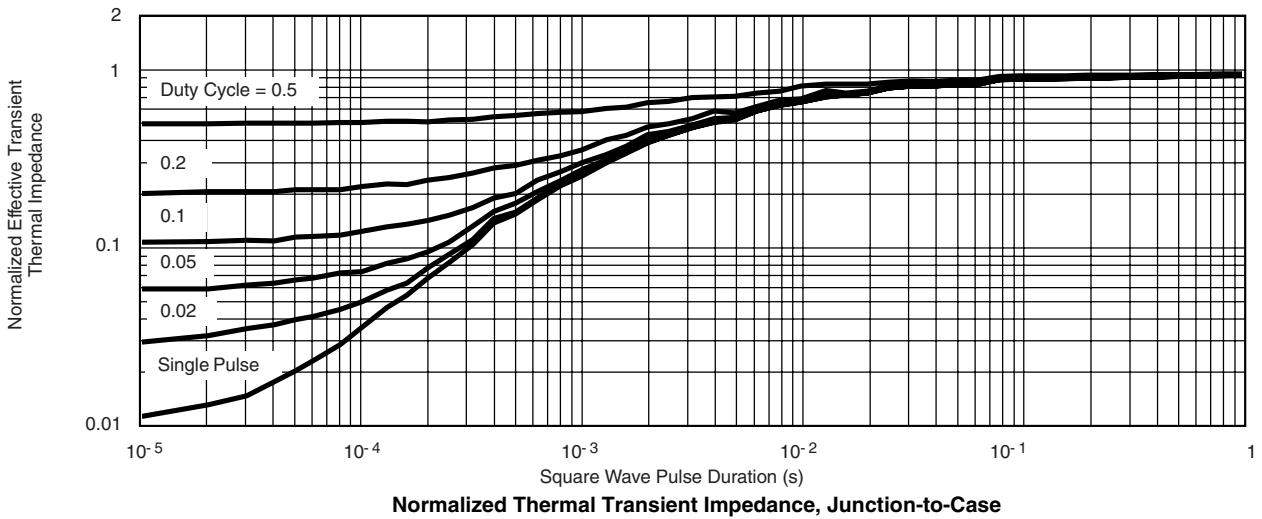
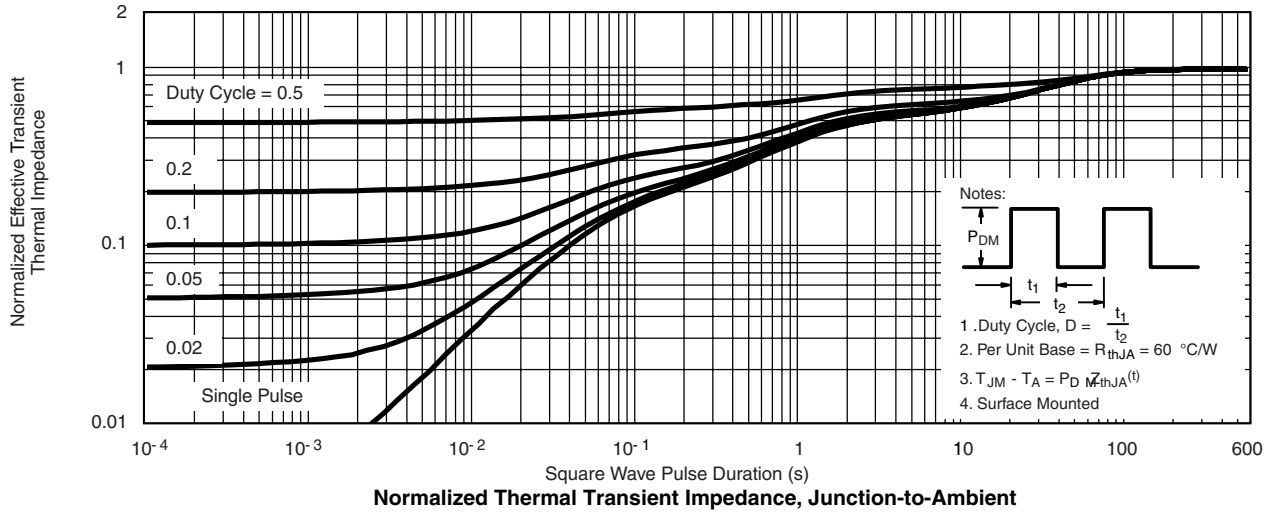
Single Pulse Power, Junction-to-Ambient



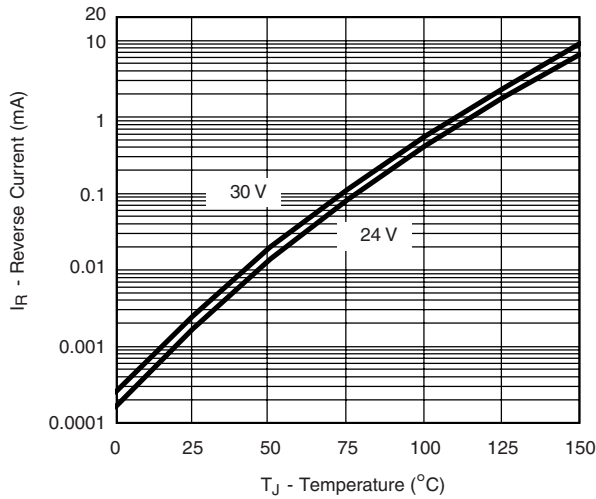
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Foot

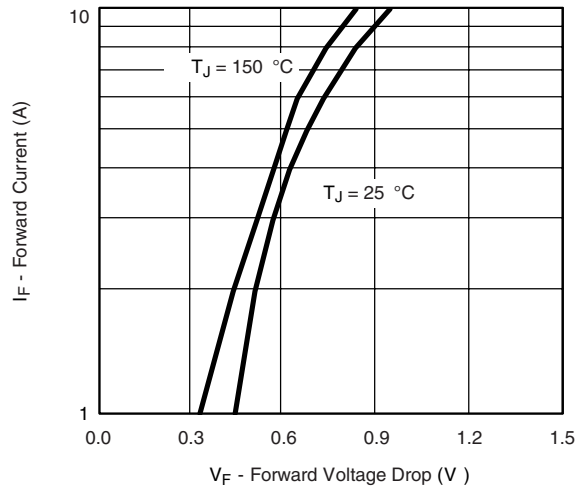
MOSFET CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



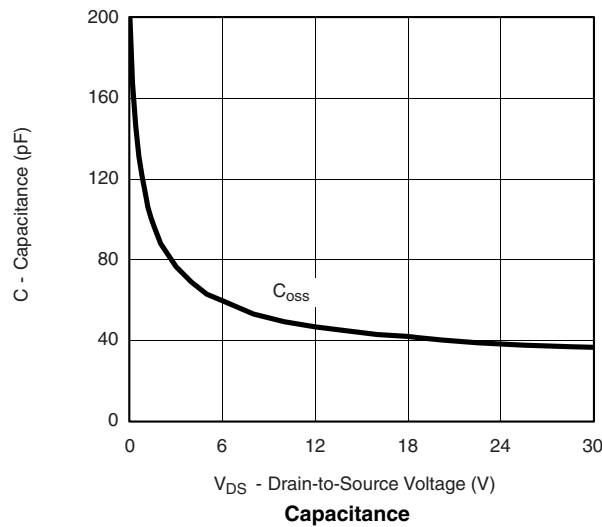
SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Reverse Current vs. Junction Temperature



Forward Voltage Drop



Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72035>.



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