74AHCU04-Q100

Hex unbuffered inverter

Rev. 2 — 7 December 2015 **Product data sheet**

1. General description

The 74AHCU04-Q100 is high-speed Si-gate CMOS device and is pin compatible with low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHCU04-Q100 is a general-purpose hex unbuffered inverter. Each of the six inverters is a single stage.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Low power dissipation
- Balanced propagation delays
- Inputs accept voltages higher than V_{CC}
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHCU04D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCU04PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCU04BQ-Q100	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

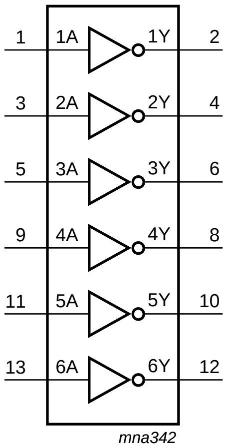


Fig 1. Logic symbol

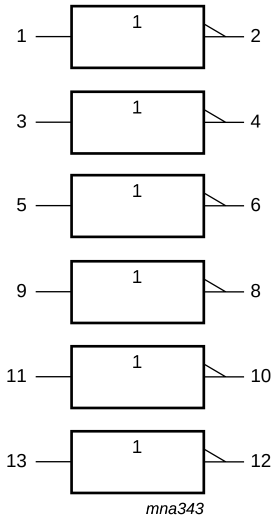


Fig 2. IEC logic symbol

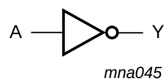


Fig 3. Logic diagram (one inverter)

5. Pinning information

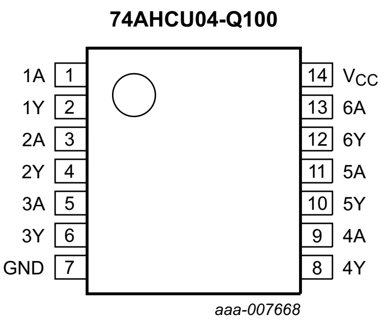
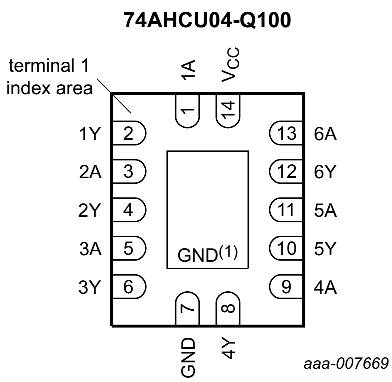


Fig 4. Pin configuration SO14 and TSSOP14



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	**nY**
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V		–20	-	mA
V_I	input voltage		[1]	–0.5	+7.0	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			–75	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			2.0	5.0	5.5	V
V_I	input voltage			0	-	5.5	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature			–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V		-	-	100	ns/V
		V_{CC} = 5.0 V ± 0.5 V		-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V_{CC} = 3.0 V	2.4	-	-	2.4	-	2.4	-	V
		V_{CC} = 5.5 V	4.4	-	-	4.4	-	4.4	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V_{CC} = 3.0 V	-	-	0.6	-	0.6	-	0.6	V
		V_{CC} = 5.5 V	-	-	1.1	-	1.1	-	1.1	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –50 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	1.8	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.7	3.0	-	2.7	-	2.7	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.0	4.5	-	4.0	-	4.0	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.4	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.8	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	-	0.2	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.3	-	0.3	-	0.3	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.5	-	0.5	-	0.5	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
C_I	input capacitance		-	3	10	-	10	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6	[1]								
		V_{CC} = 3.0 V to 3.6 V	[2]								
		C_L = 15 pF		-	3.0	7.1	1.0	8.5	1.0	9.0	ns
		C_L = 50 pF		-	3.4	10.6	1.0	12.0	1.0	13.5	ns
		V_{CC} = 4.5 V to 5.5 V	[3]								
		C_L = 15 pF		-	2.4	5.5	1.0	6.5	1.0	7.0	ns
		C_L = 50 pF		-	3.5	7.0	1.0	8.0	1.0	9.0	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	9.1	-	-	-	-	-	pF

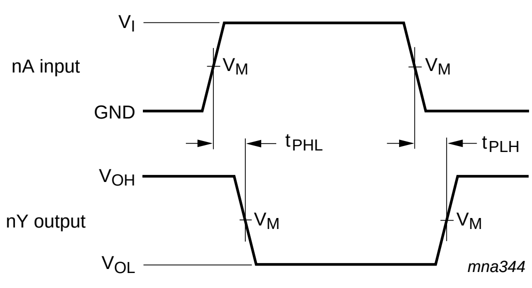
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] Typical values are measured at V_{CC} = 3.3 V.

[3] Typical values are measured at V_{CC} = 5.0 V.

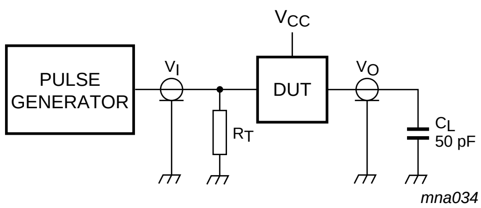
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



$V_M = 0.5 \times V_{CC}$; V_I = GND to V_{CC}.

Fig 6. The input (nA) to output (nY) propagation delay times



Test data is given in Table 7.

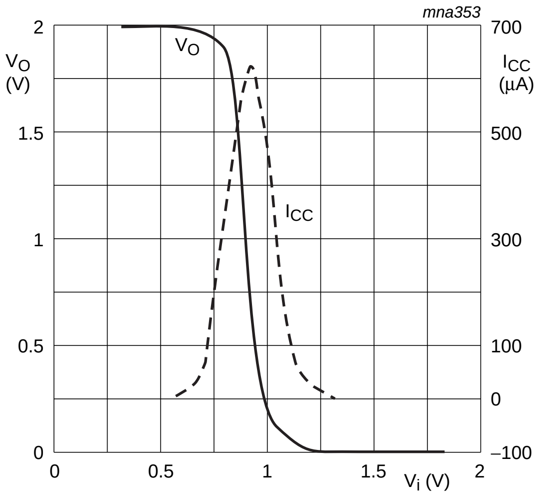
Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

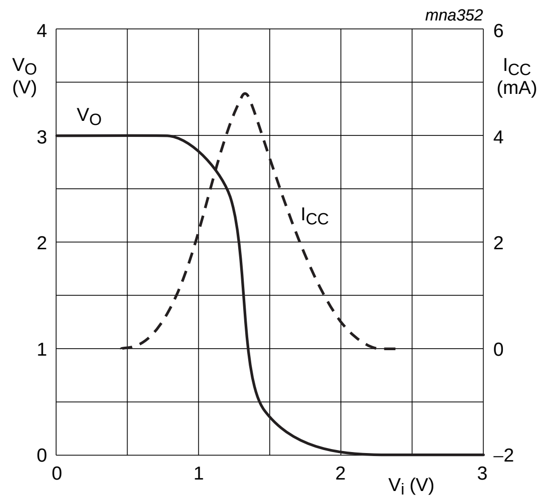
Fig 7. Test circuit for measuring switching times

12. Typical transfer characteristics



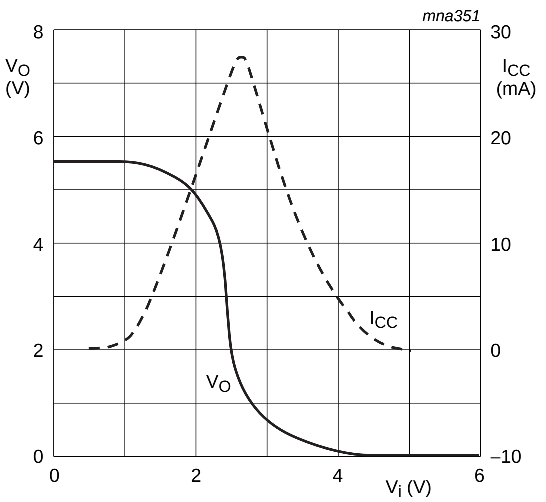
T_{amb} = 25 °C.

Fig 8. V_{CC} = 2.0 V; I_O = 0 A



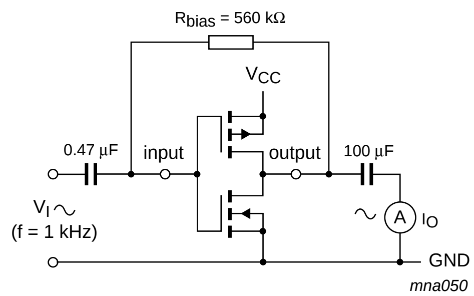
T_{amb} = 25 °C.

Fig 9. V_{CC} = 3.0 V; I_O = 0 A



T_{amb} = 25 °C.

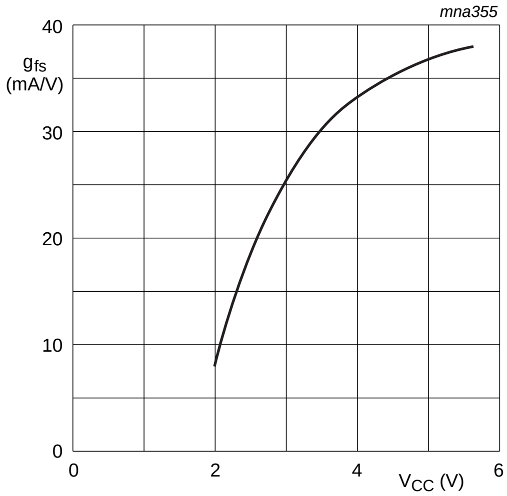
Fig 10. V_{CC} = 5.5 V; I_O = 0 A



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

f_i = 1 kHz at V_O is constant

Fig 11. Test set-up for measuring forward transconductance



T_{amb} = 25 °C.

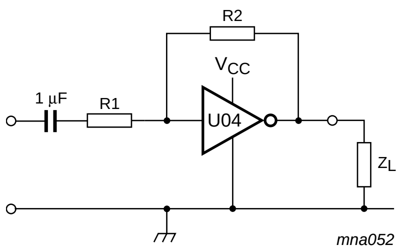
Fig 12. Typical forward transconductance as a function of the supply voltage

13. Application information

Some applications are:

- Linear amplifier (see Figure 13)
- Crystal oscillator design (see Figure 14)

Remark: All values given are typical unless otherwise specified.



Maximum $V_{o(p\text{-}p)} = V_{CC} - 1.5$ V centered at $0.5 \times V_{CC}$.

$$G_v = -\frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G_{ol} = open loop gain

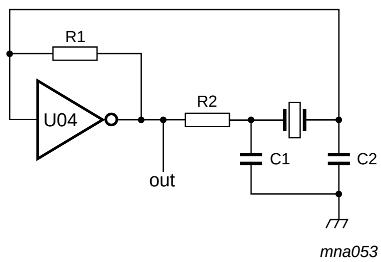
G_v = voltage gain

R1 ≥ 3 kΩ, R2 ≤ 1 MΩ

Z_L > 10 kΩ; G_{ol} = 12 (typical)

Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier



C1 = 47 pF (typical)

C2 = 33 pF (typical)

R1 = 1 MΩ to 10 MΩ (typical

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC}. I_{CC} is typically 5 mA at V_{CC} = 5 V and f_i = 10 MHz.

Fig 14. Crystal oscillator configuration

Table 8. External components for resonator (f < 1 MHz)

All values given are typical and must be used as an initial set-up.

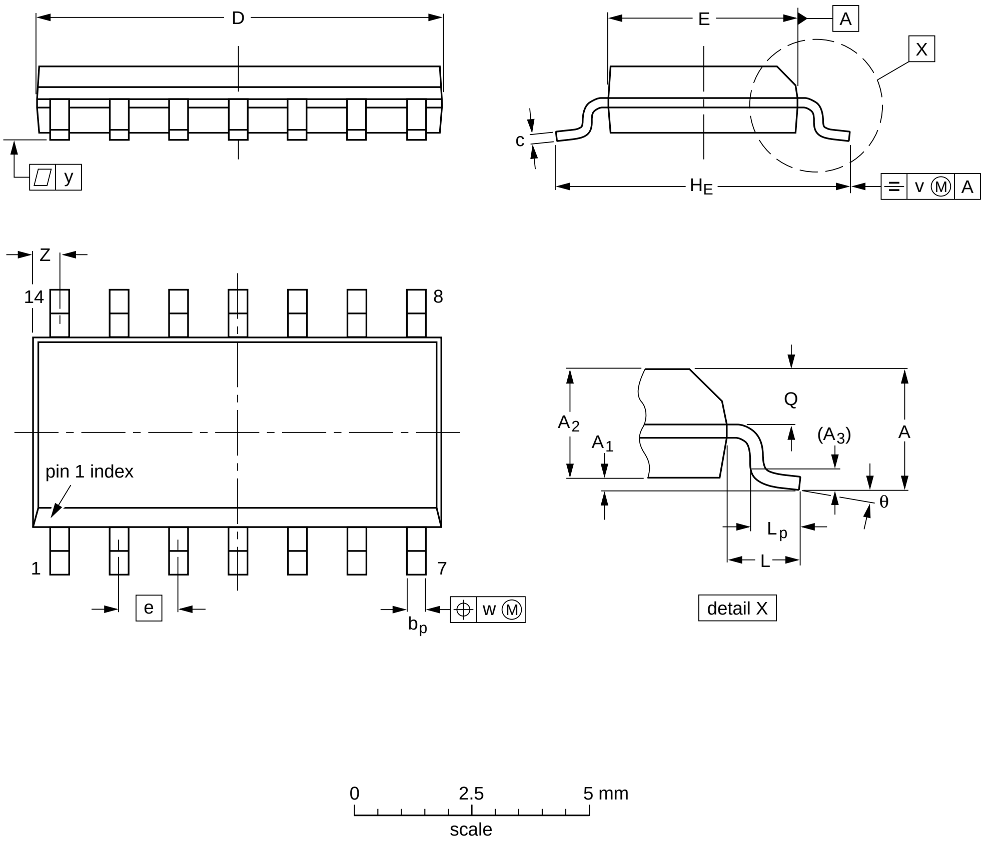
Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	22 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	22 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	22 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	22 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	10 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	10 MΩ	47 kΩ	47 pF	5 pF

Table 9. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I_{CC}
	8.0 kΩ	minimum influence due to change in V_{CC}
6 kHz	1.0 kΩ	minimum required I_{CC}
	4.7 kΩ	minimum influence by V_{CC}
10 kHz	0.5 kΩ	minimum required I_{CC}
	2.0 kΩ	minimum influence by V_{CC}
14 kHz	0.5 kΩ	minimum required I_{CC}
	1.0 kΩ	minimum influence by V_{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

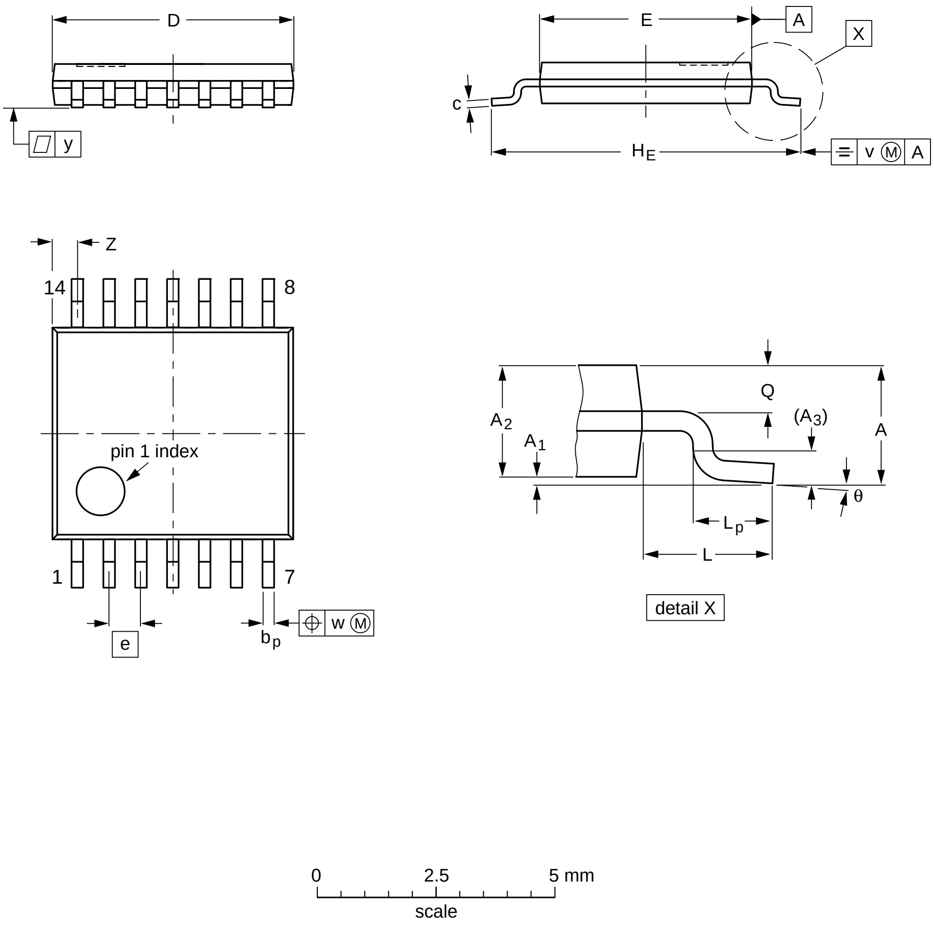
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

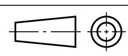
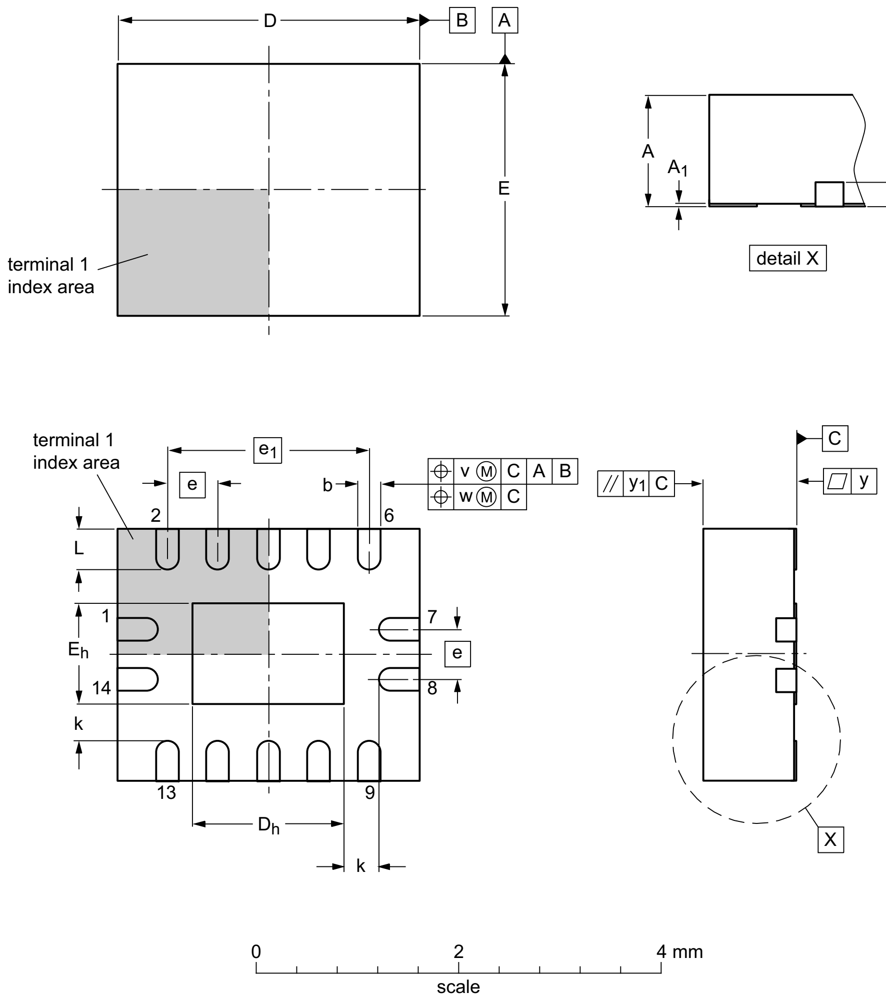
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig 17. Package outline SOT762-1 (DHVQFN14)

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCU04_Q100 v.2	20151207	Product data sheet	-	74AHCU04_Q100 v.1
Modifications:	• General description corrected (added "-Q100" to product types (errata)).			
74AHCU04_Q100 v.1	20130605	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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18. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

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