CYPRESS
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CYRF6986

WirelessUSB™ LPstar 2.4 GHz Radio SoC

Features

- 2.4 GHz direct sequence spread spectrum (DSSS) radio transceiver
- Operates in the unlicensed worldwide Industrial, Scientific, and Medical (ISM) band (2.400 GHz to 2.483 GHz)
- On Air compatible with second generation radio WirelessUSB™ LP and PRoC LP
- Pin-to-pin compatible with WirelessUSB LP except the Pin30 and Pin37

Low Power

- Operating current: 21 mA (transmit at –5 dBm)
- Sleep current less than 1 μA
- Operating voltage: 2.7 V to 3.6 V
- Fast startup and fast channel changes
- Supports coin-cell operated applications

Reliable and Robust

- Receive Sensitivity typical –90 dBm
- AutoRate™ – dynamic data rate reception
  - Enables data reception for any of the supported bit rates automatically.
  - DSSS (250 Kbps), GFSK (1 Mbps)
- Operating Temperature: 0 °C to 70 °C
- Closed-loop frequency synthesis for minimal frequency drift

Simple Development

- Auto transaction sequencer (ATS): Enables MCU to sleep longer
- Framing, length, CRC16, and auto ACK
- Separate 16-byte transmit and receive FIFOs
- Receive signal strength indication (RSSI)
- Serial peripheral interface (SPI) control while in sleep mode
- 4 MHz SPI microcontroller interface

BOM Savings

- Low external component count
- Battery voltage monitoring circuitry
- Small footprint 40-pin QFN (6 mm × 6 mm)

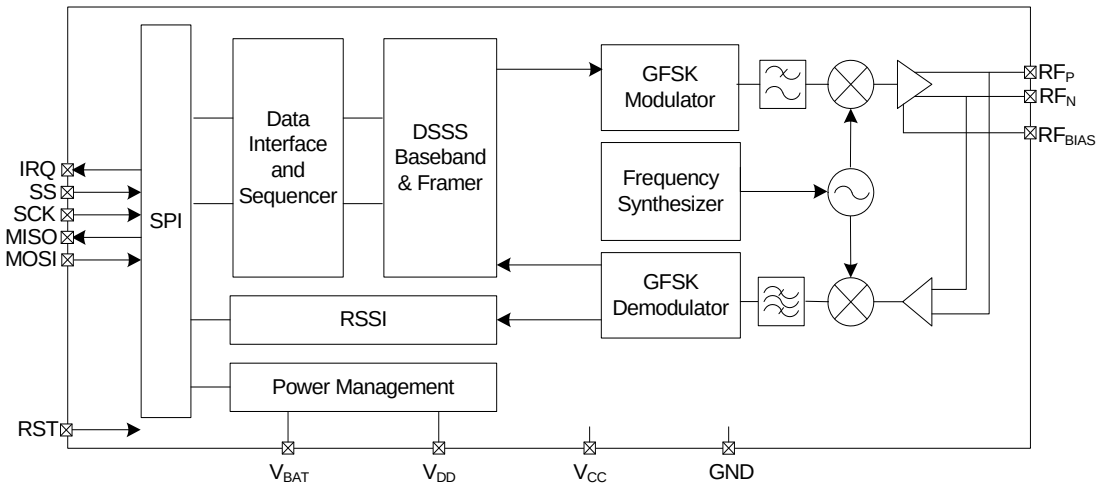
Applications

- Wireless keyboards and mice
- Presentation tools
- Wireless gamepads
- Remote controls
- Toys
- Fitness

Applications Support

See www.cypress.com for development tools, reference designs, and application notes.

Logic Block Diagram



Not recommended for new designs

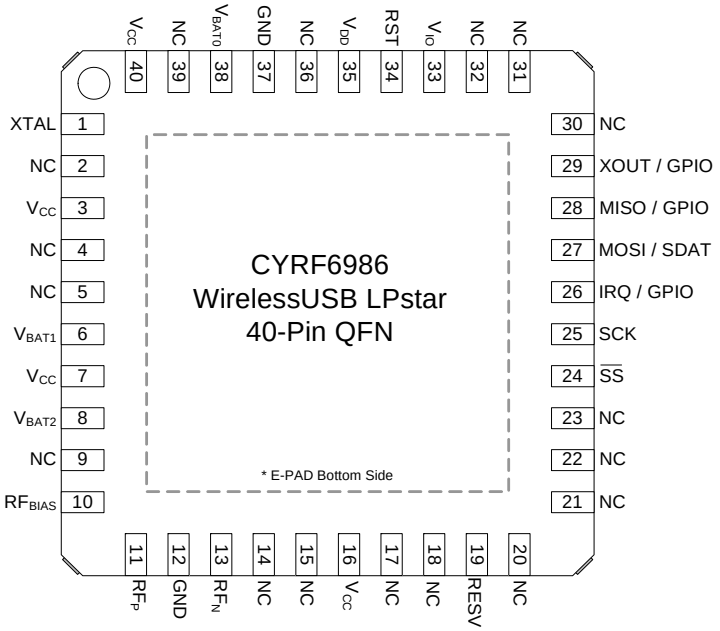
Contents

Functional Description

The CYRF6986 WirelessUSB LPstar radio is a second generation member of the Cypress WirelessUSB Radio System-On-Chip (SoC) family. The CYRF6986 IC adds a range of enhanced features, including reduced supply current in all operating modes, reduced crystal start up, synthesizer settling, and link turnaround times.

Pinouts

Figure 1. 40-pin QFN pinout



Pin Definitions

Pin Number	Name	Type	Default	Description
1	XTAL	I	I	12 MHz crystal.
2, 4, 5, 9, 14, 15, 17, 18, 20, 21, 22, 23, 31, 32, 36, 39	NC	NC		Connect to GND.
3, 7, 16, 40	V_{CC}	Pwr		V_{CC} = 2.7 V to 3.6 V.
6, 8, 38	$V_{BAT(0-2)}$	Pwr		V_{BAT} = 2.7 V to 3.6 V. Main supply.
10	RF_{BIAS}	O	O	RF IO 1.8 V reference voltage.
11	RF_P	I/O	I	Differential RF signal to and from antenna.
12	GND	GND		Ground.
13	RF_N	IO	I	Differential RF signal to and from antenna.
19	RESV	I		Must be connected to GND.
24	SS	I	I	SPI enable, active LOW assertion. Enables and frames transfers.
25	SCK	I	I	SPI clock.
26	IRQ	I/O	O	Interrupt output (configurable active HIGH or LOW), or GPIO.
27	MOSI	I/O	I	SPI data input pin (Master Out Slave In), or SDAT.

Pin Definitions (continued)

Pin Number	Name	Type	Default	Description
28	MISO	I/O	Z	SPI data output pin (Master In Slave Out), or GPIO (in SPI 3-pin mode). Tri-states when SPI 3PIN = 0 and SS is deasserted.
29	XOUT	I/O	O	Buffered 0.75, 1.5, 3, 6, or 12 MHz clock or GPIO. Tri-states in sleep mode (configure as GPIO drive LOW).
30	NC	NC		Must be floating.
33	V_{IO}	Pwr		I/O interface voltage, 2.7–3.6 V.
34	RST	I	I	Device reset. Internal 10 kΩ pull down resistor. Active HIGH, connect through a 0.47 µF capacitor to V_{BAT}. Must have RST = 1 event the first time power is applied to the radio. Otherwise the state of the radio control registers is unknown.
35	V_{DD}	Pwr		Decoupling pin for 1.8 V logic regulator, connect through a 0.47 µF capacitor to GND.
37	GND	GND		Must be connected to ground.
E-PAD	GND	GND		Must be soldered to ground.

Functional Overview

The CYRF6986 IC provides a complete WirelessUSB SPI to antenna wireless MODEMs. The SoC is designed to implement wireless device links operating in the worldwide 2.4 GHz ISM frequency band. It is intended for systems compliant with worldwide regulations covered by ETSI EN 301 489-1 V1.41, ETSI EN 300 328-1 V1.3.1 (Europe), FCC CFR 47 Part 15 (USA and Industry Canada), and TELEC ARIB_T66_March, 2003 (Japan).

The SoC contains a 2.4 GHz, 1 Mbps GFSK radio transceiver, packet data buffering, packet framer, DSSS baseband controller, Received Signal Strength Indication (RSSI), and SPI interface for data transfer and device configuration.

The radio supports 98 discrete 1 MHz channels (regulations may limit the use of some of these channels in certain jurisdictions).

The baseband performs DSSS spreading/despreading, Start of Packet (SOP), End of Packet (EOP) detection, and CRC16 generation and checking. The baseband may also be configured to automatically transmit Acknowledge (ACK) handshake packets whenever a valid packet is received.

When in receive mode, with packet framing enabled, the device is always ready to receive data transmitted at any of the supported bit rates. This enables the implementation of mixed-rate systems in which different devices use different data rates. This also enables the implementation of dynamic data rate systems that use high data rates at shorter distances or in a low-moderate interference environment or both. It changes to lower data rates at longer distances or in high interference environments or both.

Data Transmission Modes

The SoC supports two different data transmission modes:

- In GFSK mode, data is transmitted at 1 Mbps, without any DSSS.
- In DSSS mode eight bits (8DR, 32-chip) are encoded in each derived code symbol transmitted, resulting in effective 250 kbps data rate.

32-chip pseudo noise (PN) codes are supported. The two data transmission modes apply to the data after the SOP. In particular the length, data, and CRC16 are all sent in the same mode. In general, DSSS reduce packet error rate in any given environment.

Link Layer Modes

The CYRF6986 IC device supports the following data packet framing features:

SOP

Packets begin with a two-symbol SoP marker. If framing is disabled then an SOP event is inferred whenever two successive correlations are detected. The SOP_CODE_ADR code used for the SOP is different from that used for the “body” of the packet, and if desired may be a different length. SOP must be configured to be the same length on both sides of the link.

Length

Length field is the first eight bits after the SOP symbol, and is transmitted at the payload data rate. An EoP condition is inferred after reception of the number of bytes defined in the length field, plus two bytes for the CRC16.

CRC16

The device may be configured to append a 16 bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver verifies the calculated CRC16 for the payload data against the received value in the CRC16 field. The seed value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed; the received data CRC16 is checked against both the configured and zero CRC16 seeds.

CRC16 detects the following errors:

- Any one bit in error.
- Any two bits in error (irrespective of how far apart, which column, and so on).

- Any odd number of bits in error (irrespective of the location).
- An error burst as wide as the checksum itself.

Figure 2 shows an example packet with SOP, CRC16, and lengths fields enabled, and Figure 3 shows a standard ACK packet.

Figure 2. Example Packet Format

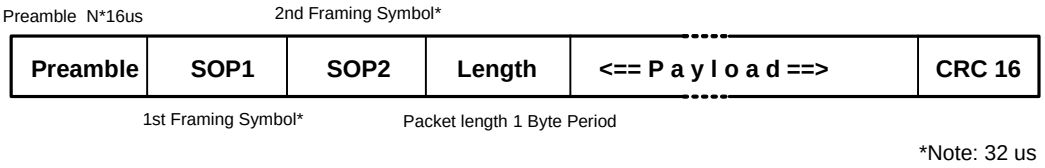
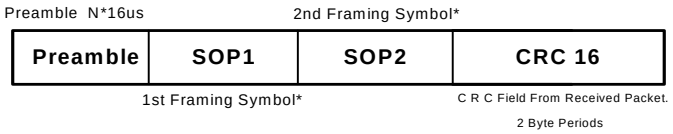


Figure 3. Example ACK Packet Format



Packet Buffers

All data transmission and reception use the 16 byte packet buffers - one for transmission and one for reception.

The transmit buffer allows loading a complete packet of up to 16 bytes of payload data in one burst SPI transaction. This is then transmitted with no further MCU intervention. Similarly, the receive buffer allows receiving an entire packet of payload data up to 16 bytes with no firmware intervention required until the packet reception is complete.

The CYRF6986 IC supports packets up to 255 bytes. However, the actual maximum packet length depends on the accuracy of the clock on each end of the link and the data mode. Interrupts are provided to allow an MCU to use the transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the MCU can load 16 bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the MCU must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

Auto Transaction Sequencer (ATS)

The CYRF6986 IC provides automated support for transmission and reception of acknowledged data packets.

When transmitting in transaction mode, the device automatically:

- Starts the crystal and synthesizer
- Enters transmit mode
- Transmits the packet in the transmit buffer
- Transitions to receive mode and waits for an ACK packet
- Transitions to the transaction end state when an ACK packet is received or a timeout period expires

Similarly, when receiving in transaction mode, the device automatically:

- Waits in receive mode for a valid packet to be received
- Transitions to transmit mode, transmits an ACK packet
- Transitions to the transaction end state (receive mode to await the next packet, and so on.)

The contents of the packet buffers are not affected by the transmission or reception of ACK packets.

In each case, the entire packet transaction takes place without any need for MCU firmware action (as long as packets of 16 bytes or less are used). To transmit data, the MCU must load the data packet to be transmitted, set the length, and set the TX GO bit. Similarly, when receiving packets in transaction mode, firmware must retrieve the fully received packet in response to an interrupt request indicating reception of a packet.

Data Rates

The CYRF6986 IC supports the following data rates by combining the PN code lengths and data transmission modes described in the previous sections:

- 1000 kbps (GFSK)
- 250 kbps (32 chip 8DR)

Functional Block Overview

2.4 GHz Radio

The radio transceiver is a dual conversion low IF architecture optimized for power, range, and robustness. The radio employs channel-matched filters to achieve high performance in the presence of interference. An integrated Power Amplifier (PA) provides up to 0 dBm transmit power, with an output power

control range of 35 dB in six steps. The supply current of the device is reduced as the RF output power is reduced.

Table 1. Internal PA Output Power Step Table

PA Setting	Typical Output Power (dBm)
6	0
5	–5
4	–13
3	–18
2	–24
1	–30
0	–35

Frequency Synthesizer

Before transmission or reception may begin, the frequency synthesizer must settle. The settling time varies depending on channel; 25 fast channels are provided with a maximum settling time of 100 µs.

The 'fast channels' (less than 100 µs settling time) are every third channel, starting at 0 up to and including 72 (for example, 0, 3, 6, 9 …. 69, 72).

Baseband and Framer

The baseband and framer blocks provide the DSSS encoding and decoding, SOP generation and reception, CRC16 generation and checking, and EOP detection and length field.

Packet Buffers and Radio Configuration Registers

Packet data and configuration registers are accessed through the SPI interface. All configuration registers are directly addressed through the address field in the SPI packet. Configuration registers allow configuration of DSSS PN codes, data rate, operating mode, interrupt masks, interrupt status, and so on.

SPI Interface

The CYRF6986 IC has an SPI interface supporting communication between an application MCU and one or more slave devices (including the CYRF6986). The SPI interface supports single-byte and multi-byte serial transfers using either 4-pin or 3-pin interfacing. The SPI communications interface consists of Slave Select ($\overline{SS}$), Serial Clock (SCK), Master Out-Slave In (MOSI), Master In-Slave Out (MISO), or Serial Data (SDAT).

SPI communication may be described as the following:

- Command Direction (bit 7) = '1' enables SPI write transaction. A '0' enables SPI read transactions.
- Command Increment (bit 6) = '1' enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access. Otherwise the same address is accessed.
- Six bits of address
- Eight bits of data

The device receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active LOW Slave Select ($\overline{SS}$) pin must be asserted to initiate an SPI transfer.

The application MCU can initiate SPI data transfers using a multi-byte transaction. The first byte is the Command/Address byte, and the following bytes are the data bytes shown in Table 2 through Figure 6 on page 7.

The SPI communications interface has a burst mechanism, where the first byte can be followed by as many data bytes as required. A burst transaction is terminated by deasserting the slave select ($\overline{SS}$ = 1).

The SPI communications interface single read and burst read sequences are shown in Figure 4 on page 7 and Figure 5 on page 7, respectively.

The SPI communications interface single write and burst write sequences are shown in Figure 6 on page 7 and Figure 7 on page 7, respectively.

This interface may be optionally operated in a 3-pin mode with the MISO and MOSI functions combined in a single bidirectional data pin (SDAT). When using 3-pin mode, user firmware must ensure that the MOSI pin on the MCU is in a high impedance state except when MOSI is actively transmitting data.

The device registers may be written to or read from one byte at a time, or several sequential register locations may be written or read in a single SPI transaction using incrementing burst mode. In addition to single byte configuration registers, the device includes register files. Register files are FIFOs written to and read from using nonincrementing burst SPI transactions.

The IRQ pin function may be optionally multiplexed onto the MOSI pin. When this option is enabled, the IRQ function is not available while the $\overline{SS}$ pin is LOW. When using this configuration, user firmware must ensure that the MOSI pin on the MCU is in a high impedance state whenever the $\overline{SS}$ pin is HIGH.

The SPI interface is not dependent on the internal 12 MHz clock. Registers may therefore be read from or written to when the device is in sleep mode, and the 12 MHz oscillator disabled.

The SPI interface and the IRQ and RST pins have a separate voltage reference pin (V_{IO}). This enables the device to interface directly to MCUs operating at voltages below the CYRF6986 IC supply voltage.

Table 2. SPI Transaction Format

Parameter	Byte 1			Byte 1+N
Bit #	7	6	[5:0]	[7:0]
Bit Name	DIR	INC	Address	Data

Figure 4. SPI Single Read Sequence

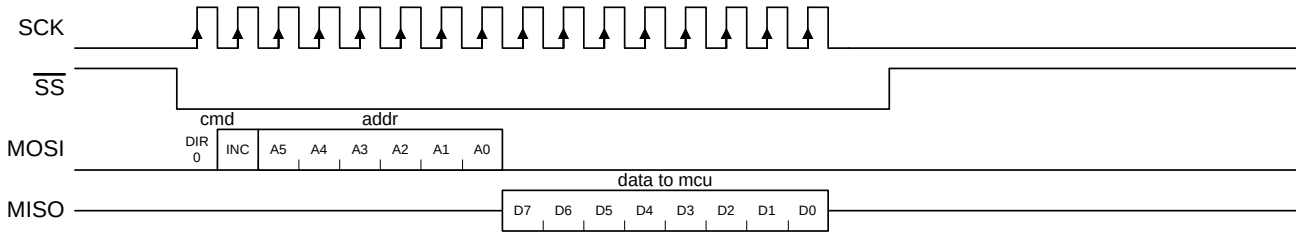


Figure 5. SPI Incrementing Burst Read Sequence

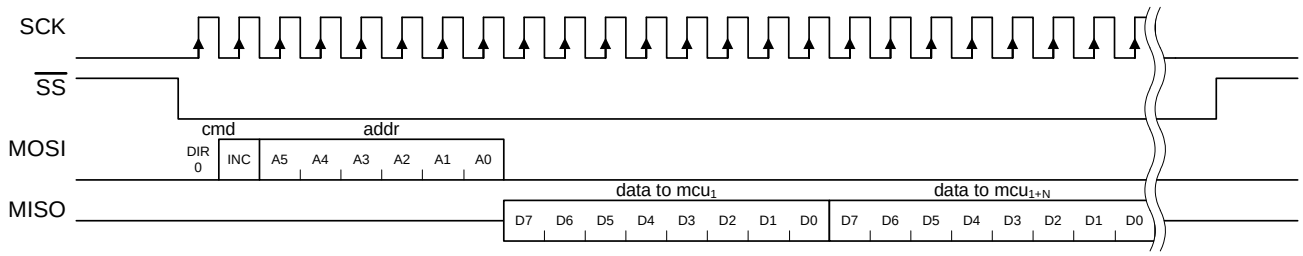


Figure 6. SPI Single Write Sequence

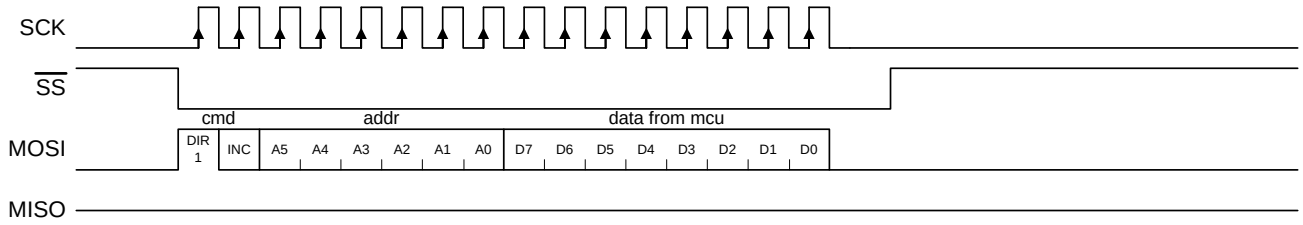
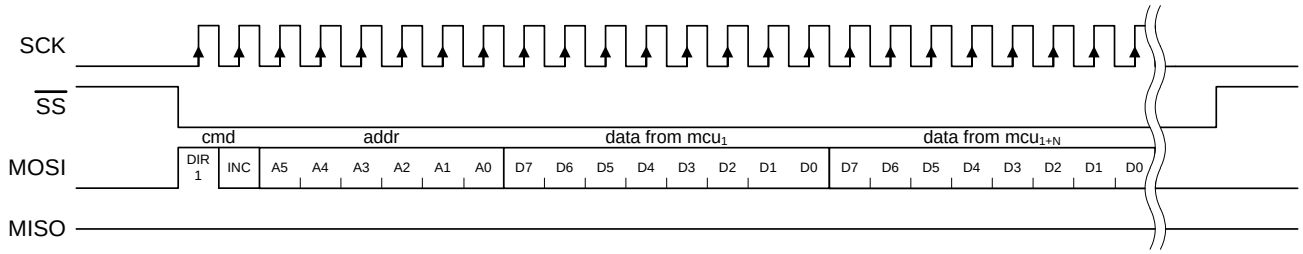


Figure 7. SPI Incrementing Burst Write Sequence



Interrupts

The device provides an interrupt (IRQ) output, which is configurable to indicate the occurrence of various different events. The IRQ pin may be programmed to be either active HIGH or active LOW, and be either a CMOS or open drain output. The available interrupts are described in the section Registers on page 11.

The CYRF6986 IC features three sets of interrupts: transmit, receive, and system interrupts. These interrupts all share a single pin (IRQ), but can be independently enabled or disabled. The contents of the enable registers are preserved when switching between transmit and receive modes.

If more than one interrupt is enabled at any time, it is necessary to read the relevant status register to determine which event caused the IRQ pin to assert. Even when a given interrupt source is disabled, the status of the condition that would otherwise cause an interrupt can be determined by reading the appropriate status register. It is therefore possible to use the devices without the IRQ pin, by polling the status registers to wait for an event, rather than using the IRQ pin.

Clocks

A 12 MHz crystal (30 ppm or better) is directly connected between XTAL and GND without the need for external capacitors. A digital clock out function is provided, with selectable output frequencies of 0.75, 1.5, 3, 6, or 12 MHz. This output may be used to clock an external microcontroller (MCU) or ASIC. This output is enabled by default, but may be disabled.

The requirements to directly connect the crystal to the XTAL pin and GND are:

- Nominal Frequency: 12 MHz
- Operating Mode: Fundamental Mode
- Resonance Mode: Parallel Resonant
- Frequency Stability: ±30 ppm
- Series Resistance: ≤60 ohms
- Load Capacitance: 10 pF
- Drive Level: 100 µW

Power Management

The operating voltage of the device is 2.7 V to 3.6 V DC, which is applied to the V_{BAT} pin. The device can be shut down to a fully static sleep mode by writing to the FRC END = 1 and END STATE = 000 bits in the XACT_CFG_ADR register over the SPI interface. The device enters sleep mode within 35 µs after the last SCK positive edge at the end of this SPI transaction. Alternatively, the device may be configured to automatically enter sleep mode after completing the packet transmission or reception. When in sleep mode, the on-chip oscillator is stopped, but the SPI interface remains functional. The device wakes from sleep mode automatically when the device is commanded to enter transmit or receive mode. When resuming from sleep mode, there is a short delay while the oscillator restarts. The device can be configured to assert the IRQ pin when the oscillator has stabilized.

Low Noise Amplifier and Received Signal Strength Indication

The gain of the receiver can be controlled directly by clearing the AGC EN bit and writing to the Low Noise Amplifier (LNA) bit of the RX_CFG_ADR register. Clearing the LNA bit reduces the receiver gain approximately 20 dB, allowing accurate reception of very strong received signals (for example, when operating a receiver very close to the transmitter). Approximately 30 dB of receiver attenuation can be added by setting the Attenuation (ATT) bit. This limits data reception to devices at very short ranges. Disabling AGC and enabling LNA is recommended, unless receiving from a device using external PA.When the device is in receive mode the RSSI_ADR register returns the relative signal strength of the on-channel signal power.

When receiving, the device automatically measures and stores the relative strength of the signal being received as a five bit value. An RSSI reading is taken automatically when the SoP is detected. In addition, a new RSSI reading is taken every time the previous reading is read from the RSSI_ADR register, allowing the background RF energy level on any given channel to be easily measured when RSSI is read while no signal is being received. A new reading can occur as fast as once every 12 µs. received.

Application Example

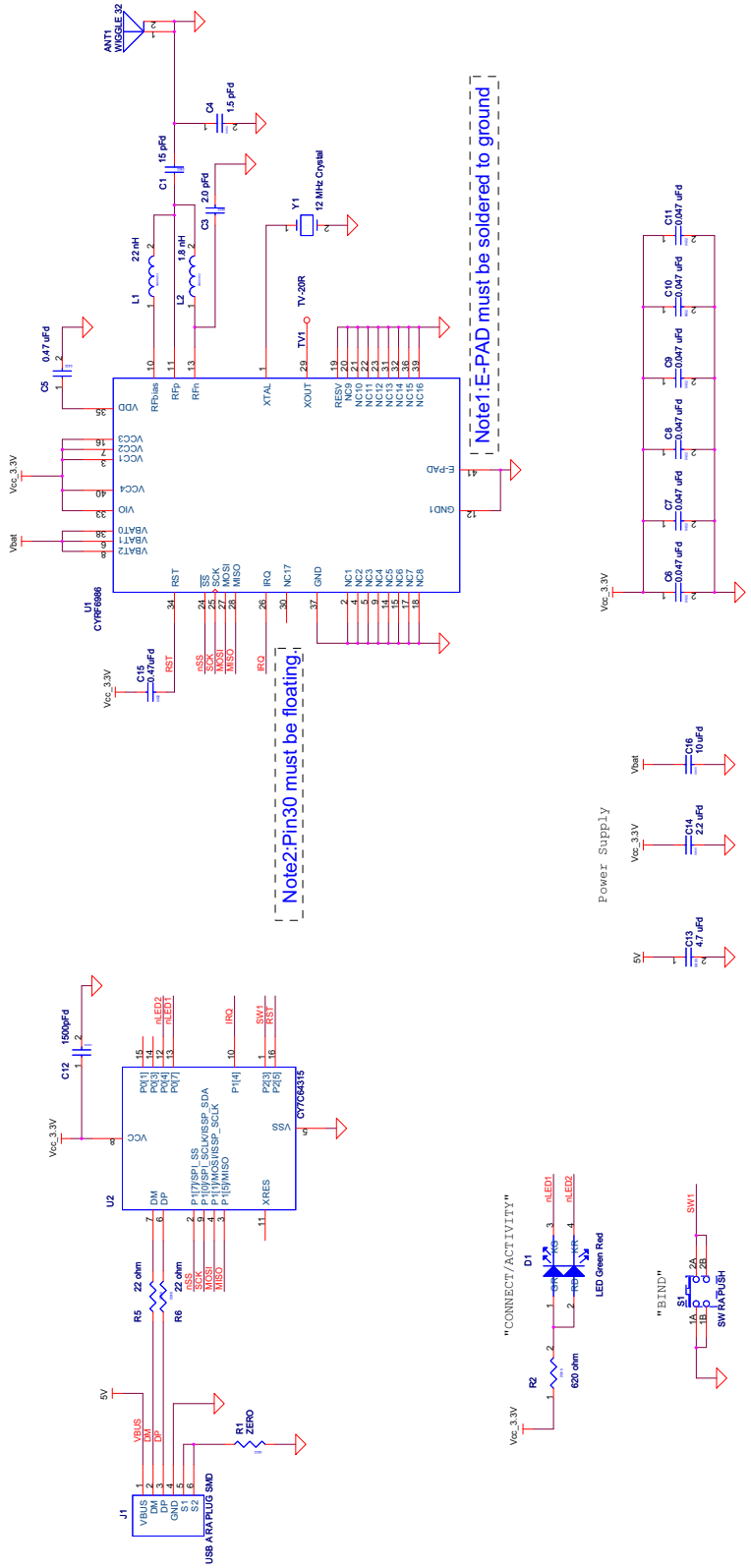


Table 3. Recommended BoM

Item	Qty	CY Part Number	Reference	Description	Manufacturer	Mfr Part Number
1	1	NA	ANT1	2.5 GHz H-STUB WIGGLE ANTENNA FOR 32 MIL PCB	NA	NA
2	1	730-10012	C1	CAP 15 pF 50 V CERAMIC NPO 0402	Panasonic	ECJ-0EC1H150J
3	1	730-11955	C3	CAP 2.0 pF 50 V CERAMIC NPO 0402	Kemet	C0402C209C5GACTU
4	1	730-11398	C4	CAP 1.5 pF 50 V CERAMIC NPO 0402 SMD	PANASONIC	ECJ-0EC1H1R5C
5	1	730-13322	C5, C15	CAP 0.47 uF 6.3 V CERAMIC X5R 0402	Murata	GRM155R60J474KE19D
6	6	730-13404	C6,C7,C8,C9,C10,C11	CAP 0.047 uF 16 V CERAMIC X5R 0402	AVX	0402YD473KAT2A
7	1	730-11953	C12	CAP 1500 pF 50 V CERAMIC X7R 0402	Kemet	C0402C152K5RACTU
8	1	730-13040	C13	CAP CERAMIC 4.7 uF 6.3 V XR5 0805	Kemet	C0805C475K9PACTU
9	1	730-12003	C14	CAP CER 2.2 uF 10 V 10% X7R 0805	Murata Electronics North America	GRM21BR71A225KA01L
10	1	NA	C16	CAP CERAMIC 10 uF 6.3 V XR5 0805	NA	NA
11	1	800-13333	D1	LED GREEN/RED BICOLOR 1210 SMD	LITEON	LTST-C155KGJRKT
12	1	420-13046	J1	CONN USB PLUG TYPE A PCB SMT	ACON	UAR72-4N5J10
13	1	800-13401	L1	INDUCTOR 22NH 2% FIXED 0603 SMD	Panasonic - ECG	ELJ-RE22NGF2
14	1	800-11651	L2	INDUCTOR 1.8NH +-.3NH FIXED 0402 SMD	Panasonic - ECG	ELJ-RF1N8DF
15	1	610-10343	R1	RES ZERO ohm 1/16W 0402 SMD	Panasonic - ECG	ERJ-2GE0R00X
16	1	610-13472	R2	RES CHIP 620 ohm 1/16W 5% 0402 SMD	Panasonic - ECG	ERJ-2GEJ621X
17	1	200-13471	S1	SWITCH LT 3.5 mm x 2.9mm 160GF SMD	Panasonic - ECG	EVQ-P7J01K
18	1	CYRF6986-40LFC	U1	IC, LPstar 2.4 GHz RADIO SoC QFN-40	Cypress Semiconductor	CYRF6986
19	1	CY7C64315	U2	IC enCoRe V FULL-SPEED USB CONTROLLER	Cypress Semiconductor	CY7C64315
20	1	800-13259	Y1	CRYSTAL 12.00 MHz HC49 SMD	eCERA	GF-1200008
21	1	xxx-xxxx-x	PCB	PRINTED CIRCUIT BOARD	Cypress Semiconductor	xxx-xxxx-x

Registers

All registers are read and writable, except where noted. Registers may be written to or read from individually or in sequential groups.[1, 2]

Table 4. Register Map Summary

Address	Mnemonic	b7	b6	b5	b4	b3	b2	b1	b0	Default[1]	Access[1]
0x00	CHANNEL_ADR	Not Used	Channel							-1001000	-bbbbbbb
0x01	TX_LENGTH_ADR	TX Length								00000000	bbbbbbbb
0x02	TX_CTRL_ADR	TX GO	TX CLR	TXB15 IRQEN	TXB8 IRQEN	TXB0 IRQEN	TXBERR IRQEN	TXC IRQEN	TXE IRQEN	00000011	bbbbbbbb
0x03	TX_CFG_ADR	Not Used	Not Used	DATA CODE LENGTH	RSVD	Data mode	PA SETTING			--000101	--bbbbbb
0x04	TX_IRQ_STATUS_ADR	OS IRQ	RSVD	TXB15 IRQ	TXB8 IRQ	TXB0 IRQ	TXBERR IRQ	TXC IRQ	TXE IRQ	--------	rrrrrrrr
0x05	RX_CTRL_ADR	RX GO	RSVD	RXB16 IRQEN	RXB8 IRQEN	RXB1 IRQEN	RXBERR IRQEN	RXC IRQEN	RXE IRQEN	00000111	bbbbbbbb
0x06	RX_CFG_ADR	AGC EN	LNA	ATT	HILO	FAST TURN EN	Not Used	RXOW EN	VLD EN	10010-10	bbbbb-bb
0x07	RX_IRQ_STATUS_ADR	RXOW IRQ	SOPDET IRQ	RXB16 IRQ	RXB8 IRQ	RXB1 IRQ	RXBERR IRQ	RXC IRQ	RXE IRQ	--------	brrrrrrr
0x08	RX_STATUS_ADR	RX ACK	PKT ERR	EOP ERR	CRC0	Bad CRC	RX Code	RX Data Mode		--------	rrrrrrrr
0x09	RX_COUNT_ADR	RX Count								00000000	rrrrrrrr
0x0A	RX_LENGTH_ADR	RX Length								00000000	rrrrrrrr
0x0B	PWR_CTRL_ADR	**The firmware should set "00010000" to this register while initiating**								10100000	bbbbbbbb
0x0C	XTAL_CTRL_ADR	XOUT FN		XSIRQ EN	Not Used	Not Used	FREQ			000--100	bbb--bbb
0x0D	IO_CFG_ADR	IRQ OD	IRQ POL	MISO OD	XOUT OD	RSVD	RSVD	SPI 3PIN	IRQ GPIO	00000000	bbbbbbbb
0x0E	GPIO_CTRL_ADR	XOUT OP	MISO OP	RSVD	IRQ OP	XOUT IP	MISO IP	RSVD	IRQ IP	0000----	bbbbrrrr
0x0F	XACT_CFG_ADR	ACK EN	Not Used	FRC END	END STATE			ACK TO		1-000000	b-bbbbbb
0x10	FRAMING_CFG_ADR	SOP EN	SOP LEN	LEN EN	SOP TH					10100101	bbbbbbbb
0x11	DATA32_THOLD_ADR	Not Used	Not Used	Not Used	Not Used	TH32				----0100	----bbbb
0x12	DATA64_THOLD_ADR	Not Used	Not Used	Not Used	TH64					---01010	---bbbbb
0x13	RSSI_ADR	SOP	Not Used	LNA	RSSI					0-100000	r-rrrrrr
0x14	EOP_CTRL_ADR[3]	HEN	HINT		EOP					10100100	bbbbbbbb
0x15	CRC_SEED_LSB_ADR	CRC SEED LSB								00000000	bbbbbbbb
0x16	CRC_SEED_MSB_ADR	CRC SEED MSB								00000000	bbbbbbbb
0x17	TX_CRC_LSB_ADR	CRC LSB								--------	rrrrrrrr
0x18	TX_CRC_MSB_ADR	CRC MSB								--------	rrrrrrrr
0x19	RX_CRC_LSB_ADR	CRC LSB								11111111	rrrrrrrr
0x1A	RX_CRC_MSB_ADR	CRC MSB								11111111	rrrrrrrr
0x1B	TX_OFFSET_LSB_ADR	STRIM LSB								00000000	bbbbbbbb
0x1C	TX_OFFSET_MSB_ADR	Not Used	Not Used	Not Used	Not Used	STRIM MSB				----0000	----bbbb
0x1D	MODE_OVERRIDE_ADR	RSVD	RSVD	FRC SEN	FRC AWAKE		Not Used	Not Used	RST	00000--0	wwwww--w
0x1E	RX_OVERRIDE_ADR	ACK RX	RXTX DLY	MAN RXACK	FRC RXDR	DIS CRC0	DIS RXCRC	ACE	Not Used	0000000-	bbbbbbb-
0x1F	TX_OVERRIDE_ADR	ACK TX	FRC PRE	RSVD	MAN TXACK	OVRD ACK	DIS TXCRC	RSVD	TX INV	00000000	bbbbbbbb
0x26	XTAL_CFG_ADR	RSVD	RSVD	RSVD	RSVD	START DLY	RSVD	RSVD	RSVD	00000000	wwwwwwww
0x27	CLK_OVERRIDE_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww
0x28	CLK_EN_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RXF	RSVD	00000000	wwwwwwww
0x29	RX_ABORT_ADR	RSVD	RSVD	ABORT EN	RSVD	RSVD	RSVD	RSVD	RSVD	00000000	wwwwwwww
0x32	AUTO_CAL_TIME_ADR	AUTO_CAL_TIME								00000011	wwwwwwww
0x35	AUTO_CAL_OFFSET_ADR	AUTO_CAL_OFFSET								00000000	wwwwwwww
0x39	ANALOG_CTRL_ADR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RX INV	ALL SLOW	00000000	wwwwwwww
Register Files											
0x20	TX_BUFFER_ADR	TX Buffer File								--------	wwwwwwww
0x21	RX_BUFFER_ADR	RX Buffer File								--------	rrrrrrrr
0x22	SOP_CODE_ADR	SOP Code File								Note 4	bbbbbbbb
0x23	DATA_CODE_ADR	Data Code File								Note 5	bbbbbbbb
0x24	PREAMBLE_ADR	Preamble File								Note 6	bbbbbbbb
0x25	MFG_ID_ADR	MFG ID File								NA	rrrrrrrr

Notes
1. b = read/write; r = read only; w = write only; '-' = not used, default value is undefined.
2. Registers must be configured or accessed only when the radio is in IDLE or SLEEP mode. The GPIOs, and RSSI registers can be accessed in Active Tx and Rx mode.
3. EOP_CTRL_ADR[6:4] must never have the value of "000", that is, EOP Hint Symbol count must never be "0"
4. SOP_CODE_ADR default = 0x17FF9E213690C782.
5. DATA_CODE_ADR default = 0x02F9939702FA5CE3012BF1DB0132BE6F.
6. PREAMBLE_ADR default = 0x333302.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on any power supply pin relative to V_{SS} .....–0.3 V to +3.9 V

DC voltage to logic inputs [8] ..... –0.3 V to V_{IO} +0.3 V

DC voltage applied to outputs in High-Z State ..... –0.3 V to V_{IO} +0.3 V

Static discharge voltage (Digital) [9] .....>2000 V

Static discharge voltage (RF) [9] ..... 1100 V

Latch-up current .....+200 mA, –200 mA

Operating Conditions

V_{CC} ..... 2.7 V to 3.6 V

V_{IO} .....2.7 V to 3.6 V

V_{BAT} .....2.7 V to 3.6 V

T_A (Ambient Temperature Under Bias) ..... 0 °C to +70 °C

Ground Voltage ..... 0 V

F_{OSC} (Crystal Frequency) ..... 12 MHz ±30 ppm

DC Characteristics

(T = 25 °C, V_{BAT} = 2.7 V, f_{OSC} = 12.000000 MHz)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery Voltage	0–70 °C	2.7	–	3.6	V
V_{IO}[10]	V_{IO} Voltage		2.7	–	3.6	V
V_{CC}	V_{CC} Voltage	0–70 °C	2.7	–	3.6	V
V_{OH1}	Output High Voltage Condition 1	At I_{OH} = –100.0 µA	V_{IO} – 0.2	V_{IO}	–	V
V_{OH2}	Output High Voltage Condition 2	At I_{OH} = –2.0 mA	V_{IO} – 0.4	V_{IO}	–	V
V_{OL}	Output Low Voltage	At I_{OL} = 2.0 mA	–	0	0.45	V
V_{IH}	Input High Voltage		0.7 × V_{IO}		V_{IO}	V
V_{IL}	Input Low Voltage		0		0.3 × V_{IO}	V
I_{IL}	Input Leakage Current	0 < V_{IN} < V_{IO}	–1	0.26	+1	µA
C_{IN}	Pin Input Capacitance	except XTAL, RF_N, RF_P, RF_{BIAS}	–	3.5	10	pF
I_{CC} (GFSK)[11]	Average TX I_{CC}, 1 Mbps, slow channel	PA = 5, 2 way, 4 bytes/10 ms	–	0.87	–	mA
I_{CC} (32-8DR)[11]	Average TX I_{CC}, 250 kbps, fast channel	PA = 5, 2 way, 4 bytes/10 ms	–	1.2	–	mA
I_{SB}[12]	Sleep Mode I_{CC}		–	0.8	10	µA
IDLE I_{CC}	Radio off, XTAL Active	XOUT disabled	–	1.0	–	mA
I_{synth}	I_{CC} during Synth Start		–	8.4	–	mA
TX I_{CC}	I_{CC} during Transmit	PA = 5 (–5 dBm)	–	20.8	–	mA
TX I_{CC}	I_{CC} during Transmit	PA = 6 (0 dBm)	–	26.2	–	mA
RX I_{CC}	I_{CC} during Receive	LNA off, ATT on	–	18.4	–	mA
RX I_{CC}	I_{CC} during Receive	LNA on, ATT off	–	21.2	–	mA

Notes

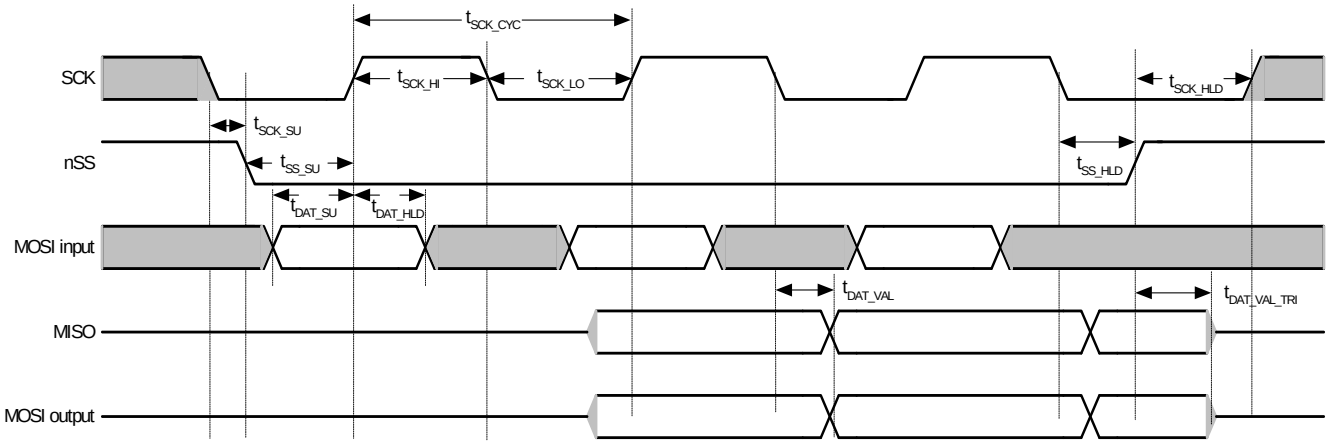
8. It is permissible to connect voltages above V_{IO} to inputs through a series resistor limiting input current to 1 mA. AC timing not guaranteed.
9. Human Body Model (HBM).
10. In sleep mode, the IO interface voltage reference is V_{BAT}.
11. Includes current drawn while starting crystal, starting synthesizer, transmitting packet (including SOP and CRC16), changing to receive mode, and receiving ACK handshake. Device is in sleep except during this transaction.
12. ISB is not guaranteed if any IO pin is connected to voltages higher than V_{IO}.

AC Characteristics

SPI Interface

Parameter [13, 14]	Description	Min	Typ	Max	Unit
t_{SCK_CYC}	SPI Clock Period	238.1	–	–	ns
t_{SCK_HI}	SPI Clock High Time	100	–	–	ns
t_{SCK_LO}	SPI Clock Low Time	100	–	–	ns
t_{DAT_SU}	SPI Input Data Setup Time	25	–	–	ns
t_{DAT_HLD}	SPI Input Data Hold Time	10	–	–	ns
t_{DAT_VAL}	SPI Output Data Valid Time	0	–	50	ns
$t_{DAT\_VAL\_TRI}$	SPI Output Data Tri-state (MOSI from Slave Select Deassert)	–	–	20	ns
t_{SS_SU}	SPI Slave Select Setup Time before first positive edge of SCK[15]	10	–	–	ns
t_{SS_HLD}	SPI Slave Select Hold Time after last negative edge of SCK	10	–	–	ns
t_{SS_PW}	SPI Slave Select Minimum Pulse Width	20	–	–	ns
t_{SCK_SU}	SPI Slave Select Setup Time	10	–	–	ns
t_{SCK_HLD}	SPI SCK Hold Time	10	–	–	ns
t_{RESET}	Minimum RST Pin Pulse Width	10	–	–	ns

Figure 8. SPI Timing



Notes
13. AC values are not guaranteed if voltage on any pin exceeding V_{IO}.
14. C_{LOAD} = 30 pF
15. SCK must start low at the time $\overline{SS}$ goes LOW, otherwise the success of SPI transactions are not guaranteed.

RF Characteristics

Table 5. Radio Parameters

Parameter Description	Conditions	Min	Typ	Max	Unit
RF Frequency Range	Note 19	2.400	–	2.497	GHz
Receiver (T = 25 °C, V_{CC} = V_{BAT} = 3.0 V, f_{OSC} = 12.000000 MHz, BER < 1E-3)					
Sensitivity 250 kbps 32-8DR	BER 1E-3	–	–90	–	dBm
Sensitivity GFSK	BER 1E-3, ALL SLOW = 1	–	–84	–	dBm
LNA Gain		–	22.8	–	dB
ATT Gain		–	–31.7	–	dB
Maximum Received Signal	LNA On	–15	–6	–	dBm
RSSI Value for PWR_{in} –60 dBm	LNA On	–	21	–	Count
RSSI Slope		–	1.9	–	dB/Count
Interference Performance (CER 1E-3)					
Co-channel Interference rejection Carrier-to-Interference (C/I)	C = –60 dBm	–	9	–	dB
Adjacent (±1 MHz) channel selectivity C/I 1 MHz	C = –60 dBm	–	3	–	dB
Adjacent (±2 MHz) channel selectivity C/I 2 MHz	C = –60 dBm	–	–30	–	dB
Adjacent (≥ 3 MHz) channel selectivity C/I ≥ 3 MHz	C = –67 dBm	–	–38	–	dB
Out-of-Band Blocking 30 MHz–12.75 MHz[20]	C = –67 dBm	–	–30	–	dBm
Inter modulation	C = –64 dBm, Δf = 5,10 MHz	–	–36	–	dBm
Receive Spurious Emission					
800 MHz	100 kHz ResBW	–	–79	–	dBm
1.6 GHz	100 kHz ResBW	–	–71	–	dBm
3.2 GHz	100 kHz ResBW	–	–65	–	dBm
Transmitter (T = 25 °C, V_{CC} = 3.0 V)					
Maximum RF Transmit Power	PA = 6	–2	0	+2	dBm
Maximum RF Transmit Power	PA = 5	–7	–5	–3	dBm
Maximum RF Transmit Power	PA = 0	–	–35		dBm
RF Power Control Range		–	35		dB
RF Power Range Control Step Size	Six steps, monotonic	–	5.6		dB
Frequency Deviation Min	PN Code Pattern 10101010	–	270		kHz
Frequency Deviation Max	PN Code Pattern 11110000	–	323		kHz
Error Vector Magnitude (FSK error)	>0 dBm	–	10	–	%rms
Occupied Bandwidth	–6 dBc, 100 kHz ResBW	500	876	–	kHz

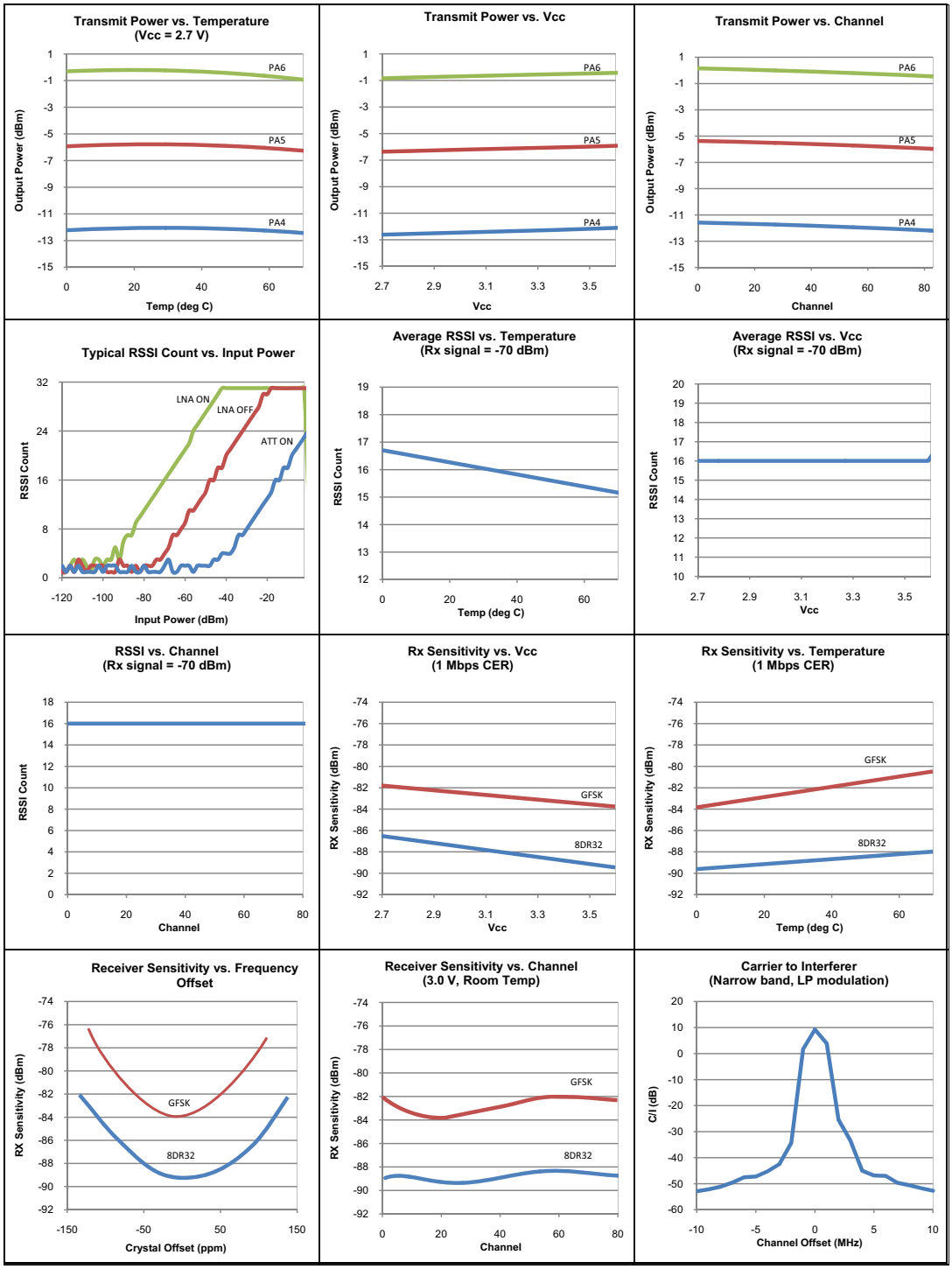
Notes
19. Subject to regulation.
20. Exceptions F/3 & 5C/3.

Table 5. Radio Parameters (continued)

Parameter Description	Conditions	Min	Typ	Max	Unit
Transmit Spurious Emission (PA = 6)					
In-band Spurious Second Channel Power (±2 MHz)		–	–38	–	dBm
In-band Spurious Third Channel Power (≥3 MHz)		–	–44	–	dBm
Non-Harmonically Related Spurs (800 MHz)		–	–38	–	dBm
Non-Harmonically Related Spurs (1.6 GHz)		–	–34	–	dBm
Non-Harmonically Related Spurs (3.2 GHz)		–	–47	–	dBm
Harmonic Spurs (Second Harmonic)		–	–43	–	dBm
Harmonic Spurs (Third Harmonic)		–	–48	–	dBm
Fourth and Greater Harmonics		–	–59	–	dBm
Power Management (Crystal PN# eCERA GF-1200008)					
Crystal Start to 10 ppm		–	0.7	1.3	ms
Crystal Start to IRQ	XSIRQ EN = 1	–	0.6	–	ms
Synth Settle	Slow channels	–	–	270	µs
Synth Settle	Medium channels	–	–	180	µs
Synth Settle	Fast channels	–	–	100	µs
Link Turnaround Time	GFSK	–	–	30	µs
Link Turnaround Time	250 kbps	–	–	62	µs
Max Packet Length	<60 ppm crystal-to-crystal	–	–	40	bytes

Typical Operating Characteristics

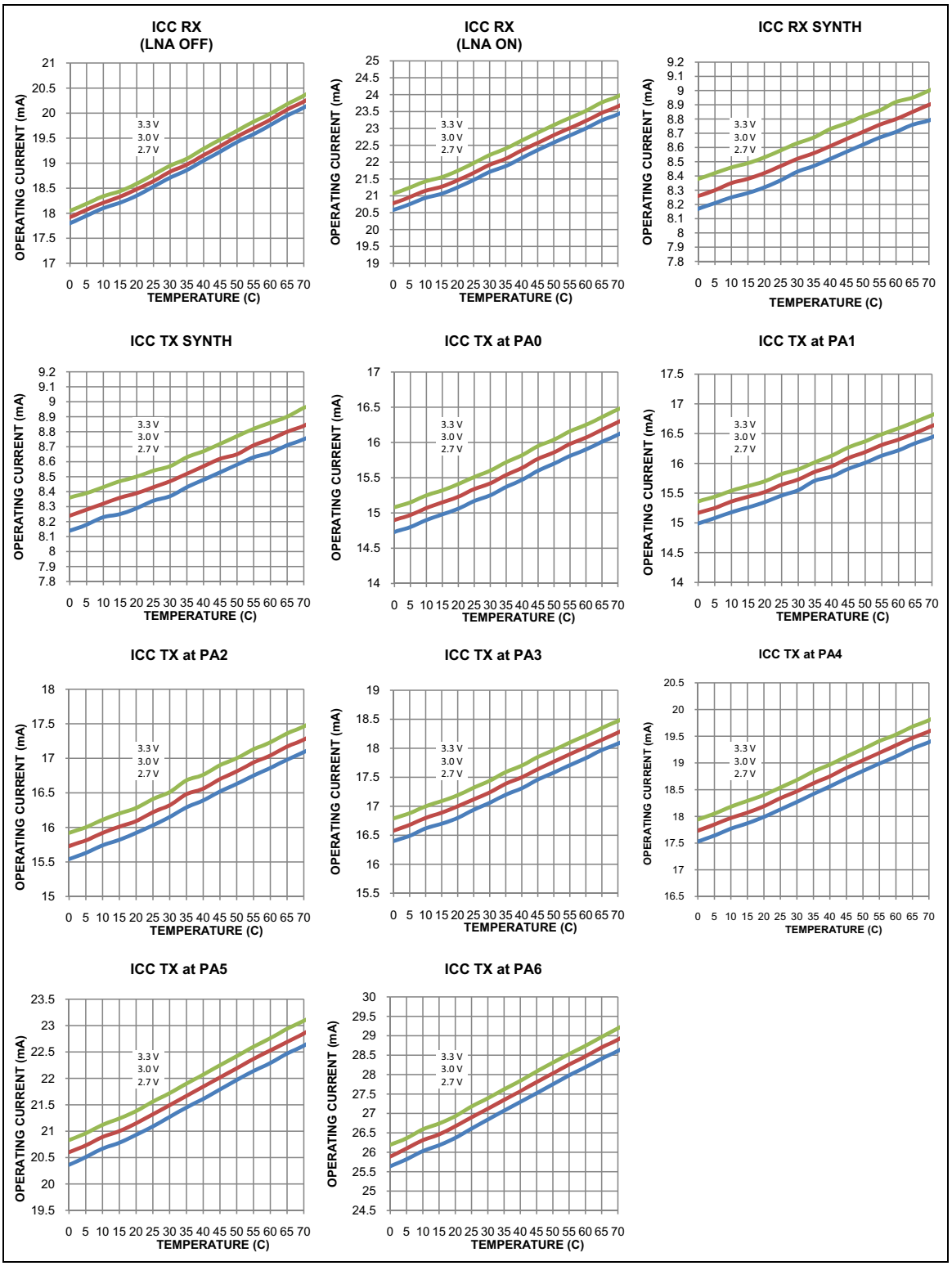
Figure 9. Typical Operating Characteristics [21]



Note

21. With LNA on, ATT off, above -2dBm erroneous RSSI values may be read. Cross-checking RSSI with LNA off/on is recommended for accurate readings.

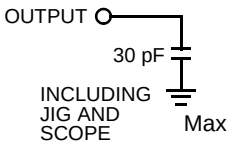
Typical Operating Characteristics (continued)

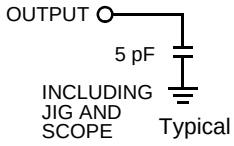


AC Test Loads and Waveforms for Digital Pins

Figure 10. AC Test Loads and Waveforms for Digital Pins

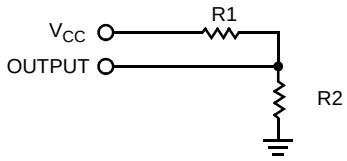
AC Test Loads

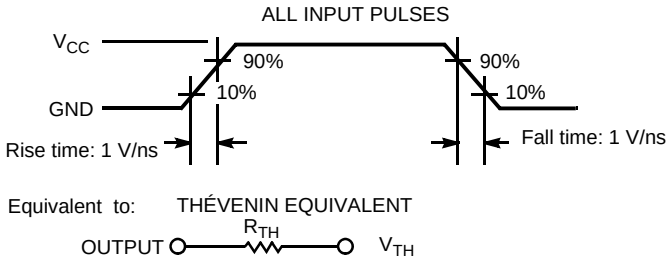


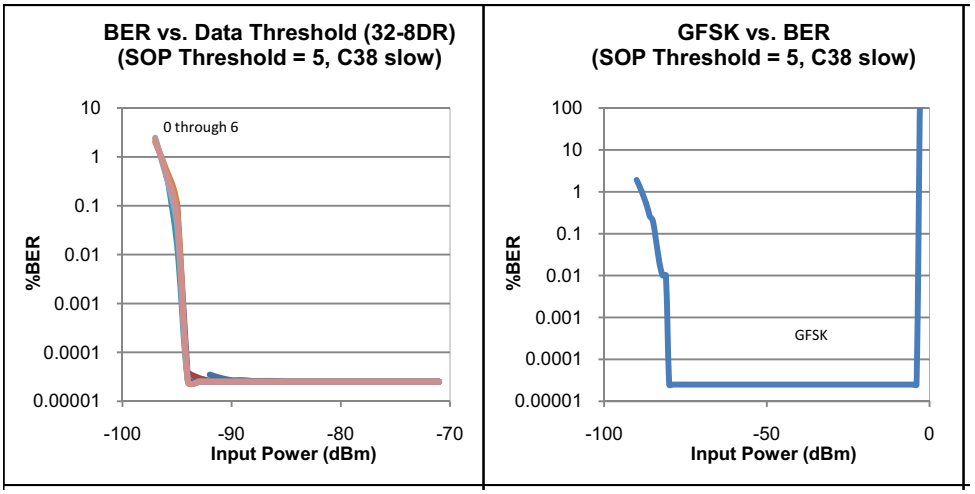


Parameter		Unit
R1	1071	Ω
R2	937	Ω
R_{TH}	500	Ω
V_{TH}	1.4	V
V_{CC}	3.00	V

DC Test Load





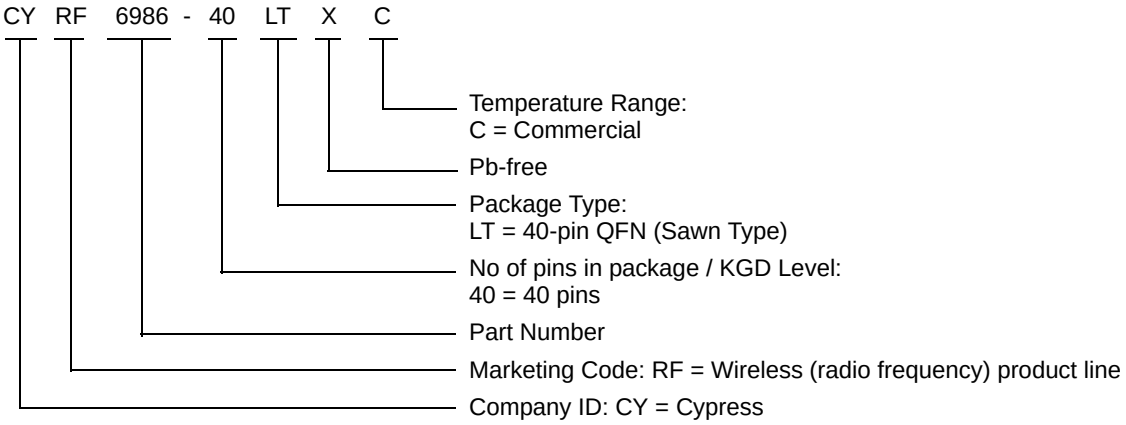


Ordering Information

Table 6. Key Feature and Package Information

Part Number	Radio	Package Name	Package Type	Operating Range
CYRF6986-40LTXC	Transceiver	001-44328	40-pin QFN (Sawn type)	Commercial

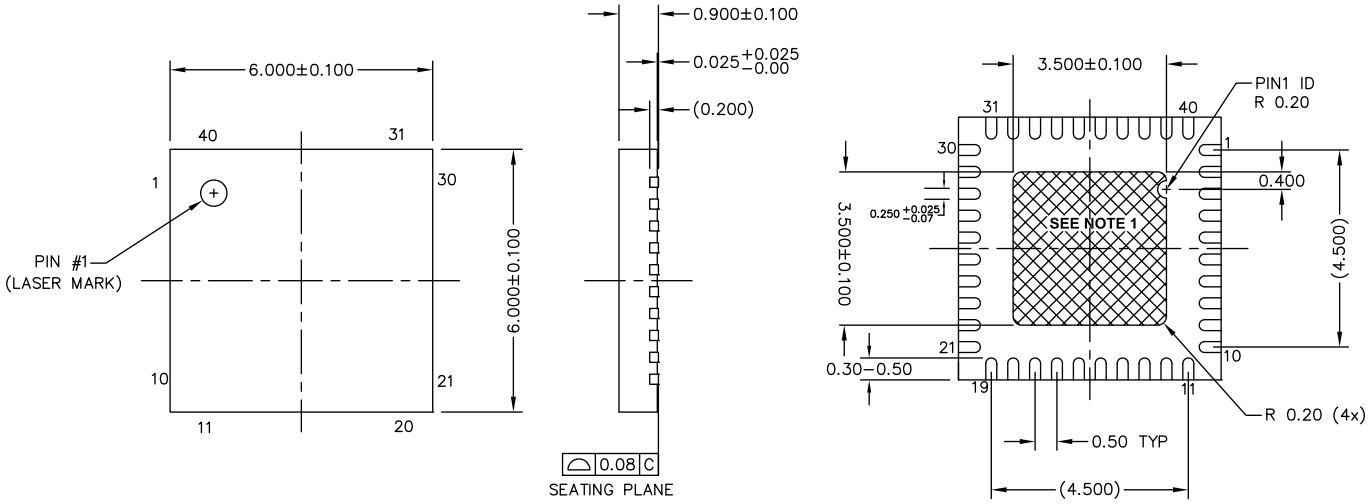
Ordering Code Definitions



Package Diagram

The recommended dimension of the PCB pad size for the E-PAD underneath the QFN is 3.5 mm × 3.5 mm (width × length).

Figure 11. 40-pin QFN (6 × 6 × 0.90 mm) 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-44328



NOTES:

1. HATCH IS SOLDERABLE EXPOSED AREA.
2. REFERENCE JEDEC #: MO−220
3. PACKAGE WEIGHT: 0.086g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-44328 *G

Acronyms

Table 7. Acronyms Used in this Document

Acronym	Description
ACK	Acknowledge (packet received, no errors)
BER	Bit Error Rate
BOM	Bill Of Materials
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
FEC	Forward Error Correction
FER	Frame Error Rate
GFSK	Gaussian Frequency-Shift Keying
HBM	Human Body Model
ISM	Industrial, Scientific, and Medical
IRQ	Interrupt Request
MCU	Microcontroller Unit
NRZ	Non Return to Zero
PLL	Phase Locked Loop
QFN	Quad Flat No-leads
RSSI	Received Signal Strength Indication
RF	Radio Frequency
Rx	Receive
Tx	Transmit

Document Conventions

Units of Measure

Table 8. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
dBc	decibel relative to carrier
dBm	decibel-milliwatt
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µs	microsecond
µV	microvolt
µVrms	microvolts root-mean-square
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
V	volt

Document History Page

Description Title: CYRF6986, WirelessUSB™ LPstar 2.4 GHz Radio SoC Document Number: 001-66073				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3139241	KKCN	01/14/2011	New data sheet.
*A	3170692	KKCN	02/11/2011	Updated to new template.
*B	3196461	KKCN	03/15/2011	Updated the text with LPstar.
*C	3333406	KPMD	08/01/2011	Changed status from Preliminary to Final.
*D	4237039	LIP	01/06/2014	Updated Package Diagram: spec 001-44328 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*E	5599939	CHYY	01/31/2017	Updated Package Diagram: spec 001-44328 – Changed revision from *F to *G. Updated to new template.
*F	5742403	SGUP	05/19/2017	Added watermark “Not recommended for new designs” across the document. Updated to new template.

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