

# FC6B22160L1

## Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

■ Features

- Low source-source ON resistance:  $R_{ss(on)}$  typ. = 4.9 mΩ (VGS = 3.8 V)
- CSP(Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

■ Marking Symbol: 36

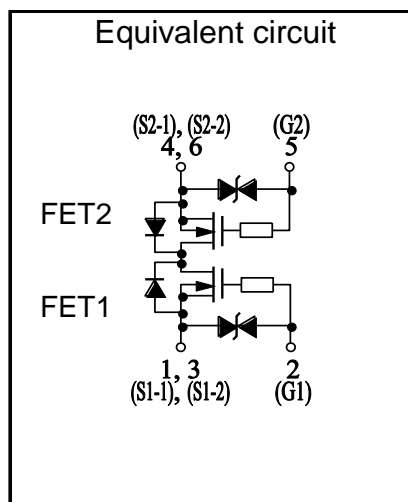
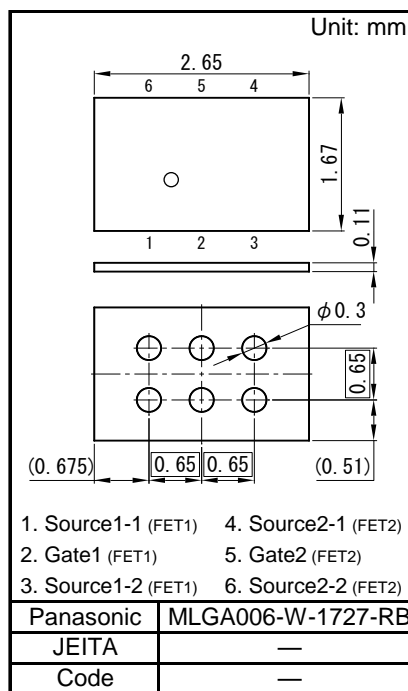
■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

| Parameter                 | Symbol              | Rating      | Unit |
|---------------------------|---------------------|-------------|------|
| Source-source Voltage     | VSS                 | 20          | V    |
| Gate-source Voltage       | VGS                 | ±8          | V    |
| Source Current            | DC <sup>*1</sup>    | IS1         | 8    |
|                           | DC <sup>*2</sup>    | IS2         | 17   |
|                           | Pulse <sup>*3</sup> | ISp         | 80   |
| Total Power Dissipation   | DC <sup>*1</sup>    | PD1         | 0.45 |
|                           | DC <sup>*2</sup>    | PD2         | 2.1  |
| Channel Temperature       | Tch                 | 150         | °C   |
| Storage Temperature Range | Tstg                | -55 to +150 | °C   |
| Thermal Resistance (ch-a) | DC <sup>*1</sup>    | Rth1        | 278  |
|                           | DC <sup>*2</sup>    | Rth2        | 59   |

- Note \*1 Mounted on FR4 board ( 25.4 mm × 25.4 mm × t1.0 mm )  
 using the minimum recommended pad size (36μm Copper ).  
 \*2 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm).  
 \*3 t = 10 μs, Duty Cycle ≤ 1 %



■ Electrical Characteristics Ta = 25 °C ± 3 °C

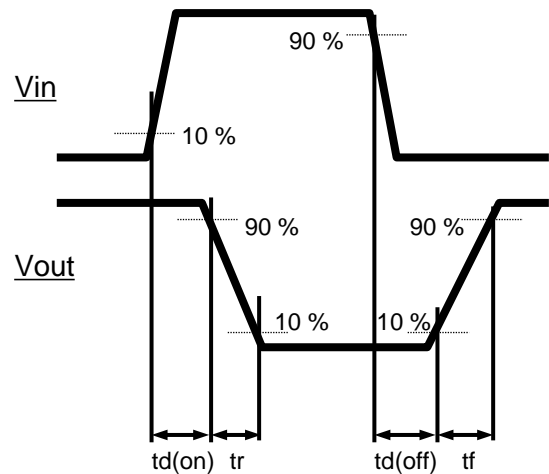
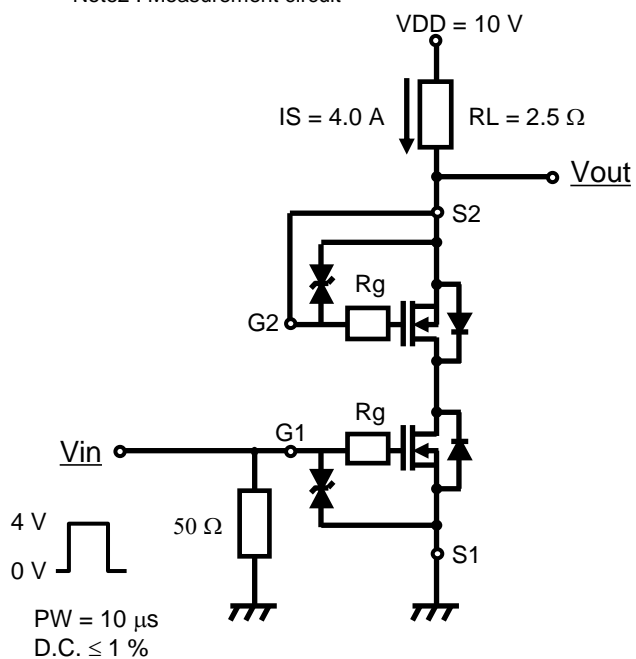
| Parameter                         | Symbol   | Conditions                       | Min  | Typ  | Max  | Unit |
|-----------------------------------|----------|----------------------------------|------|------|------|------|
| Source-source Breakdown Voltage   | VSSS     | IS = 1 mA, VGS = 0 V             | 20   |      |      | V    |
| Zero Gate Voltage Source Current  | ISSS     | VSS = 20 V, VGS = 0 V            |      |      | 1.0  | μA   |
| Gate-source Leakage Current       | IGSS     | VGS = ±8 V, VSS = 0 V            |      |      | ±10  | μA   |
|                                   |          | VGS = ±5 V, VSS = 0 V            |      |      | ±1.0 |      |
| Gate-source Threshold Voltage     | Vth      | IS = 1.1 mA, VSS = 10 V          | 0.35 | 0.90 | 1.4  | V    |
| Source-source On-state Resistance | RSS(on)1 | IS = 4.0 A, VGS = 4.5 V          | 3.5  | 4.7  | 6.2  | mΩ   |
|                                   | RSS(on)2 | IS = 4.0 A, VGS = 4.0 V          | 3.6  | 4.8  | 6.4  |      |
|                                   | RSS(on)3 | IS = 4.0 A, VGS = 3.8 V          | 3.7  | 4.9  | 6.6  |      |
|                                   | RSS(on)4 | IS = 4.0 A, VGS = 3.1 V          | 3.9  | 5.2  | 8.6  |      |
|                                   | RSS(on)5 | IS = 4.0 A, VGS = 2.5 V          | 4    | 6    | 11.8 |      |
| Body Diode Forward Voltage        | VF(s-s)  | IF = 4.0 A, VGS = 0 V            |      | 0.8  | 1.2  | V    |
| Input Capacitance *1              | Ciss     | VSS = 10 V, VGS = 0 V, f = 1 MHz |      | 3250 |      | pF   |
| Output Capacitance *1             | Coss     |                                  |      | 290  |      |      |
| Reverse Transfer Capacitance *1   | Crss     |                                  |      | 250  |      |      |
| Turn-on delay Time *1,*2          | td(on)   | VDD = 10 V, VGS = 0 to 4.0 V     |      | 1.2  |      | μs   |
| Rise Time *1,*2                   | tr       | IS = 4.0 A                       |      | 2.4  |      |      |
| Turn-off delay Time *1,*2         | td(off)  | VDD = 10 V, VGS = 4.0 to 0 V     |      | 8.1  |      | μs   |
| Fall Time *1,*2                   | tf       | IS = 4.0 A                       |      | 3.9  |      |      |
| Total Gate Charge *1              | Qg       | VDD = 10 V                       |      | 35   |      | nC   |
| Gate-source Charge *1             | Qgs      | VGS = 0 to 4.0 V,                |      | 5    |      |      |
| Gate-drain Charge *1              | Qgd      | IS = 4.0 A                       |      | 10   |      |      |

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

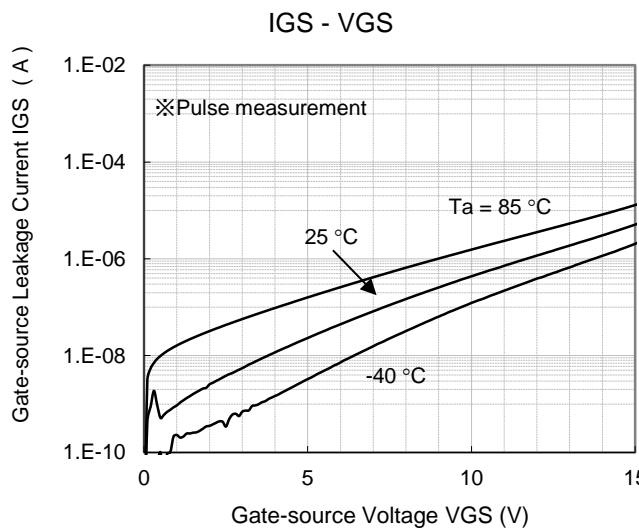
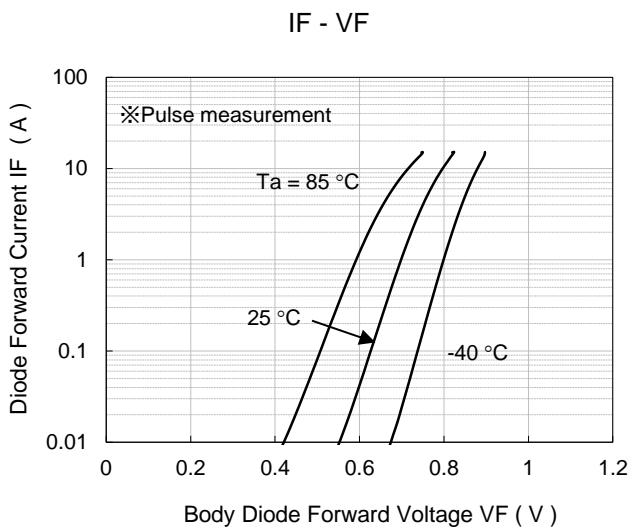
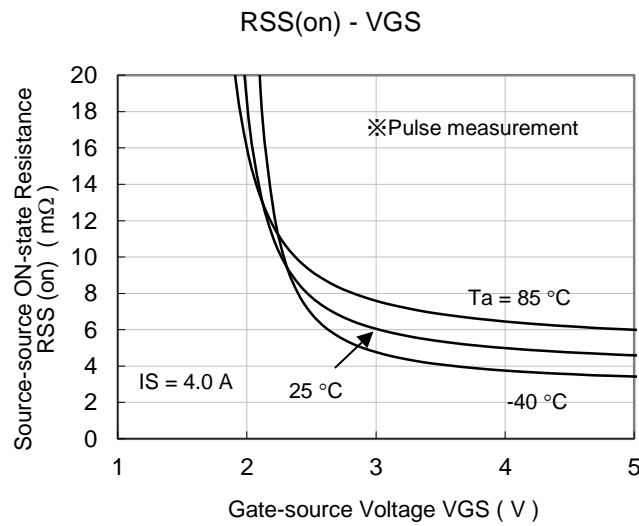
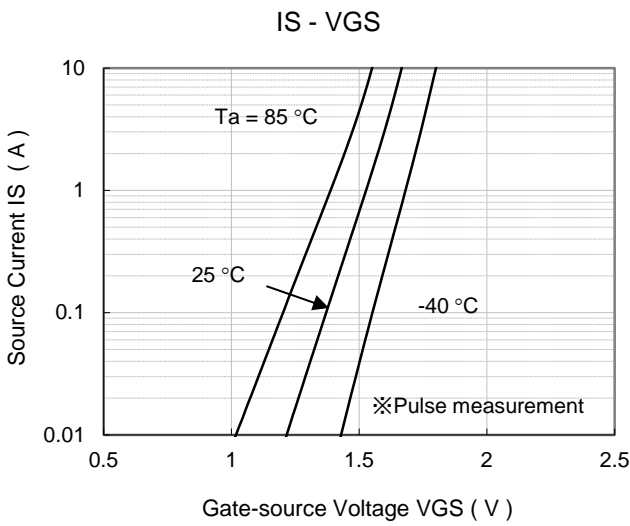
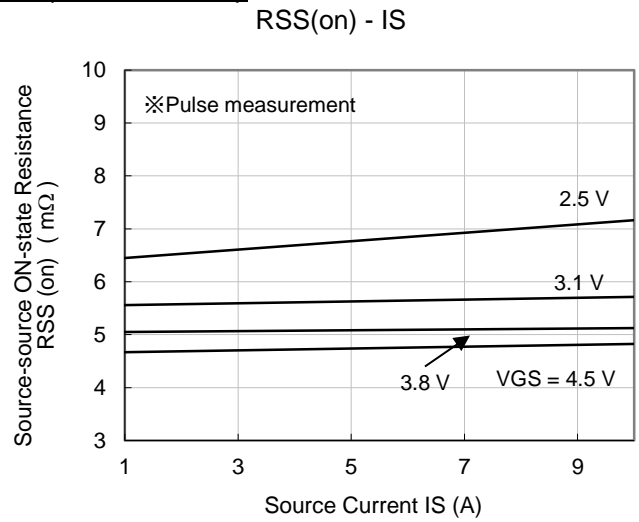
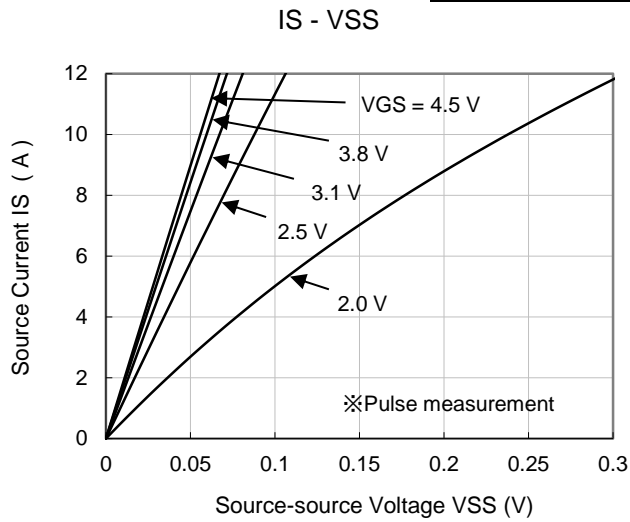
\*1 Guaranteed by design, not subject to production testing

\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Note2 : Measurement circuit



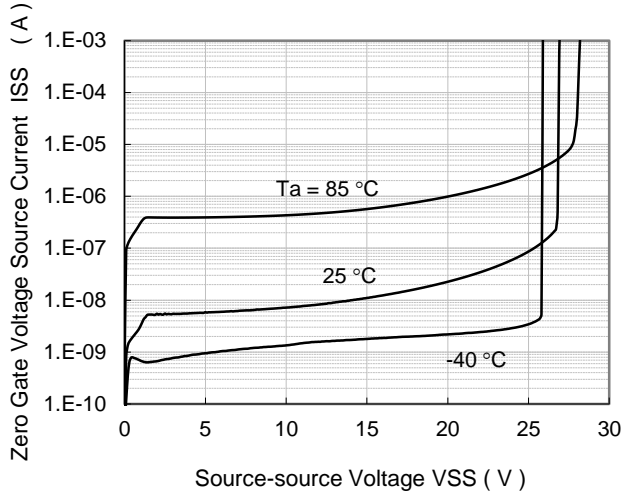
Technical Data ( reference )



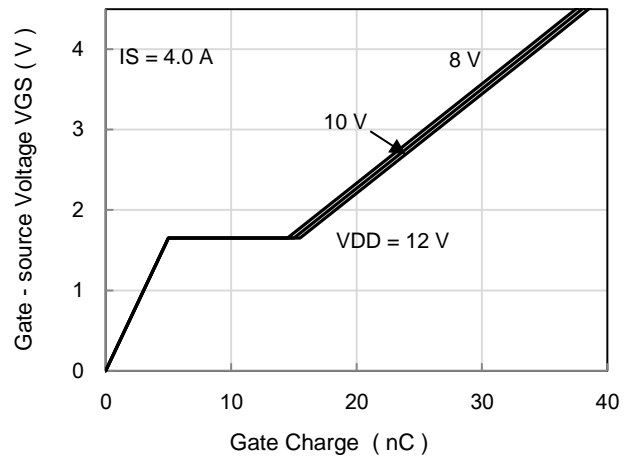


Technical Data ( reference )

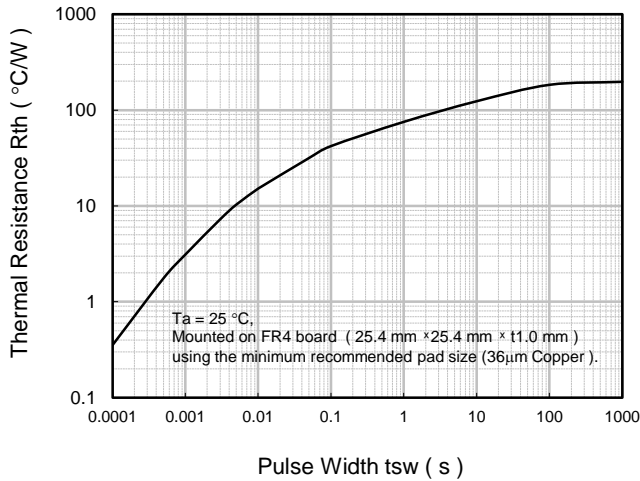
ISS - VSS



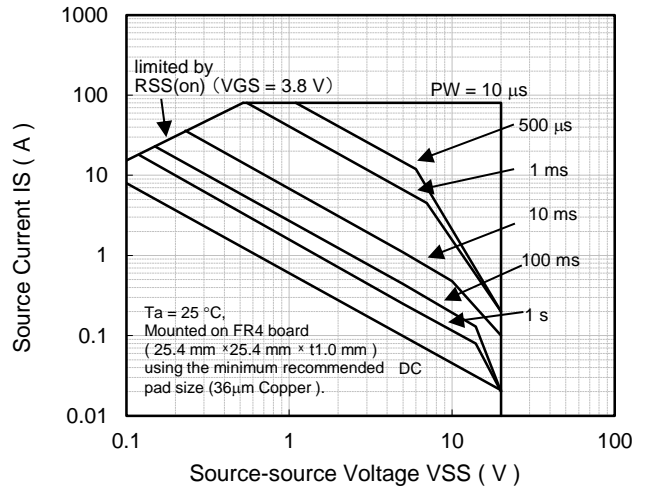
Dynamic Input/Output Characteristics



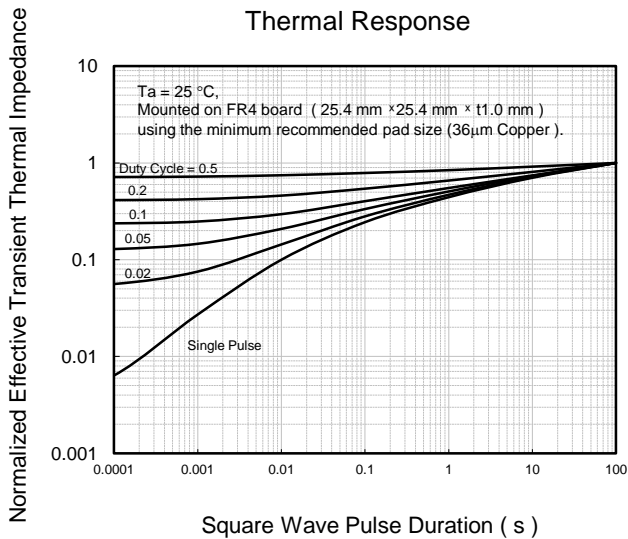
Rth - tsw



Safe Operating Area

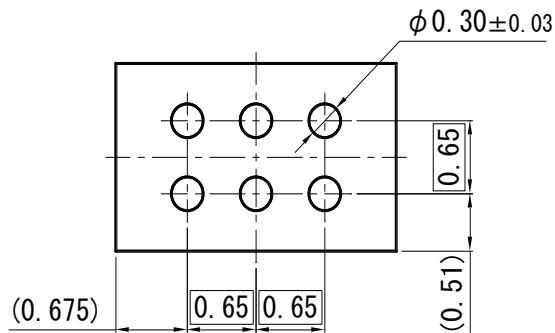
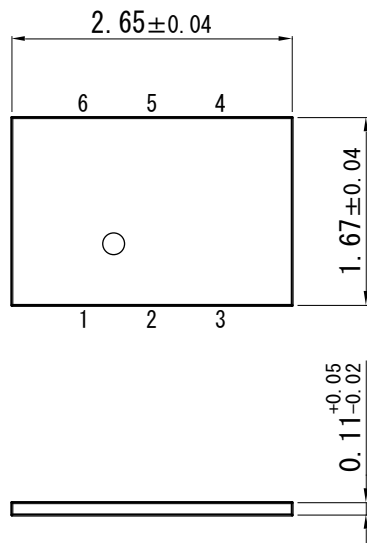


Thermal Response



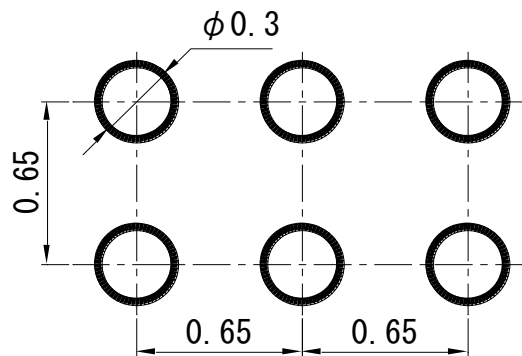
■ Outline (MLGA006-W-1727-RB)

Unit: mm



■ Land Pattern (Reference)

Unit: mm



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